

SONY®

Semiconductor IC

**Data Book
1991
Memory**

SONY

**Semiconductor Integrated Circuit Data Book
1991**

Preface

This is the 1991 version of the Sony Semiconductor IC Memory Databook. This book covers all the memory semiconductor marketed by Sony Corporation of America. In preparation of this databook, as much characteristic and application data as possible have been collected and added with a view of making this book a convenient reference for users of Sony products. If, however, you are dissatisfied with this book in any way, please let us know so that we can improve it.

Index by Usages

1

Description

2

Static RAM

3

ASM (Application Specific Memory)

4

Mask ROM

5

Sales Offices

6

SONY

Semiconductor Integrated Circuit Data Book

1991

Preface

This is the 1991 version of the Sony Semiconductor IC Memory Databook. This book covers all the memory semiconductors marketed by Sony Corporation of America.

In preparation of this databook, as much characteristic and application data as possible have been collected and added with a view of making this book a convenient reference for users of Sony products. If, however, you are dissatisfied with this book in any way, please write, we welcome suggestions and comments.

The contents of this data book although accurate and complete at the time of publication, are subject to change in order to incorporate improvements on the products.

Circuits shown are typical examples illustrating the operation of the devices. They are not meant to convey any patents or other rights. Sony cannot assume responsibility for any problems arising out of the use of these circuits.

Sony reserves the right to change products and specifications without notice. This information does not convey any license under patent rights of Sony Corporation or others.

© 1991 by Sony Corporation of America

Contents

	Page
1. Index by Usage	1
2. Product Overview	3
3. IC Nomenclature	7
4. Precautions for IC Application	
1) Absolute maximum ratings	8
2) Protection against electrostatic breakdown	9
3) Mounting method	13
5. Quality Assurance and Reliability	15
6. Cross Reference	20
7. Sony Package Product Name	24
8. Data Sheets	
1) Static RAM	25
2) ASM (Application Specific Memory)	321
3) Mask ROM	347
9. Sales Office	357

1. Index by Usage

(1) Static RAM (cont.)

1) Static RAM

Type	Function	Process	Page
CXK5164P CXK5164J	65,536 word x 1bit, 25/30/35ns SRAM	MIX CMOS	29
CXK5464AP CXK5464AJ	16,384 word x 4bits, 25/30/35ns SRAM	MIX CMOS	37
CXK5466P CXK5466J	16,384 word x 4bits, 15/20ns SRAM	MIX CMOS	45
CXK5465P CXK5465J	16,384 word x 4bits, 25/30/35ns SRAM with OE	MIX CMOS	53
CXK5467P CXK5467J	16,384 word x 4bits, 15/20ns SRAM with OE	MIX CMOS	61
CXK5863AP CXK5863AJ	8,192 word x 8bits, 20/25/30ns SRAM	FULL CMOS	69
CXK5863P CXK5863M CXK5863J	8,192 word x 8bits, 25/30/35ns SRAM	FULL CMOS	76
CXK5864BP-L/LL CXK5864BSP-L/LL CXK5864BM-L/LL	8,192 word x 8bits, 70/100/120ns SRAM	MIX CMOS	86
CXK5971P CXK5971M CXK5971J	8,192 word x 9bits, 25/30/35ns SRAM	FULL CMOS	96
CXK51256P	262,144 word x 1bit, 35/45/55ns SRAM	MIX CMOS	106
CXK54256P	65,536 word x 4bits, 35/45/55ns SRAM	MIX CMOS	114
CXK58258AP CXK58258AJ	32,768 word x 8bits, 15/20/25ns SRAM	MIX CMOS	122
CXK58258BP-L/LL CXK58258BJ-L/LL CXK58258BM-L/LL	32,768 word x 8bits, 20/25/35ns SRAM	MIX CMOS	129
CXK58258P CXK58258SP	32,768 word x 8bits, 35/45/55ns SRAM	MIX CMOS	137
CXK58257AP-L/LL CXK58257ASP-L/LL CXK58257AM-L/LL	32,768 word x 8bits, 70/85/100/120ns SRAM	MIX CMOS	146
CXK58257AP-LX/LLX CXK58257ASP-LX/LLX CXK58257AM-LX/LLX	32,768 word x 8bits, 70/85/100/120ns SRAM	MIX CMOS	156
CXK58257ATM-L/LL CXK58257AYM-L/LL	32,768 word x 8bits, 70/85/100/120ns SRAM	MIX CMOS	166

1) Static RAM (con't)

Type	Function	Process	Page
CXK58257ATM-LX/LLX CXK58257AYM-LX/LLX	32,768 word x 8bits, 70/85/100/120ns SRAM	MIX CMOS	176
CXK58257P-L/LL CXK58257SP-L/LL CXK58257M-L/LL	32,768 word x 8bits, 70/85/100/120ns SRAM	MIX CMOS	186
CXK58267AP-L/LL CXK58267ASP-L/LL CXK58267AM-L/LL	32,768 word x 8bits, 70/85/100/120ns SRAM 2 CE	MIX CMOS	194
CXK58267ATM-L/LL CXK58267AYM-L/LL	32,768 word x 8bits, 70/85/100/120ns SRAM 2 CE	MIX CMOS	205
CXK59288P CXK59288J	32,768 word x 9bits, 15/20/25ns SRAM	MIX CMOS	216
CXK59290M-L CXK59290TM-L	32,768 word x 9 bits, 70/10/120ns SRAM	MIX CMOS	223
CXK581020SP CXK581020J	131,072 word x 8bits, 35/45/55ns SRAM	MIX CMOS	234
CXK581001P-L/LL CXK581001M-L/LL	131,072 word x 8bits, 70/85ns SRAM	MIX CMOS	243
CXK581000P-L/LL CXK581000M-L/LL	131,072 word x 8bits, 100/120/150ns SRAM	MIX CMOS	252
CXK581000P-LX/LLX CXK581000M-LX/LLX	131,072 word x 8bits, 100/120/150ns SRAM -25°C to +85°C (Extended Temp.)	MIX CMOS	263
CXK581000P-12LB CXK581000M-12LB	131,072 word x8bits, 120ns at V _{CC} =5V 240ns at V _{CC} =3V	MIX CMOS	272
CXK581100TM-L/LL CXK581100YM-L/LL	131,072 words x 8bits, 100/120/150ns SRAM	MIX CMOS	283
CXK581100TM-LX/LLX CXK581100YM-LX/LLX	131,072 words x 8bits, 100/120/150ns SRAM	MIX CMOS	294
CXK581100TM-12LB CXK581100YM-12LB	131,072 word x8bits, 120ns at V _{CC} =5V 240ns at V _{CC} =3V	MIX CMOS	303
CXK541000J	262,144 words x 4bits, 25/30/35ns SRAM	MIX CMOS	314

2) ASM (Application Specific Memory)

CXK7701J	8,192 word x 16bits, 30/35/45ns SRAM	MIX CMOS	324
CXK77910J	131,072 word x 9 bits, 17/20ns SRAM (Synchronous)	MIX CMOS	339

3) Mask ROM

CXK384001	524,288 word x 8bits, 200ns	CMOS	350
-----------	-----------------------------	------	-----

2. Product Over View

1) SRAM

Density	Organization	Product Name	Speed (ns)	Package	Process	Page
64K	64Kx1	CXK5164P -25	25	22pin	MIX CMOS	29
		-30	30	300mil DIP		
		-35	35			
		CXK5164J -25	25	24pin	MIX CMOS	29
		-30	30	300mil SOJ		
		-35	35			
	16Kx4	CXK5466P -15	15	22pin	MIX CMOS	45
		-20	20	300mil DIP		
		CXK5466J -15	15	24pin	MIX CMOS	45
		-20	20	300mil SOJ		
		CXK5464AP -25	25	22pin	MIX CMOS	37
		-30	30	300mil DIP		
		-35	35			
		CXK5464AJ -25	25	24pin	MIX CMOS	37
		-30	30	300mil SOJ		
		-35	35			
		CXK5467P -15	15	24pin	MIX CMOS	61
		w/OE -20	20	300mil DIP		
		CXK5467J -15	15	24pin	MIX CMOS	61
		w/OE -20	20	300mil SOJ		
		CXK5465P -25	25	24pin	MIX CMOS	53
		w/OE -30	30	300mil DIP		
		-35	35			
		CXK5465J -25	25	24pin	MIX CMOS	53
		w/OE -30	30	300mil SOJ		
		-35	35			
8Kx8	8Kx8	CXK5863AP -20	20	28pin	FULL CMOS	69
		-25	25	300mil DIP		
		CXK5863AJ -20	20	28pin	FULL CMOS	69
		-25	25	300mil SOJ		
		CXK5863P -25	25	28pin	FULL CMOS	76
		-30	30	300mil DIP		
		-35	35			
		CXK5863M -25	25	28pin	FULL CMOS	76
		-30	30	450mil SOP		
		-35	35			
		CXK5863J -25	25	28pin	FULL CMOS	76
		-30	30	300mil SOJ		
		-35	35			
	8Kx8	CXK5864BP -70L/LL	70	28pin	MIX CMOS	86
		-10L/LL	100	600mil DIP		
		-12L/LL	120			
		CXK5864BSP -70L/LL	70	28pin	MIX CMOS	86
		-10L/LL	100	300mil DIP		
		-12L/LL	120			
	8Kx8	CXK5864BM -70L/LL	70	28pin	MIX CMOS	86
		-10L/LL	100	450mil SOP		
		-12L/LL	120			

Density	Organization	Product Name	Speed (ns)	Package	Process	Page
72K	8Kx9	CXK5971P	-25	28pin	FULL CMOS	96
			-30	300mil DIP		
			-35			
		CXK5971M	-25	28pin	FULL CMOS	96
			-30	450mil SOP		
			-35			
		CXK5971J	-25	28pin	FULL CMOS	96
			-30	300mil SOJ		
			-35			
256K	256Kx1	CXK51256P	-35	24pin	MIX CMOS	106
			-45	300mil DIP		
			-55			
	64Kx4	CXK54256P	-35	24pin	MIX CMOS	114
			-45	300mil DIP		
			-55			
	32Kx8	CXK58258AP	-15	28pin	MIX CMOS	122
			-20	300mil DIP		
			-25			
		CXK58258AJ	-15	28pin	MIX CMOS	122
			-20	300mil SOJ		
			-25			
		CXK58258BP	-20/LL	28pin	MIX CMOS	129
			-25/LL	300mil DIP		
			-35/LL			
		CXK58258BM	-20/LL	28pin	MIX CMOS	129
			-25/LL	450mil SOP		
			-35/LL			
		CXK58258BJ	-20/LL	28pin	MIX CMOS	129
			-25/LL	300mil SOJ		
			-35/LL			
		CXK58258P	-35	28pin	MIX CMOS	137
			-45	600mil DIP		
			-55			
		CXK58258SP	-35	28pin	MIX CMOS	137
			-45	300mil DIP		
			-55			
		CXK58257AP	-70/LL	28pin	MIX CMOS	146
			-85/LL	600mil DIP		
			-10L/LL			
		CXK58257ASP	-70/LL	28pin	MIX CMOS	146
			-85/LL	300mil DIP		
			-10L/LL			
		CXK58257AM	-70/LL	28pin	MIX CMOS	146
			-85/LL	450mil SOP		
			-10L/LL			
		CXK58257AP	-70LX/LLX	28pin	MIX CMOS	156
			-85LX/LLX	600mil DIP		
			-10LX/LLX			
		CXK58257ASP	-70LX/LLX	28pin	MIX CMOS	156
			-85LX/LLX	300mil DIP		
			-10LX/LLX			
		CXK58257AM	-70LX/LLX	28pin	MIX CMOS	156
			-85LX/LLX	450mil SOP		
			-10LX/LLX			
			-12LX/LLX			

Density	Organization	Product Name	Speed (ns)	Package	Process	Page
256K (Con't)	32Kx8	CXK58257ATM-70L/LL	70	28pin	MIX CMOS	166
		-85L/LL	85	TSOP		
		-10L/LL	100	TM: Normal		
		-12L/LL	120			
		CXK58257AYM-70L/LL	70	28pin	MIX CMOS	166
		-85L/LL	85	TSOP		
		-10L/LL	100	YM: Reverse		
		-12L/LL	120			
		CXK58257ATM-70LX/LLX	70	28pin	MIX CMOS	176
		-85LX/LLX	85	TSOP		
		-10LX/LLX	100	TM: Normal		
		-12LX/LLX	120			
		CXK58257AYM-70LX/LLX	70	28pin	MIX CMOS	176
		-85LX/LLX	85	TSOP		
		-10LX/LLX	100	YM: Reverse		
		-12LX/LLX	120			
		CXK58257P-70L/LL	70	28pin	MIX CMOS	186
		-85L/LL	85	600mil DIP		
		-10L/LL	100			
		-12L/LL	120			
		CXK58257SP-70L/LL	70	28pin	MIX CMOS	186
		-85L/LL	85	300mil DIP		
		-10L/LL	100			
		-12L/LL	120			
		CXK58257M-70L/LL	70	28pin	MIX CMOS	186
		-85L/LL	85	450mil SOP		
		-10L/LL	100			
		-12L/LL	120			
		CXK58267AP-70L/LL	70	28pin	MIX CMOS	194
		-85L/LL	85	600mil DIP		
		-10L/LL	100	2CE		
		-12L/LL	120			
		CXK58267ASP-70L/LL	70	28pin	MIX CMOS	194
		-85L/LL	85	300mil DIP		
		-10L/LL	100	2CE		
		-12L/LL	120			
		CXK58267AM-70L/LL	70	28pin	MIX CMOS	194
		-85L/LL	85	450mil SOP		
		-10L/LL	100	2CE		
		-12L/LL	120			
		CXK58267ATM-70L/LL	70	28pin	MIX CMOS	205
		-85L/LL	85	TSOP		
		-10L/LL	100	TM: Normal		
		-12L/LL	120	2CE		
		CXK58267AYM-70L/LL	70	28pin	MIX CMOS	205
		-85L/LL	85	TSOP		
		-10L/LL	100	YM: Reverse		
		-12L/LL	120	2CE		
288K	32Kx9	CXK59288P-15	15	32pin	MIX CMOS	216
		-20	20	300mil DIP		
		-25	25			
		CXK59288J-15	15	32pin	MIX CMOS	216
		-20	20	300mil SOJ		
		-25	25			
		CXK59290M-70L	70	32pin	MIX CMOS	223
		-10L	100	450mil SOP		
		-12L	120			
		CXK59290TM-70L	70	32pin	MIX CMOS	223
		-10L	100	TSOP		
		-12L	120			

Density	Organization	Product Name	Speed (ns)	Package	Process	Page
1M	128Kx8	CXK581020SP -35	35	32pin	MIX CMOS	234
		-45	45	400mil DIP		
		-55	55			
		CXK581020J -35	35	32pin	MIX CMOS	234
		-45	45	400mil SOJ		
		-55	55			
		CXK581001P -70L/LL	70	32pin	MIX CMOS	243
		-85L/LL	85	600mil DIP		
		CXK581001M -70L/LL	70	32pin	MIX CMOS	243
		-85L/LL	85	525mil SOP		
		CXK581000P -10L/LL	100	32pin	MIX CMOS	252
		-12L/LL	120	600mil DIP		
		-15L/LL	150			
		CXK581000M -10L/LL	100	32pin	MIX CMOS	252
		-12L/LL	120	525mil SOP		
		-15L/LL	150			
		CXK581000P -10LX/LLX	100	32pin	MIX CMOS	263
		-12LX/LLX	120	600mil DIP		
		-15LX/LLX	150			
		CXK581000M -10LX/LLX	100	32pin	MIX CMOS	263
		-12LX/LLX	120	525mil SOP		
		-15LX/LLX	150			
		CXK581000P -12LB	120	32pin	MIX CMOS	273
		-12LB	240 (V _{CC} =3V)			
		CXK581000M -12LB	120	32pin	MIX CMOS	273
		-12LB	240 (V _{CC} =3V)			
		CXK581100TM -10L/LL	100	32pin	MIX CMOS	283
		-12L/LL	120	TSOP		
		-15L/LL	150	(EIAJ Standard)		
		CXK581100YM -10L/LL	100	32pin	MIX CMOS	283
		-12L/LL	120	TSOP		
		-15L/LL	150	(EIAJ Standard)		
		CXK581100TM -10LX/LLX	100	32pin	MIX CMOS	294
		-12LX/LLX	120	TSOP		
		-15LX/LLX	150	(EIAJ Standard)		
		CXK581100YM -10LX/LLX	100	32pin	MIX CMOS	294
		-12LX/LLX	120	TSOP		
		-15LX/LLX	150	(EIAJ Standard)		
		CXK581100TM -12LB	120	TSOP		303
		-12LB	240 (V _{CC} =3V)			
		CXK581100YM -12LB	120	TSOP		303
		-12LB	240 (V _{CC} =3V)			
		CXK541000J -25	25	32pin	MIX CMOS	314
		-30	30	400mil SOJ		
		-35	35			

2) ASM (Application Specific Memory)

128K	4Kx16x2way	CXK7701J -30	30	52pin	MIX CMOS	324
	8Kx16	-35	35	PLCC		
		-45	45			
1.1M	128Kx9	CXK77910J -17	17	32pin	MIX CMOS	339
	(Synchronous)	-20	20	400mil SOJ		

3) Mask ROM

4M	512Kx8	CXK384001	200	32pin	CMOS	350
				600mil DIP		

3. IC Nomenclature

1) Nonmenclature of IC product name

Currently, both the conventional and new nomenclature systems are mixed in naming IC products.

a) Memory Nomenclature

(Example) C X K 5 4 6 4 A P - xx xx x

Special Specifications

X = Extended Temperature

B = Wide Vcc

Y = Extended Temperature & Wide Vcc

Standby Current

Access Time

Package Mark

P : Dual in-line package

SP : Skinny outline package

M : Small outline package

J : Small outline J-leaded package

Quad Flat J-leaded package

TM : Thin small outline package

(mirror image pin out)

YM : Thin small outline package

Improvement Mark

Improvement mark is affixed when specifications are partially improved.

Product Number

Identifies the individual product.

Product Category Mark

K : Memory

Sony IC Mark

b) Mask ROM Nomenclature

(Example) C X K 3 8 1 2 8 - xxx x

Package mark (P,M)

OEM Code

Product Number

Identifies the individual product.

Product Category Mark

K : Mask POM

Sony IC Mark

4. Precautions for IC Application

1) Absolute maximum ratings

The maximum ratings for semiconductor devices are normally specified by "absolute maximum ratings". The values shown in the maximum ratings table must never be exceeded even for a moment.

If the maximum rating is ever exceeded, device deterioration or damage will occur immediately. Then, even if the affected device can operate, the life will be considerably shortened.

Maximum rating must never be reached for any TWO items at the SAME time.

IC maximum ratings

The following maximum ratings are used for ICs.

(1) Maximum power supply voltage V_{CC} (V_{DD})

The maximum voltage that can be applied between the power supply pin and ground pin.

This power supply voltage rating is directly related to the dielectric voltage of transistors in the internal circuit, the transistors may be destroyed if this voltage is exceeded.

(2) Allowable power dissipation P_D

The maximum power consumption allowed in IC.

In the circuit design the absolute maximum ratings must not be exceeded, and it must be designed only after considering the worst situations among the following :

- Fluctuation in source voltage
- Scattering in the electrical characteristics of electrical parts (transistors, resistors, capacitors, etc.)
- Power dissipation in circuit adjustment
- Ambient temperature
- Fluctuation in input signal
- Abnormal pulses

If this allowable power dissipation is exceeded, electrical and thermal damage may result.

This value varies with amount of IC integration in package types.

(3) Operating ambient temperature T_{opr}

The temperature range within which IC can operate satisfactorily.

Even if this temperature range is exceeded and some deterioration in operating characteristics is noted, the IC is not always damaged.

For some ICs, the electrical characteristics at $T_a = 25^\circ\text{C}$ are not guaranteed even in this temperature range.

(4) Storage temperature T_{stg}

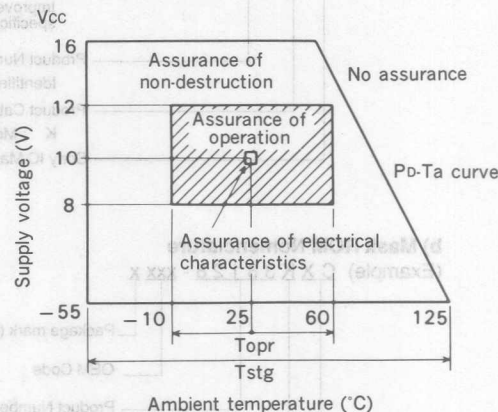
The temperature range for storing the IC which is not operating.

This temperature is restricted by the package material, and the intrinsic properties of the semiconductor.

(5) Other values

The input voltage V_{in} , output voltage V_{out} , input current I_{in} , output current I_{out} and other values may be specified in some IC's.

The relationship among these maximum ratings for IC is shown below.



2) Protection against electrostatic breakdown

There have been problems concerning electrostatic destruction of electronic devices since the 2nd World War. Those are closely related to the advancement made in the field of semiconductor devices; this is, with the development of semiconductor technology, new problems in electrostatic destruction have arisen. This situation, perhaps, can be understood by recalling the case of MOS FET.

Today, electrostatic destruction is again drawing people's attention as we are entering the era of LSI and VLSI. Here are our suggestions for preventing such destruction in the device fabrication process.

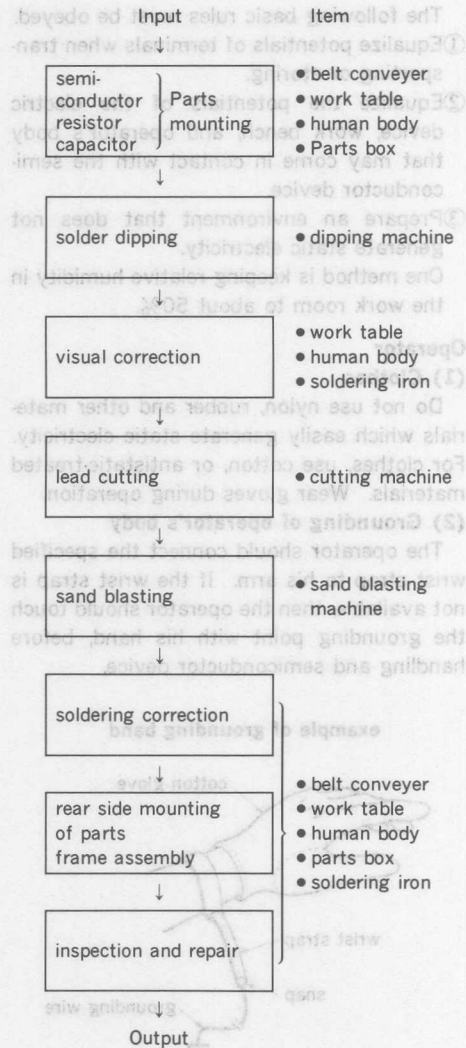
Factors causing electrostatic generation in manufacture process

A number of dielectric materials are used in manufacture process. Friction of these materials with the substrate can generate static electricity which may destroy the semiconductor device.

Factors that can cause electrostatic destruction in the manufacture process are shown below:



Causes of electrostatic destruction of semiconductor parts in manufacture process



Handling precautions for the prevention of electrostatic destruction

Explained below are procedures that must be taken in fabrication to prevent the electrostatic destruction of semiconductor devices.

The following basic rules must be obeyed.

- ① Equalize potentials of terminals when transporting or storing.
- ② Equalize the potentials of the electric device, work bench, and operator's body that may come in contact with the semiconductor device.
- ③ Prepare an environment that does not generate static electricity.
One method is keeping relative humidity in the work room to about 50%.

Operator

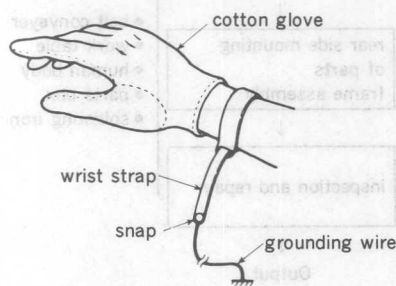
(1) Clothes

Do not use nylon, rubber and other materials which easily generate static electricity. For clothes, use cotton, or antistatic-treated materials. Wear gloves during operation.

(2) Grounding of operator's body

The operator should connect the specified wrist strap to his arm. If the wrist strap is not available, then the operator should touch the grounding point with his hand, before handling and semiconductor device.

example of grounding band

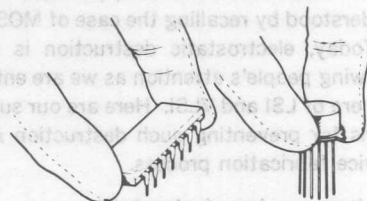


When using a copper wire for grounding, connect a 1MΩ resistance in series near the hand for safety.

(3) Handling of semiconductor device

Do not touch the lead. Touch the body of the semiconductor device when holding. Limit the number of handling times to a minimum. Do not take the device out of the magazine or package box unless it is absolutely necessary.

holding of semiconductor device



Equipment and tools

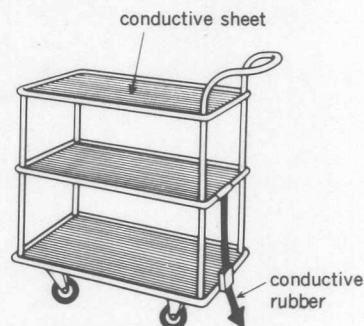
(1) Grounding of equipment and tools

Ground the equipments and tools that are to be used. Check insulation beforehand to prevent leakage.

[Check point]

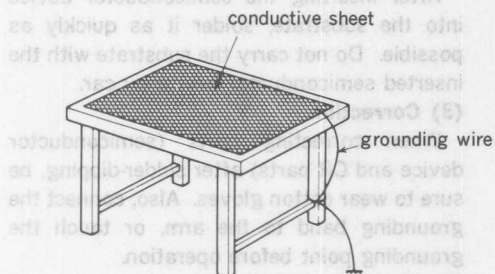
- measuring instrument
- conveyer
- electric deburr brush
- carrier
- solder dipping tank
- lead cutter
- shelves and racks

grounding of carrier



not put anything which can easily generate static electricity, such as foam styrol, on the work table.

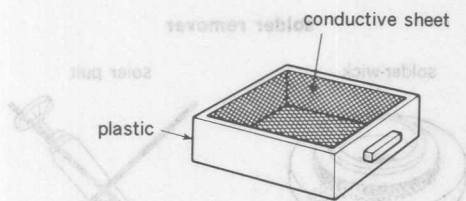
grounding of work table



(3) Semiconductor device case

Use a metal case, or an antistatic plastic case (lined with conductive sheet).

plastic case for semiconductor devices



(4) Insertion of semiconductor device

Insert the semiconductor device during the mounting process or on the belt conveyer. The insertion should be done on a conductive sheet, or on a wood or on a metal carrier.

(5) Operation in energized state

When the substrate is checked while energizing the substrate where the delicate semiconductor device is mounted, be sure to place the substrate on corrugated cardboard, wood, or on a metal carrier.

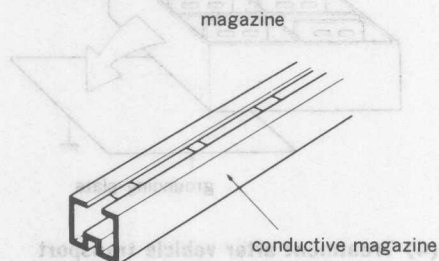
used for removing lead chips. Use metal or antistatic-treated plastic brushes.

Transporting, storing and packaging methods

(1) Magazine

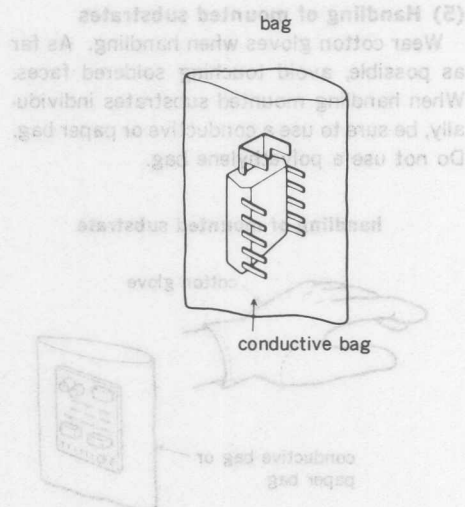
Use metal, or antistatic-treated plastic IC magazines.

Plastic magazines used for shipping ICs are antistatic-treated, and they can be used for storing ICs.



(2) Bag

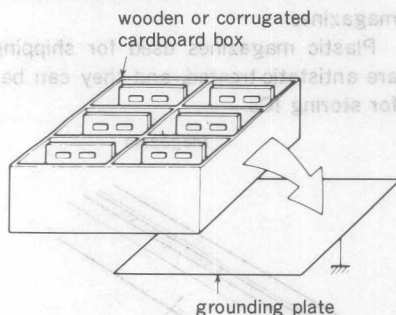
Use a conductive bag to store ICs. If the use of vinyl bag is unavoidable, be sure to wrap the IC with aluminum foil.



(3) Handling of delivery box

The delivery box used for carrying substrates must be made of wood or corrugated cardboard. Do not use a vinyl chloride or acrylic delivery box, otherwise static electricity will be generated.

handling of delivery box



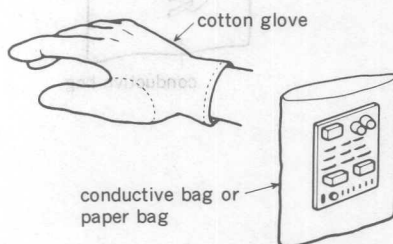
(4) Treatment after vehicle transport

After truck transport, place the magazine, package box or delivery box on the grounded rack, work table, or concrete floor for discharging. Do not pull the delivery box for more than 1 meter except on a concrete or a wooden floor.

(5) Handling of mounted substrates

Wear cotton gloves when handling. As far as possible, avoid touching soldered faces. When handling mounted substrates individually, be sure to use a conductive or paper bag. Do not use a polyethylene bag.

handling of mounted substrate



Soldering operation

(1) Soldering iron

Use a soldering iron with a grounded metal part or a soldering iron with an insulation resistance greater than $10M\Omega$ (DC 500V) after five minutes from energizing.

(2) Operation

After inserting the semiconductor device into the substrate, solder it as quickly as possible. Do not carry the substrate with the inserted semiconductor device by ear.

(3) Correction

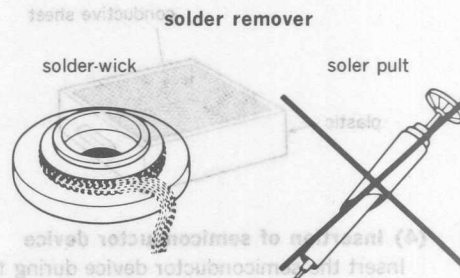
When correcting parts (semiconductor device and CR parts) after solder-dipping, be sure to wear cotton gloves. Also, connect the grounding band to the arm, or touch the grounding point before operation.

(4) Manual soldering

Solder with wrist strap connected to the hand, or by touching the grounding point from time to time during operation.

(5) Removing semiconductor device

Do not use the Solder-Pult when removing the semiconductor device. Use a Solder-wick or equivalent.



(6) Soldering work table

Use a grounded work table, corrugated cardboard, or wooden work table for soldering. Do not solder on foam styrol, vinyl, or decorative board.

3) Mounting method

Soldering and solderability

(1) Solderability by JIS

JIS specifies solderability of an IC terminal (lead) in "JIS-C7022 Test Procedure A-2".

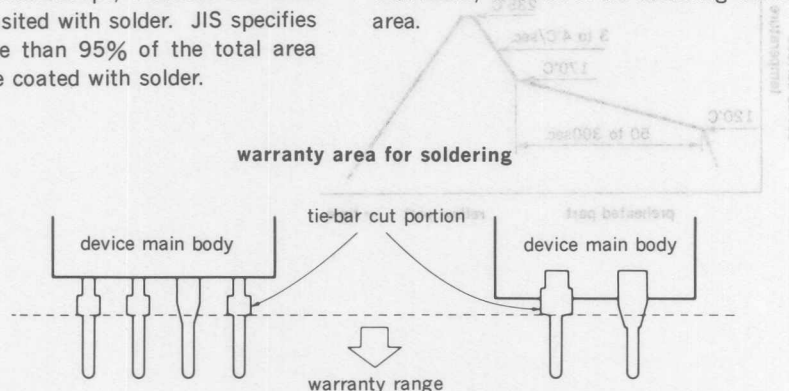
An abstract of this standard follows:

- Rosin flux must be used, and the terminal must be dipped in it for 5-10 seconds.
- H63A or equivalent solder must be used, and the terminal must be dipped in the solder which been heated to $230^{\circ}\text{C} \pm 5^{\circ}\text{C}$ for 5 ± 1 seconds.
- Using a microscope, measure the area (%) deposited with solder. JIS specifies that more than 95% of the total area should be coated with solder.

(2) Area for soldering warranty

Soldering is warranted for a specific portion of the terminal. The warranted portion is shown in the following figure.

The tie-bar cut portion also serves as a dam to prevent the sealing resin flowing out during device fabrication; it is cut off at the end of the process. Since the terminal is exposed at the cut-off end, the area for soldering is restricted. The portion near the resin is often covered with burrs when sealing with resin; it is not in the soldering warranty area.



Resistance to soldering heat

(1) Specification of JIS

JIS specifies the method for testing the resistance to soldering heat. This method is used for guaranteeing the IC resistance against thermal stresses by soldering. An abstract of this standard is as follows:

- Dip the device terminal only once for 10 ± 1 seconds in a solder bath of $260^{\circ}\text{C} \pm 5^{\circ}\text{C}$, or for 3 ± 0.5 seconds in a solder bath of $350^{\circ}\text{C} \pm 10^{\circ}\text{C}$, for a distance of up to 1 to 1.5 mm from the main body.

For the solder flow system temperature should be $260^{\circ}\text{C} \pm 5^{\circ}\text{C}$. To solder by soldering iron temperature should be $350^{\circ}\text{C} \pm 10^{\circ}\text{C}$.

- Leave the device for more than two hours after dipping, then measure the device characteristics.
- Normally, the warranty is limited to 10 seconds at $260^{\circ}\text{C} \pm 5^{\circ}\text{C}$. The distance between the device main body and solder bath is 1.6 mm.

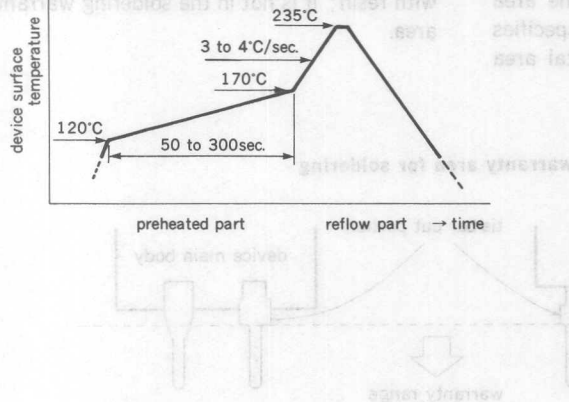
(2) Resistance to soldering heat when mounting infrared reflow.

When surface mount Devices (SOP, QFP etc) are dipped directly into a solder pot.

The device moisture resistance may deteriorate and thermal stress generate cracks in the pallet.

Carefully observe the mounting conditions.

Recommended temperature profile when mounting infrared reflows is shown in the figure below.



For the solder flow system temperature should be $250^{\circ}\text{C}\pm 5^{\circ}\text{C}$. To solder by soldering iron temperature should be $350^{\circ}\text{C}\pm 10^{\circ}\text{C}$.

- Leave the device for more than two hours after dipping, then measure the device characteristics.
- Normally, the warranty is limited to 10 seconds at $250^{\circ}\text{C}\pm 5^{\circ}\text{C}$. The distance between the device main body and solder bath is 1.8 mm.

(3) Mounting method

Soldering and solderability

(1) Solderability by JIS

JIS specifies solderability of an IC terminal (lead) in "JIS-C1022 Test Procedure A-2". An abstract of this standard follows:

- Rosin flux must be used and the terminal must be dipped in it for 5-10 seconds.
- H63A or equivalent solder must be used, and the terminal must be dipped in the solder which has been heated to $250^{\circ}\text{C}\pm 5^{\circ}\text{C}$ for 5 ± 1 seconds.
- Using a microscope, measure the area (%) deposited with solder. JIS specifies that more than 55% of the total area should be coated with solder.

Resistance to soldering heat

(1) Specification of JIS

JIS specifies the method for testing the resistance to soldering heat. This method is used for guaranteeing the IC resistance against thermal stresses by soldering. An abstract of this standard is as follows:

- Dip the device terminal only once for 10 ± 1 seconds in a solder bath of $250^{\circ}\text{C}\pm 5^{\circ}\text{C}$ or for 5 ± 1 seconds in a solder bath of $350^{\circ}\text{C}\pm 10^{\circ}\text{C}$ for a distance of up to 1 to 1.5 mm from the main body.

5. Quality Assurance and Reliability

The Concept to Quality Assurance

There are 2 fundamental principles guiding Sony Semiconductors.

1. Customer satisfaction
2. Top level performance

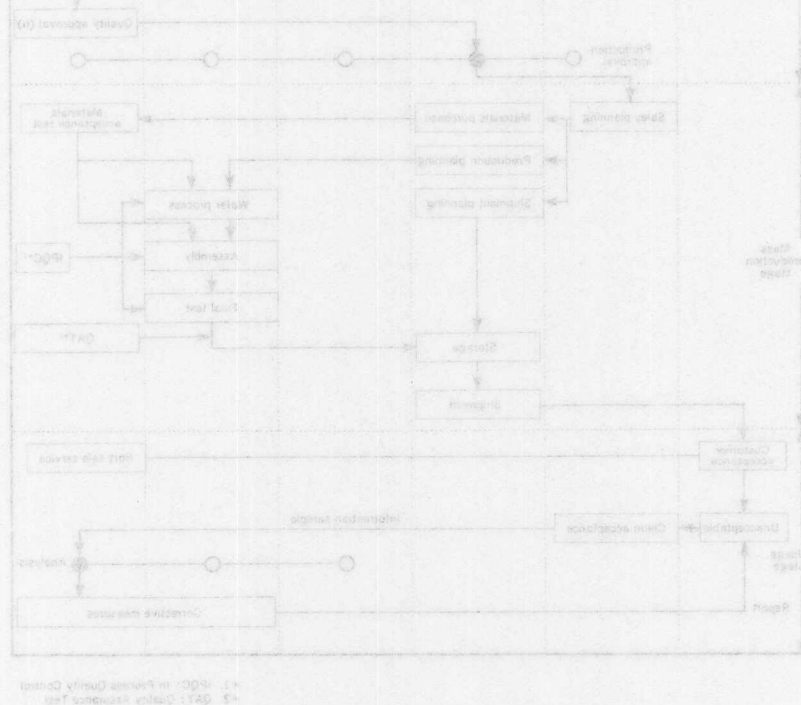
What comes first is the ability to respond convincingly to given requirements in terms of Quality, Delivery, Cost and Servicing. This involves all operations involved in the process. The second requisite is the quest for superior accomplishment. Here, talent is demanded to fulfill customer expectations, where quality is concerned, and pursue related activities.

To this effect an elaborate system of quality assurance is firmly established. From the early stages of research and development well into production, sales and servicing,

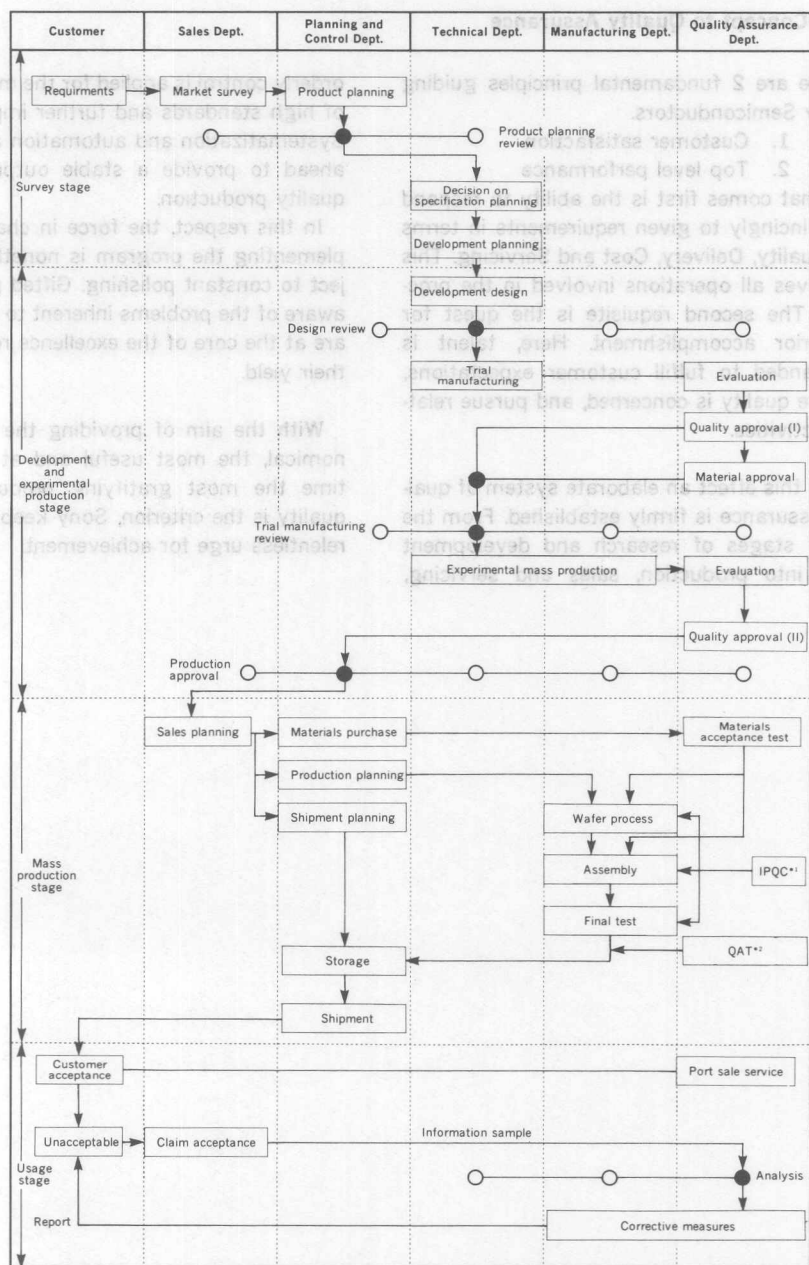
orderly control is applied for the maintenance of high standards and further improvement. Systematization and automation are pushed ahead to provide a stable output of high quality production.

In this respect, the force in charge of implementing the program is nonetheless subject to constant polishing. Gifted people well aware of the problems inherent to their tasks are at the core of the excellence reflected on their yield.

With the aim of providing the most economical, the most useful and at the same time the most gratifying products where quality is the criterion, Sony keeps fueling a relentless urge for achievement.



Quality assurance system of semiconductor products



*1. IPQC: In Process Quality Control
*2. QAT: Quality Assurance Test

Quality assurance criteria and reliability test criteria

1) Quality assurance in shipping

Establishing quality in the design and in fabrication is essential to keep the quality and reliability levels of the semiconductor devices at a high level. This is done by the "Zero-defect" (ZD) movement. Further sampling checks, in units of shipping lot, is done on products that have been "totally-

inspected" at the final fabrication stage, thus ensuring no defective items. This sampling inspection is done in accordance with MIL-STD-105D.

2) Reliability

The reliability test is done, periodically, to confirm reliability level.

Periodic Reliability Test

Item	Testing time	LTPD
Electrical Characteristics Test	In order to know the initial quality level, some types are selected and tested again.	
Life Test	high temperature operation high temperature and high humidity with bias pressure cooker	up to 1000 h up to 1000 h up to 200 h
Environmental Test	soldering heat resistance heat cycle	10s 100 cycles
Mechanical Test	solderability length strength	Japan Industrial Standard (JIS)
Other Tests	If necessary, tests are selected according to JIS C7021 C7022 and EIAJ SD121 IC121.	

*These tests are selected by sampling standard.

LTPD: Lot Tolerance Percent Defective

These tests and inspection data are useful not only to improve design and wafer processes, but also serve to forecast reliability at the consumer level.

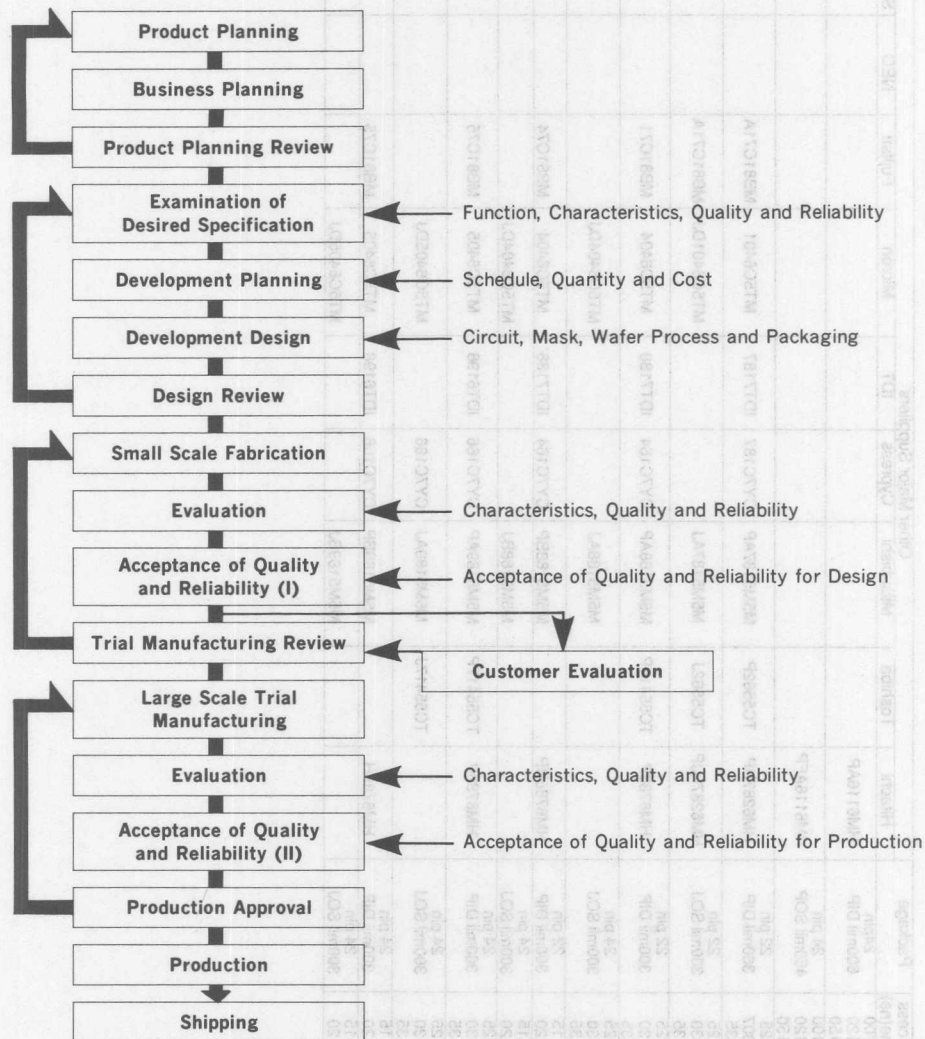
Reliability Test Standards

Types of test	Condition	Supply voltages	Testing time	LTPD
High temperature operation	Ta=125°C, 150°C	Typical	1000h	5%
High temperature with bias	Ta=125°C, 150°C	Typical	1000h	5%
High temperature storage	Ta=150°C		1000h	5%
Low temperature storage	Ta= -65°C		1000h	5%
High temperature and high humidity storage	Ta=85°C 85%RH		1000h	5%
High temperature and high humidity with bias	Ta=85°C 85%RH	Typical	1000h	5%
Pressure cooker	Ta=121°C 100%RH 30 pounds per square inch		200h	5%
Temperature cycle	Ta= -65°C to +150°C		100c	10%
Heat shock	Ta= -65°C to +150°C		100c	10%
Soldering heat resistance	T solder=260°C		10s	10%
Solderability	T solder=230°C (rosin type flux)		5s	10%
Mechanical shock	X, Y, Z 1500G Half part of sinusoidal wave of 0.5ms		3times for each direction	10%
Vibration	X, Y, G 20G 10Hz to 2000Hz to 10Hz (4min) Sinusoidal wave vibration		16minutes for each direction	10%
Constant acceleration	X, Y, Z 20,000G Centrifugal acceleration		1minute for each direction	10%
Free fall	Free fall from the height of 75cm to maple plate		3times	10%
Lead strength (bend) (pull)		based on JIS		10%
Electrostatic strength	Device must be designed again, when electrostatic strength below standard supplying surge voltage to each pin under the condition of C=200pF and Rs=0Ω.			

LTPD: Lot Tolerance Percent Defective

Flow Chart from Development to Manufacturing

Sony attains high quality and high reliability of semiconductor products by designing devices with quality and reliability from the initial steps of development and evaluating them sufficiently in each step of the development.



6. SRAM Cross Reference Guide

Density	Organ-ization	Product Name	Access Time(ns)	Package	Other Major Suppliers											
					Hitachi	Toshiba	Mitsubishi	Cypress	IDT	Micron	Fujitsu	NEC	Samsung	Motorola		
16K	2Kx8	CXK5816PN-10L	100	24pin	HM6116AP											
		-12L	120	600mil DIP												
		-15L	150													
		CXK5816M-10L	100	24 pin	HM6116AFP											
		-12L	120	450mil SOP												
		-15L	150													
64K	64Kx1	CXK5164P-25	25	22 pin	HM6287HP	TC5562P	M5M5187AP	CY7C187	IDT7187	MT5C6401	MB81C71A			MCM6287		
		-30	307	300mil DIP												
			-35	35												
			CXK5164J-25	25	22 pin	HM6287HJP	TC5562J	M5M5187AJ			MT5C6401DJ	MB81C71A		MCM6287		
			-30	30	300mil SOJ											
			-35	35												
		16Kx4	CXK5464AP-25	25	22 pin	HM6788P	TC55416P	M5M5188AP	CY7C164	IDT7188	MT5C6404	MB81C71				
				-30	30											300mil DIP
				-35	35											
				CXK5464AJ-25	25	24 pin			M5M5188AJ			MT5C6404DJ				
				-30	30	300mil SOJ										
				-35	35											
				CXK5466P-15	15	22 pin	HM6788HP		M5M5188BP	CY7C164	IDT7188	MT5C6404	MB81C74		MCM6288	
				-20	20	300mil DIP										
				CXK5466J-15	15	24 pin			M5M5188BJ			MT5C6404DJ			MCM6288	
				-20	20	300mil SOJ										
				CXK5465P-25	25	24 pin	HM6789P	TC55417P	M5M5189AP	CY7C166	IDT6198	MT5C6405	MB81C75			
				-30	30	300mil DIP										
			-35	35												
			CXK5465J-25	25	24 pin		TC55417J	M5M5189AJ	CY7C166		MT5C6405DJ					
		-30	30	300mil SOJ												
		-35	35													
		CXK5467P-15	15	24 pin	HM6789H		M5M5189BP	CY7C166	IDT6198	MT5C6405	MB81C75			MCM6290		
		-20	20	300mil DIP												
		CXK5467J-15	15	24 pin			M5M5189BJ			MT5C6405DJ				MCM6290		
		-20	20	300mil SOJ												

SRAM Cross Reference Guide (con't)

Density	Organ-ization	Product Name	Access Time(ns)	Package	Other Major Suppliers									
					Hitachi	Toshiba	Mitsubishi	Cypress	IDT	Micron	Fujitsu	NEC	Samsung	Motorola
64K (Con't)	8Kx8	CXK5866P-12	12	28 pin		TC5588D		CY7C185	IDT7164	MT5C6408				MCM6264
		-15	15	300mil DIP										
		-20	20											
		CXK5866J-12	12	28 pin		TC5588J		CY7C185		MT5C6408DJ				MCM6264
		-15	15	300mil SOJ										
		-20	20											
		CXK5863AP-20	20	28 pin		TC5588P		CY7C185	IDT7164	MT5C6408				MCM6264
		-25	25	300mil DIP										
		CXK5863AJ-20	20	28 pin		TC588J		CY7C185		MT5C6408DJ				MCM6264
		-25	25	300mil SOJ										
		CXK5863P-25	25	28 pin		TC5588P		CY7C185	IDT7164	MT5C6408	MB81C78A			MCM6264
		-30	30	300mil DIP										
-35	35													
CXK5863M-25	25	28 pin												
-30	30	450mil SOP												
-35	35													
CXK5863J-25	25	28 pin												
-30	30	300mil SOJ		TC5588J		CY7C185		MT5C6408DJ				MCM6264		
-35	35													
CXK5864BP-70L	70	28 pin		HM6264AP	TC5563AP	M5M5165P			MB8464A	MPD4364	KM6264AP			
-10L	100	600mil DIP												
-12L	120													
CXK5864SP-70L	70	28 pin												
-10L	100	300mil DIP		HM6264ASP							KM6264AG			
-12L	120													
CXK5864BM-70L	70	28 pin		HM6264AFP	TC5563AF	M5M5165FP			MB8464A					
-10L	100	450mil SOP												
-12L	120													
72K	8Kx9	CXK5971P-25	25	28 pin		TC5589P				MB81C79A			MCM6265	
		-30	30	300mil DIP										
		-35	35											
		CXK5971J-25	25	28 pin		TC5589J							MCM6265	
		-30	30	300mil SOJ										
		-35	35											
		CXK5971M-25	25	28pin						MB81C79A				
		-30	30	450mil SOP										
		-35	35											
		CXK5972P-12	12	28 pin		TC5589P				MB82B79			MCM6265	
		-15	15	300mil DIP										
		-20	20											
CXK5972J-12	12	28pin		TC5589J							MCM6265			
-15	15	300mil SOJ												
-20	20													

SRAM Cross Reference Guide (con't)

SRAM Cross Reference Guide (con't)

Density	Organ-ization	Product Name	Access Time(ns)	Package	Other Major Suppliers									
					Hitachi	Toshiba	Mitsubishi	Cypress	IDT	Micron	Fujitsu	NEC	Samsung	Motorola
256K	256Kx1	CXK51256P-35	35	24 pin										
		-45	45	300mil DIP	HM6207		M5M5257P	CY7C197	IDT71257	MT5C2561	MB81C81	MPD43254	KM61257P	
	64Kx4	CXK54256P-35	35	24 pin										
		-45	45	300mil DIP	HM6208	TC55465P	M5M5258P	CY7C194	IDT71258	MT5C2564	MB81C86		KM64257P	
	32Kx8	CXK58258P-35	35	28 pin										
		-45	45	600mil DIP				CY7C198	IDT71256	MT5C2568W				
		-55	55											
		CXK58258SP-35	35	28 pin	HM62832	TC55328P		CY7C199		MT5C2568				
		-45	45	300mil DIP										
		-55	55											
		CXK58258AJ-15	15	28 pin										
		-20	20	300mil SOJ		T55328J				MT5C2568				
		-25	25											
		CXK58258AP-15	15	28 pin										
		-20	20	300mil DIP		T55328P		CY7C199		MT5C2568				MCM6206
		-25	25											
		CXK58258BP-20L	20	28 pin										
		-25L	25	300mil DIP					IDT712564L					
		-35L	35											
		CXK58258BJ-20L	20	28 pin										
		-25L	25	300mil SOJ										
		-35L	35											
CXK58258BM-20L	20	28 pin												
-25L	25	450mil SOP					IDT712564L							
-35L	35													
512K	32Kx8	CXK58257P-85L	85	28 pin	HM62256P	TC55257 AP	M5M255P				MB84256	MPD43256A	KM62256AP	
		CXK58257AP-10L	100	600mil DIP			M5M256P							
		-12L	120											
		-70L	70											
		CXK58257SP-85L	85	28 pin										
		CXK58257ASP-10L	100	300mil DIP										
		-12L	120											
		-70L	70											
		CXK58257M-85L	85	28 pin	HM62256FP	TC55257 AF	M5M255FP				MB84256		KM62256AG	
		CXK58257AM-10L	100	450mil SOP			M5M256FP							
		-12L	120											
		-70L	70											
CXK58257ATM-85L	85	28 pin												
CXK58257AYM-10L	100	(*) TSOP												
-12L	120													
(*) Mitsubishi Pin Compatible														

SRAM Cross Reference Guide (con't)

Density	Organ-ization	Product Name	Access Time(ns)	Package	Other Major Suppliers									
					Hitachi	Toshiba	Mitsubishi	Cypress	IDT	Micron	Fujitsu	NEC	Samsung	Motorola
288K	32Kx9	CXK59288P-15	15	32 pin										
		-20	20	300mil DIP		T55329P			IDT71259					MCM6205
		-25	25											
		CXK59288J-15	15	32 pin										
		-20	20	300mil SOJ		T55329J								MCM6205
		-25	25											
1M	128Kx8	CXK581020SP-35	35	32 pin										
		-45	45	400mil DIP						MT5C1008				
		-55	55											
		CXK581020J-35	35	32 pin										
		-45	45	400mil SOJ										
		-55	55											
		CXK581001P-70L	70	32pin										
		-85L	85	600mil DIP	HM628128P	TC551001P	M5M51008P						KM581000P	
		CXK581001M-70L	70	32pin										
		-85L	85	525mil SOP	HM628128FP		M5M51008FP						KM581000G	
126K	4Kx16x 2 way & 8Kx16	CXK581000P-10L	100	32 pin										
		-12L	120	600mil DIP	HM628128P	TC551001P	M5M51008P						KM581000P	
		-15L	150											
		CXK58000M-10L	100	32 pin										
		-12L	120	525mil SOP	HM628128FP		M5M51008FP						KM581000G	
		-15L	150											
		CXK581100TM-10L	100	TSOP	HM628128TS		M5M51008VP							
		CXK581100YM-12L	120	(EIAJ Standard)			M5M51008RV							
		-15L	150											
				CXK7701J-30	30									
		-35	35											
		-45	45	52 pin	HM62A168	TC55168T		CY7C184		MT56C2416EJ	V63C328 (Vitellic)			
		-55	55	PLCC										
		CXK7701AJ-25	25	52 pin										
		-35	35	PLCC										
		-45	45		HM62A168	TC55168T		CY7C184		MT56C2416EJ	V63C328 (Vitellic)			

7. Sony Package Product Name

Type	Package name		Package	Features			
	Symbol	Description		Material*	Lead pitch	Lead shape	Lead pull out direction
Inserted	Standard	D I P	DUAL IN-LINE PACKAGE	P C	2.54mm (100MIL)	Through Hole Lead	2-direction
		S I P	SINGLE IN-LINE PACKAGE	P	2.54mm (100MIL)	Through Hole Lead	1-direction
		Z I P	Zig-Zag IN-LINE PACKAGE	P	2.54mm (100MIL) Zig Zag inline	Through Hole Lead	1-direction
		P G A	PIN GRID ARRAY	C	2.54mm (100MIL)	Through Hole Lead	Package side
		PIGGY BACK	PIGGY BACK	C	2.54mm (100MIL)	Through Hole Lead	2-direction
	Shrink	SDIP	SHRINK DUAL IN-LINE PACKAGE	P	1.778mm (70MIL)	Through Hole Lead	2-direction
		SZIP	SHRINK Zig-Zag IN-LINE PACKAGE	P	1.778mm (70MIL) Zig Zag inline	Through Hole Lead	1-direction
Surface mounted	Standard flat package	Q F P	QUAD FLAT L-LEADED PACKAGE	P	1.0mm 0.8mm 0.65mm	Gull-Wing	4-direction
		S O P	SMALL OUTLINE L-LEADED PACKAGE	P	1.27mm (50MIL)	Gull-Wing	2-direction
	Standard 2-direction chip carrier	S O J	SMALL OUTLINE J-LEADED PACKAGE	P	1.27mm (50MIL)	J-Lead	2-direction
	Shrink flat package	VQFP	VERY SMALL QUAD FLAT PACKAGE	P	0.5mm	Gull-Wing	4-direction
		VSOP	VERY SMALL OUTLINE PACKAGE	P	0.65mm	Gull-Wing	2-direction
	Standard chip carrier	Q F J (PLCC)	QUAD FLAT J-LEADED PACKAGE	P	1.27mm (50MIL)	J-Lead	4-direction
		Q F N (LCC)	QUAD FLAT NON-LEADED PACKAGE	C	1.27mm (50MIL)	Leadless	Package side

* P.....Plastic, C.....Ceramic

Index by Usage

Type	Function	Process	Page
CXK2547P CXK2547L	63,535 word x 16bit, 25/30/35ns SRAM	MIX CMOS	59
CXK2547AP CXK2547AL	10,324 word x 16bit, 25/30/35ns SRAM	MIX CMOS	37
CXK2547BP CXK2547BL	15,384 word x 16bit, 15/20ns SRAM	MIX CMOS	45
CXK2547CP CXK2547CL	10,324 word x 16bit, 25/30/35ns SRAM with CE	MIX CMOS	33
CXK2547DP CXK2547DL	8,324 word x 16bit, 15/20ns SRAM with CE	MIX CMOS	81
CXK2547AP CXK2547AL	8,125 word x 8bit, 20/25/35ns SRAM	FULL CMOS	89
CXK2547BP CXK2547BL	8,125 word x 8bit, 25/30/35ns SRAM	FULL CMOS	78
CXK2547CP CXK2547CL	8,125 word x 8bit, 20/100/120ns SRAM	MIX CMOS	86
CXK2547DP CXK2547DL	8,103 word x 8bit, 25/30/35ns SRAM	FULL CMOS	96
CXK2547BP CXK2547BL	32,144 word x 8bit, 35/45/55ns SRAM	MIX CMOS	108
CXK2547CP CXK2547CL	62,320 word x 8bit, 35/45/55ns SRAM	MIX CMOS	114
CXK2547DP CXK2547DL	22,704 word x 8bit, 15/20/35ns SRAM	MIX CMOS	122
CXK2547BP CXK2547BL	22,728 word x 8bit, 30/35/55ns SRAM	MIX CMOS	129
CXK2547CP CXK2547CL	22,768 word x 8bit, 35/45/55ns SRAM	MIX CMOS	137
CXK2547BP CXK2547BL	32,144 word x 8bit, 70/85/100/120ns SRAM	MIX CMOS	146
CXK2547CP CXK2547CL	22,768 word x 8bit, 70/85/100/120ns SRAM	MIX CMOS	156
CXK2547DP CXK2547DL	12,768 word x 8bit, 70/85/100/120ns SRAM	MIX CMOS	166

Static RAM

1. Index by Usage

1) Static RAM

Type	Function	Process	Page
CXK5164P CXK5164J	65,536 word x 1bit, 25/30/35ns SRAM	MIX CMOS	29
CXK5464AP CXK5464AJ	16,384 word x 4bits, 25/30/35ns SRAM	MIX CMOS	37
CXK5466P CXK5466J	16,384 word x 4bits, 15/20ns SRAM	MIX CMOS	45
CXK5465P CXK5465J	16,384 word x 4bits, 25/30/35ns SRAM with OE	MIX CMOS	53
CXK5467P CXK5467J	16,384 word x 4bits, 15/20ns SRAM with OE	MIX CMOS	61
CXK5863AP CXK5863AJ	8,192 word x 8bits, 20/25/30ns SRAM	FULL CMOS	69
CXK5863P CXK5863M CXK5863J	8,192 word x 8bits, 25/30/35ns SRAM	FULL CMOS	76
CXK5864BP-L/LL CXK5864BSP-L/LL CXK5864BM-L/LL	8,192 word x 8bits, 70/100/120ns SRAM	MIX CMOS	86
CXK5971P CXK5971M CXK5971J	8,192 word x 9bits, 25/30/35ns SRAM	FULL CMOS	96
CXK51256P	262,144 word x 1bit, 35/45/55ns SRAM	MIX CMOS	106
CXK54256P	65,536 word x 4bits, 35/45/55ns SRAM	MIX CMOS	114
CXK58258AP CXK58258AJ	32,768 word x 8bits, 15/20/25ns SRAM	MIX CMOS	122
CXK58258BP-L/LL CXK58258BJ-L/LL CXK58258BM-L/LL	32,768 word x 8bits, 20/25/35ns SRAM	MIX CMOS	129
CXK58258P CXK58258SP	32,768 word x 8bits, 35/45/55ns SRAM	MIX CMOS	137
CXK58257AP-L/LL CXK58257ASP-L/LL CXK58257AM-L/LL	32,768 word x 8bits, 70/85/100/120ns SRAM	MIX CMOS	146
CXK58257AP-LX/LLX CXK58257ASP-LX/LLX CXK58257AM-LX/LLX	32,768 word x 8bits, 70/85/100/120ns SRAM	MIX CMOS	156
CXK58257ATM-L/LL CXK58257AYM-L/LL	32,768 word x 8bits, 70/85/100/120ns SRAM	MIX CMOS	166

1) Static RAM (con't)

Type	Function	Process	Page
CXK58257ATM-LX/LLX CXK58257AYM-LX/LLX	32,768 word x 8bits, 70/85/100/120ns SRAM	MIX CMOS	176
CXK58257P-L/LL CXK58257SP-L/LL CXK58257M-L/LL	32,768 word x 8bits, 70/85/100/120ns SRAM	MIX CMOS	186
CXK58267AP-L/LL CXK58267ASP-L/LL CXK58267AM-L/LL	32,768 word x 8bits, 70/85/100/120ns SRAM 2 CE	MIX CMOS	194
CXK58267ATM-L/LL CXK58267AYM-L/LL	32,768 word x 8bits, 70/85/100/120ns SRAM 2 CE	MIX CMOS	205
CXK59288P CXK59288J	32,768 word x 9bits, 15/20/25ns SRAM	MIX CMOS	216
CXK59290M-L CXK59290TM-L	32,768 word x 9 bits, 70/10/120ns SRAM	MIX CMOS	223
CXK581020SP CXK581020J	131,072 word x 8bits, 35/45/55ns SRAM	MIX CMOS	234
CXK581001P-L/LL CXK581001M-L/LL	131,072 word x 8bits, 70/85ns SRAM	MIX CMOS	243
CXK581000P-L/LL CXK581000M-L/LL	131,072 word x 8bits, 100/120/150ns SRAM	MIX CMOS	252
CXK581000P-LX/LLX CXK581000M-LX/LLX	131,072 word x 8bits, 100/120/150ns SRAM -25°C to +85°C (Extended Temp.)	MIX CMOS	263
CXK581000P-12LB CXK581000M-12LB	131,072 word x8bits, 120ns at V _{CC} =5V 240ns at V _{CC} =3V	MIX CMOS	272
CXK581100TM-L/LL CXK581100YM-L/LL	131,072 words x 8bits, 100/120/150ns SRAM	MIX CMOS	283
CXK581100TM-LX/LLX CXK581100YM-LX/LLX	131,072 words x 8bits, 100/120/150ns SRAM	MIX CMOS	294
CXK581100TM-12LB CXK581100YM-12LB	131,072 word x8bits, 120ns at V _{CC} =5V 240ns at V _{CC} =3V	MIX CMOS	303
CXK541000J	262,144 words x 4bits, 25/30/35ns SRAM	MIX CMOS	314

65,536-word × 1-bit High Speed CMOS Static RAM

Description

CXK5164P/J are 65,536 bits high speed CMOS static RAMs organized as 65,536 words by 1 bit and operate from a single 5V supply.

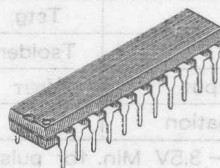
These devices have separate Data input and Data Output pins.

Features

- Fast access time :
CXK5164P/J-25 25ns (Max.)
CXK5164P/J-30 30ns (Max.)
CXK5164P/J-35 35ns (Max.)
- Low power operation : 125mW (Typ.)
- Single + 5V supply : +5V ± 10 %
- Fully static memory...No clock or timing strobe required.
- Equal access and cycle time
- Separate I/O pins
- Three-state output
- Directly TTL compatible : All inputs and outputs.
- High density : 300mil 22 pin plastic DIP
300mil 24 pin plastic SOJ

CXK5164P
24 pin SOJ (Plastic)

CXK5164J
24 pin SOJ (Plastic)



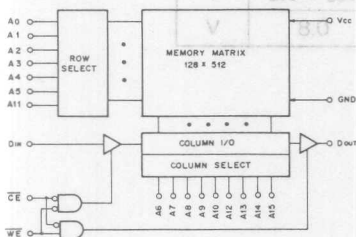
Function

65,536-word × 1-bit static RAM

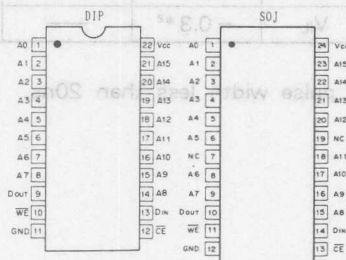
Structure

Silicon gate CMOS IC

Block Diagram



Pin Configuration (Top View)



Pin Description

Symbol	Description
A0 to A15	Address input
Din	Data input
Dout	Data output
CE	Chip enable input
WE	Write enable input
Vcc	+ 5V Power supply
GND	Ground
NC	Non connection

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply voltage	V _{CC}	- 0.5* to + 7.0	V
Input voltage	V _{IN}	- 0.5* to V _{CC} + 0.5	V
Operating temperature	T _{opr}	0 to + 70	°C
Storage temperature	T _{stg}	- 55 to + 150	°C
Soldering temperature	T _{solder}	260 • 10	°C • sec
Voltage applied to output	V _{OUT}	- 0.5* to V _{CC} + 0.5	V
Allowable power dissipation	P _D	1.0	W

*Note) V_{CC}, V_{IN}, V_{OUT} = - 3.5V Min. for pulse width less than 20ns.

Truth Table

$\overline{\text{CE}}$	$\overline{\text{WE}}$	Mode	Dout	V _{CC} Current
H	X	Not selected	High Z	I _{SB1} , I _{SB2}
L	H	Read	Data out	I _{CC1} , I _{CC2}
L	L	Write	High Z	I _{CC1} , I _{CC2}

X: "H" or "L"

DC Recommended Operating Conditions

(T_a = 0 to + 70°C, GND = 0V)

Item	Symbol	Min.	Typ.* ¹	Max.	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Input high voltage	V _{IH}	2.2	—	V _{CC} + 0.3	V
Input low voltage	V _{IL}	- 0.3* ²	—	0.8	V

Note) *1. V_{CC} = 25°C

*2. V_{IL} = - 3.0V Min. for pulse width less than 20ns.

Electrical Characteristics

DC and operating characteristics

(V_{CC} = 5V ± 10 %, GND = 0V, T_a = 0 to +70 °C)

Item	Symbol	Test conditions	- 25/30/35			Unit
			Min.	Typ.	Max.	
Input leakage current	I _{LI}	V _{IN} = GND to V _{CC}	- 1	—	1	μA
Output leakage current	I _{LO}	$\overline{CE} = V_{IH}$ or $WE = V_{IL}$ V _{I/O} = GND to V _{CC}	- 1	—	1	μA
Operating power supply current	I _{CC1}	$\overline{CE} = V_{IL}$, I _{OUT} = 0mA V _{IN} = V _{IH} /V _{IL}	—	25	45	mA
Average operating current	I _{CC2}	Cycle = Min, Duty = 100 % I _{OUT} = 0mA	—	60	90	mA
Standby current	I _{SB1}	$\overline{CE} \geq V_{CC} - 0.2V$, V _{IN} $\geq V_{CC} - 0.2V$ or V _{IN} $\leq 0.2V$	—	—	1	mA
	I _{SB2}	$\overline{CE} = V_{IH}$	—	15	30	mA
Output high voltage	V _{OH}	I _{OH} = - 4.0mA	2.4	—	—	V
Output low voltage	V _{OL}	I _{OL} = 8.0mA	—	—	0.4	V

*Note) V_{CC} = 5.0V, T_a = 25 °C

I/O capacitance

(T_a = 25 °C, f = 1MHz)

Item	Symbol	Test conditions	Min.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} = 0V	—	7	pF
Output capacitance	C _{OUT}	V _{OUT} = 0V	—	7	pF

Note) This parameter is sampled and is not 100 % tested.

AC characteristics

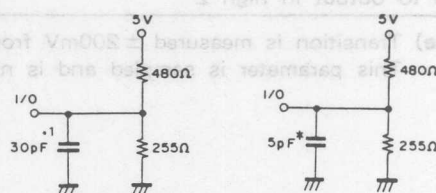
● AC test conditions

(V_{CC} = 5V ± 10 %, T_a = 0 to +70 °C)

Item	Conditions
Input pulse high level	V _{IH} = 3.0V
Input pulse low level	V _{IL} = 0V
Input rise time	t _r = 5ns
Input fall time	t _f = 5ns
Input and output timing reference level	1.5V
Output load	Fig. 1

Output Load (1)

Output Load (2)*2



*1. Including scope and jig

*2. For t_{LZ}, t_{HZ}, t_{OW}, t_{WHZ}

Fig. 1

● Read cycle

Item	Symbol	- 25		- 30		- 35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t _{RC}	25	—	30	—	35	—	ns
Address access time	t _{AA}	—	25	—	30	—	35	ns
Chip enable access time (CE)	t _{CO}	—	25	—	30	—	35	ns
Output hold from address change	t _{OH}	5	—	5	—	5	—	ns
Chip enable to output in low Z (CE)	t _{LZ} *	5	—	5	—	5	—	ns
Chip disable to output in high Z	t _{HZ} *	0	10	0	15	0	15	ns
Chip enable to power up time	t _{PU}	0	—	0	—	0	—	ns
Chip disable to power down time	t _{PD}	—	20	—	25	—	25	ns

* **Note)** Transition is measured $\pm 200\text{mV}$ from steady voltage with specified loading in Fig. 1.
This parameter is sampled and is not 100% tested.

● Write cycle

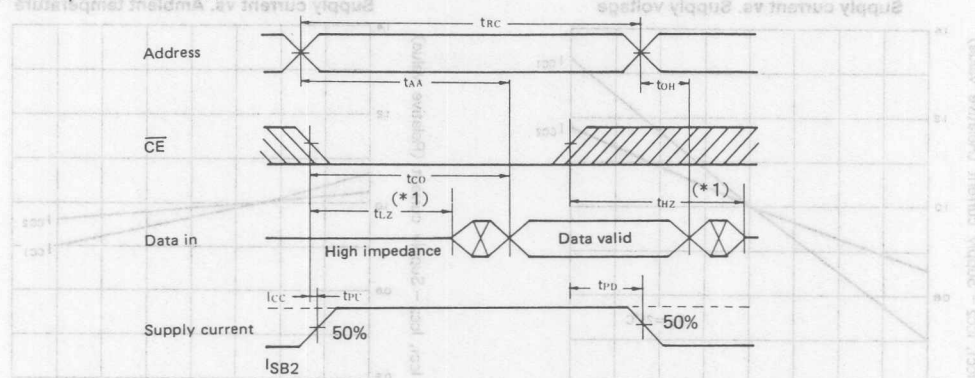
Item	Symbol	- 25		- 30		- 35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t _{WC}	25	—	30	—	35	—	ns
Address valid to end of write	t _{AW}	20	—	25	—	30	—	ns
Chip enable to end of write	t _{CW}	20	—	25	—	30	—	ns
Data to write time overlap	t _{DW}	12	—	15	—	15	—	ns
Data hold from write time	t _{DH}	0	—	0	—	0	—	ns
Write pulse width	t _{WP}	20	—	25	—	30	—	ns
Address setup time	t _{AS}	0	—	0	—	0	—	ns
Write recovery time	t _{WR}	0	—	0	—	0	—	ns
Output active from end of write	t _{OW} *	5	—	5	—	5	—	ns
Write to output in high Z	t _{WHZ} *	0	10	0	10	0	15	ns

* **Note)** Transition is measured $\pm 200\text{mV}$ from steady voltage with specified loading in Fig. 1.
This parameter is sampled and is not 100% tested.

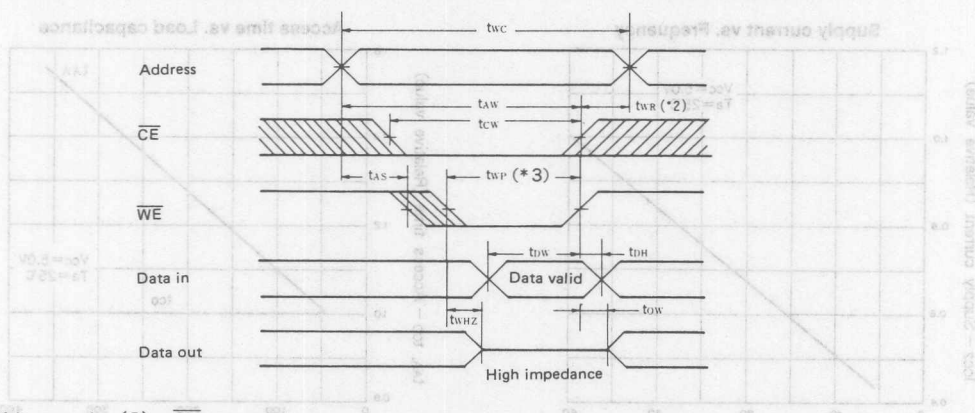
Output load	Fig. 1
Input and output timing	1.5V
Input rise time	t _r = 5ns
Input fall time	t _f = 5ns
Input pulse low level	V _{IL} = 0.8V
Input pulse high level	V _{IH} = 2.0V

Timing Waveform

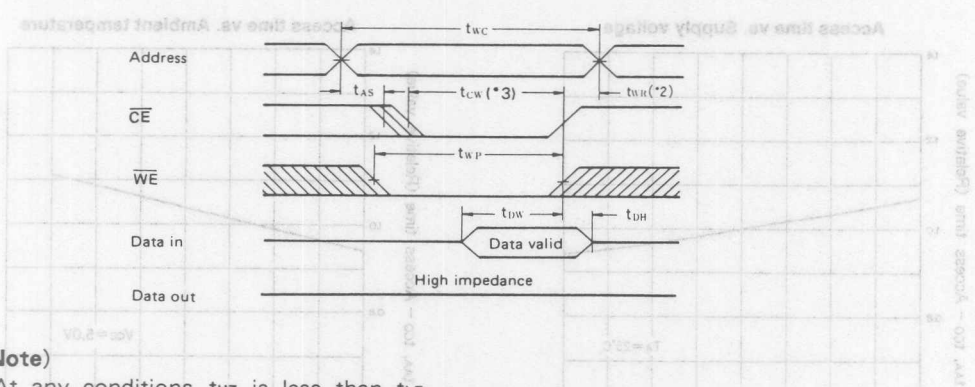
- Read cycle : $\overline{WE} = V_{IH}$



- Write cycle (1) : $\overline{WE}$ control



- Write cycle (2) : $\overline{CE}$ control

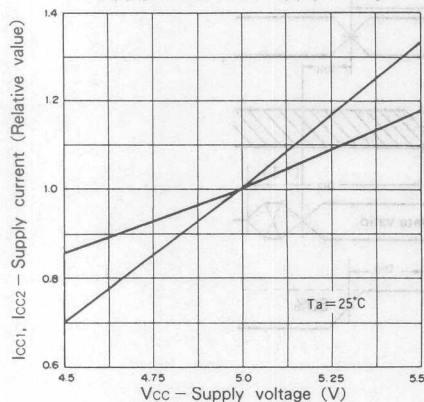


* Note

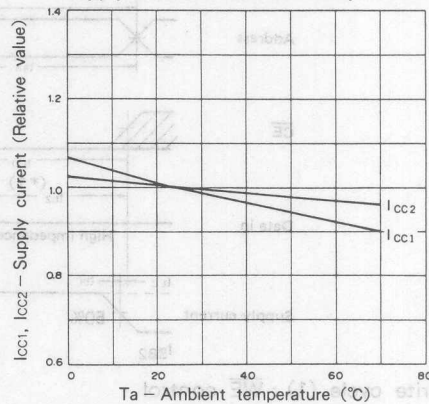
1. At any conditions, t_{hz} is less than t_{tz} .
2. t_{wr} is measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high to the end of write cycle.
3. A write occurs during the low overlap of $\overline{CE}$ and $\overline{WE}$.

Example of Representative Characteristics

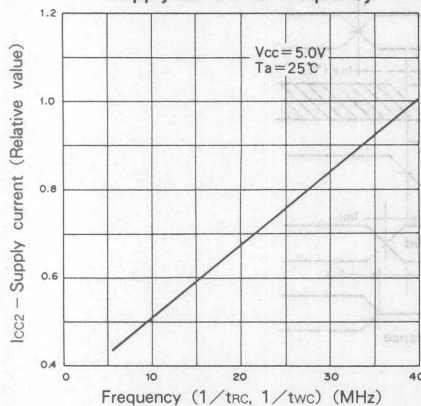
Supply current vs. Supply voltage



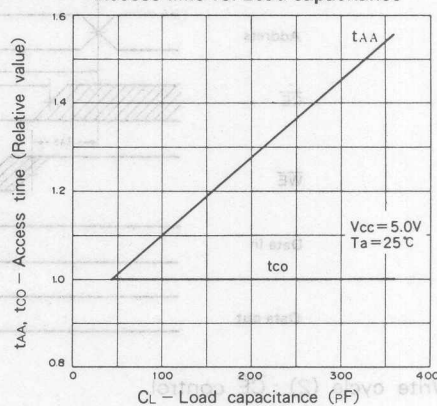
Supply current vs. Ambient temperature



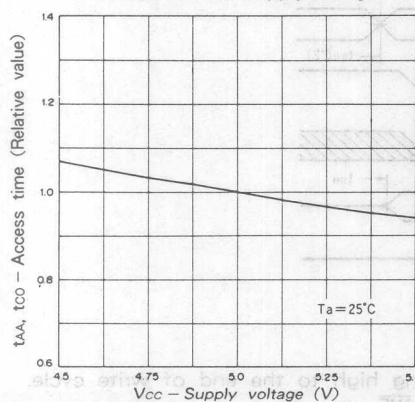
Supply current vs. Frequency



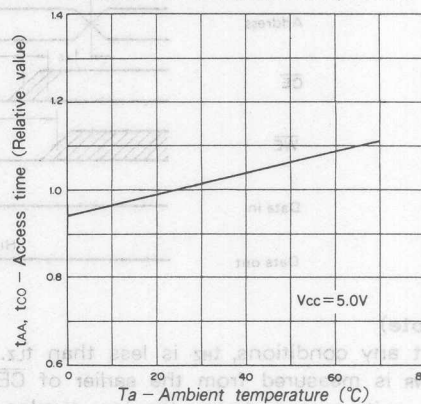
Access time vs. Load capacitance



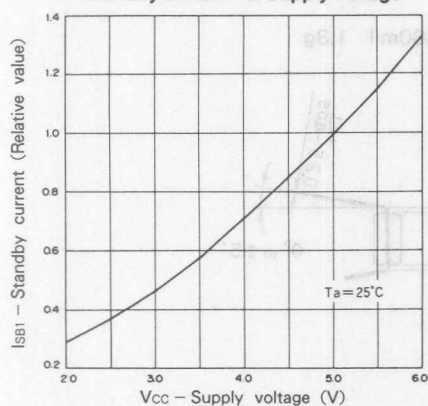
Access time vs. Supply voltage



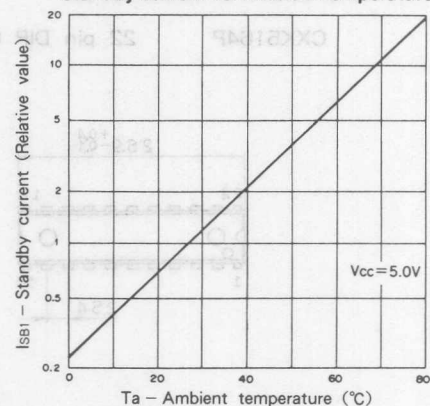
Access time vs. Ambient temperature



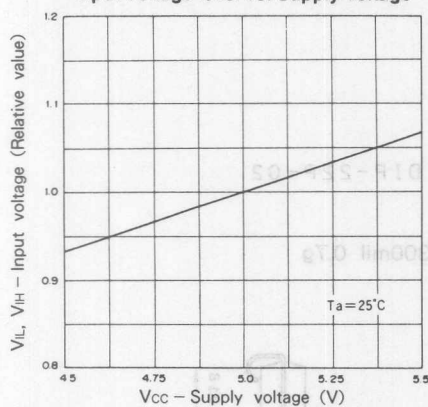
Standby current vs. Supply voltage



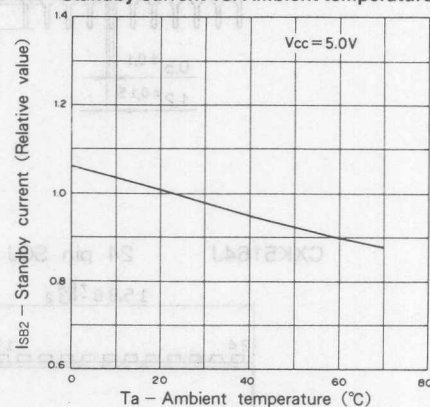
Standby current vs. Ambient temperature



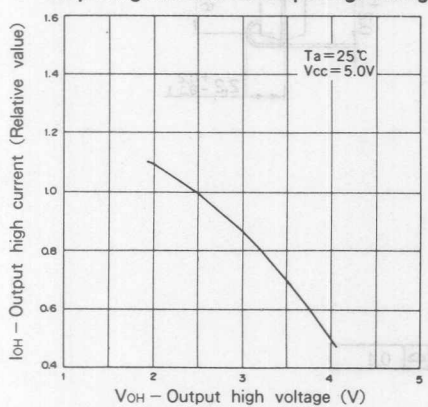
Input voltage level vs. Supply voltage



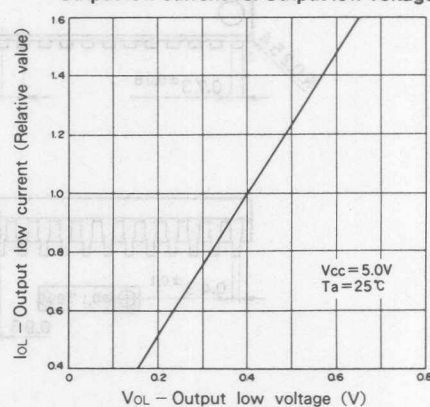
Standby current vs. Ambient temperature



Output high current vs. Output high voltage

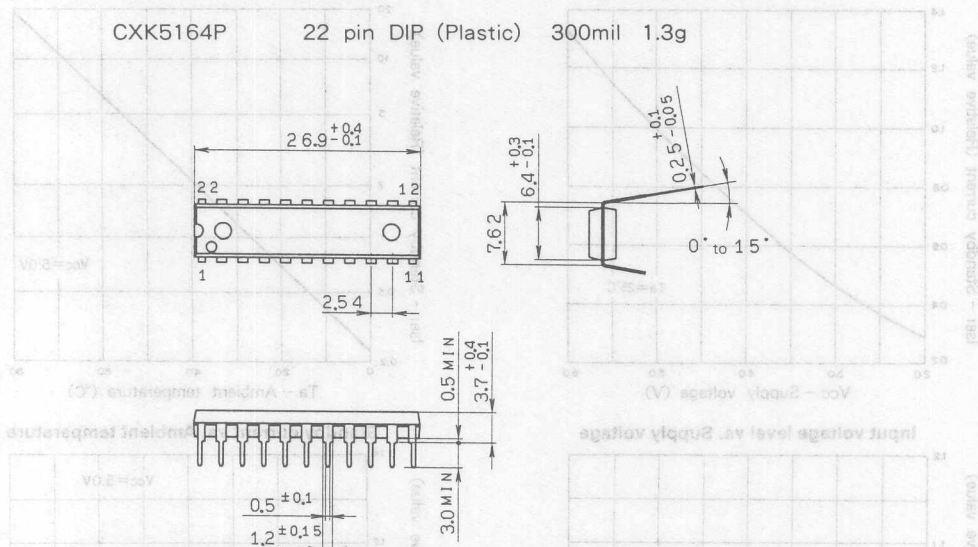


Output low current vs. Output low voltage



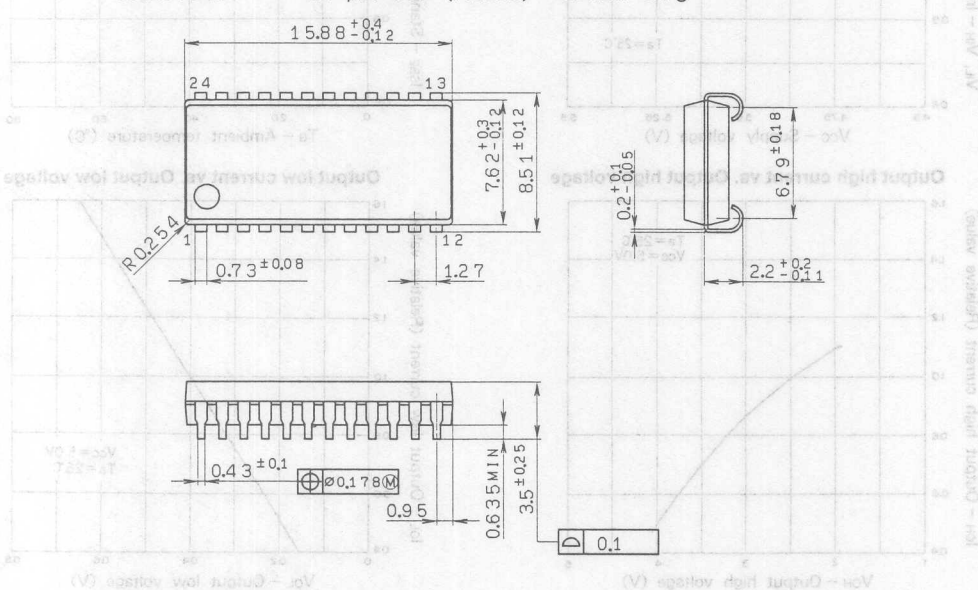
Package Outline Unit : mm

CXK5164P 22 pin DIP (Plastic) 300mil 1.3g



DIP-22P-02

CXK5164J 24 pin SOJ (Plastic) 300mil 0.7g



SOJ-24P-01

16,384-word × 4-bit High Speed CMOS Static RAM

Description

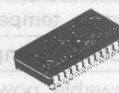
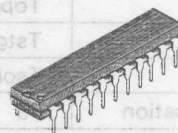
CXK5464AP/AJ are 65,536 bits high speed CMOS static RAMs organized as 16,384 words by 4 bits and operate from a single 5V supply.

Features

- Fast access time :
CXK5464AP/AJ-25 25ns (Max.)
CXK5464AP/AJ-30 30ns (Max.)
CXK5464AP/AJ-35 35ns (Max.)
- Low power operation : 125mW (Typ.)
- Single +5V supply : +5V ± 10 %
- Fully static memory...No clock or timing strobe required.
- Equal access and cycle time.
- Common data input and output : Three-state output
- Directly TTL compatible : All inputs and outputs.
- High density : 300mil 22 pin plastic DIP
300mil 24 pin plastic SOJ

CXK5464AP
22 pin DIP (Plastic)

CXK5464AJ
24 pin SOJ (Plastic)



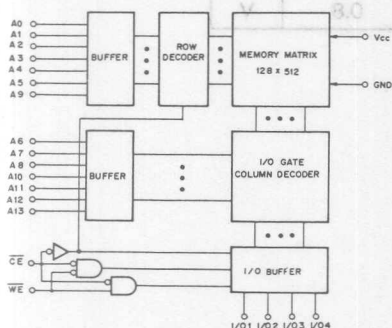
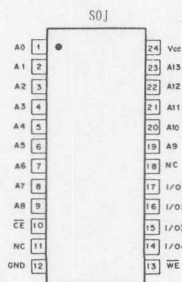
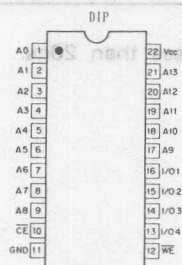
Function

16,384-word × 4-bit static RAM

Structure

Silicon gate CMOS IC

Block Diagram

Pin Configuration
(Top view)

Pin Description

Symbol	Description
A0 to A13	Address input
I/O1 to I/O4	Data input output
CE	Chip enable input
WE	Write enable input
Vcc	+5V Power supply
GND	Ground
NC	Non connection

Absolute Maximum Ratings (Ta = 25°C, GND = 0V)

Item	Symbol	Rating	Unit
Supply voltage	V _{CC}	-0.5* to +7.0	V
Input voltage	V _{IN}	-0.5* to V _{CC} + 0.5	V
Input and output voltage	V _{I/O}	-0.5* to V _{CC} + 0.5	V
Operating temperature	T _{opr}	0 to +70	°C
Storage temperature	T _{stg}	-55 to +150	°C
Soldering temperature	T _{solder}	260 • 10	°C • sec
Allowable power dissipation	P _D	1.0	W

* V_{CC}, V_{IN}, V_{I/O} = -3.5V Min. for pulse width less than 20ns.

Truth Table

$\overline{\text{CE}}$	$\overline{\text{WE}}$	Mode	I/O1 to I/O4	V _{CC} Current
H	X	Not selected	High Z	I _{SB1} , I _{SB2}
L	H	Read	Data out	I _{CC1} , I _{CC2}
L	L	Write	Data in	I _{CC1} , I _{CC2}

X: "H" or "L"

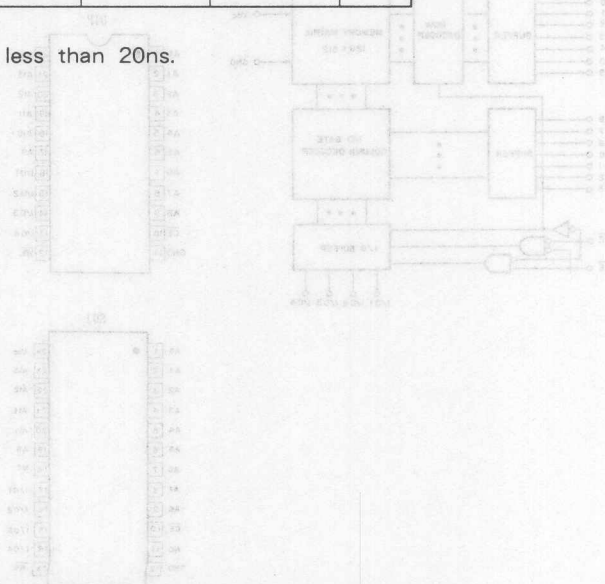
DC Recommended Operating Conditions (Ta = 0 to +70°C, GND = 0V)

Item	Symbol	Min.	Typ.*1	Max.	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Input high voltage	V _{IH}	2.2	—	V _{CC} + 0.3	V
Input low voltage	V _{IL}	-0.3*2	—	0.8	V

*1. V_{CC} = 5V, Ta = 25°C

*2. V_{IL} = -3.0V Min. for pulse width less than 20ns.

NC	Non connection
GND	Ground
V _{CC}	+5V Power supply
$\overline{\text{WE}}$	Write enable input
$\overline{\text{CE}}$	Chip enable input
I/O1 to I/O4	Data input/output



Electrical Characteristics

● DC and operating characteristics (Vcc = 5V ± 10%, GND = 0V, Ta = 0 to +70°C)

Item	Symbol	Test conditions	- 25/30/35			Unit
			Min.	Typ.*	Max.	
Input leak current	ILI	VIN = GND to Vcc	-1	—	1	μA
Output leak current	ILO	CE = VIH or WE = VIL VI/O = GND to Vcc	-1	—	1	μA
Operating supply current	Icc1	CE = VIL, IOUT = 0mA VIN = VIH/VIL	—	25	45	mA
Average operating current	Icc2	Cycle = Min., Duty = 100 % IOUT = 0mA	—	60	90	mA
Standby current	ISB1	CE ≥ Vcc - 0.2V, VIN ≥ Vcc - 0.2V or VIN ≤ 0.2V	—	—	1	mA
	ISB2	CE = VIH	—	15	30	mA
Output high voltage	VOH	Ioh = -4.0mA	2.4	—	—	V
Output low voltage	VOL	IOL = 8.0mA	—	—	0.4	V

* Vcc = 5.0V, Ta = 25°C

I/O capacitance

(Ta = 25°C, f = 1MHz)

Item	Symbol	Test conditions	Min.	Max.	Unit
Input capacitance	CIN	VIN = 0V	—	7	pF
Input/Output capacitance	CI/O	VI/O = 0V	—	7	pF

Note) This parameter is sampled and is not 100% tested.

AC characteristics

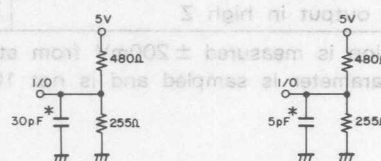
● AC test conditions

(Vcc = 5V ± 10%, Ta = 0 to +70°C)

Item	Conditions
Input pulse high level	VIH = 3.0V
Input pulse low level	VIL = 0V
Input rise time	tr = 5ns
Input fall time	tf = 5ns
Input and output reference level	1.5V
Output load conditions	Fig. 1

Output Load (1)

Output Load (2)**



* including scope and jig

** for tLZ, tHZ, tOW, tWHZ

Fig. 1

● Read cycle

Item	Symbol	- 25		- 30		- 35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t _{RC}	25	—	30	—	35	—	ns
Address access time	t _{AA}	—	25	—	30	—	35	ns
Chip enable access time (CE)	t _{CO}	—	25	—	30	—	35	ns
Output hold from address change	t _{OH}	5	—	5	—	5	—	ns
Chip enable to output in low Z (CE)	t _{LZ} *	5	—	5	—	5	—	ns
Chip disable to output in high Z	t _{HZ} *	0	10	0	15	0	15	ns
Chip enable to power up time	t _{PU}	0	—	0	—	0	—	ns
Chip enable to power down time	t _{PD}	—	20	—	25	—	25	ns

* Transition is measured $\pm 200\text{mV}$ from steady voltage with specified loading in Fig. 1.

This parameter is sampled and is not 100% tested.

● Write cycle

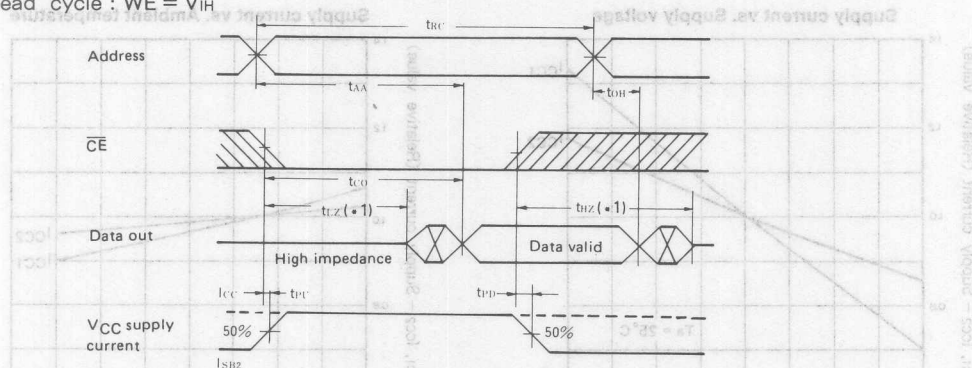
Item	Symbol	- 25		- 30		- 35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t _{WC}	25	—	30	—	35	—	ns
Address valid to end of write	t _{AW}	20	—	25	—	30	—	ns
Chip enable to end of write	t _{CW}	20	—	25	—	30	—	ns
Data to write time overlap	t _{DW}	12	—	15	—	15	—	ns
Data hold from write time	t _{DH}	0	—	0	—	0	—	ns
Write pulse width	t _{WP}	20	—	25	—	30	—	ns
Address setup time	t _{AS}	0	—	0	—	0	—	ns
Write recovery time	t _{WR}	0	—	0	—	0	—	ns
Output active from end of write	t _{OW} *	5	—	5	—	5	—	ns
Write to output in high Z	t _{WHZ} *	0	10	0	10	0	15	ns

* Transition is measured $\pm 200\text{mV}$ from steady voltage with specified loading in Fig. 1.

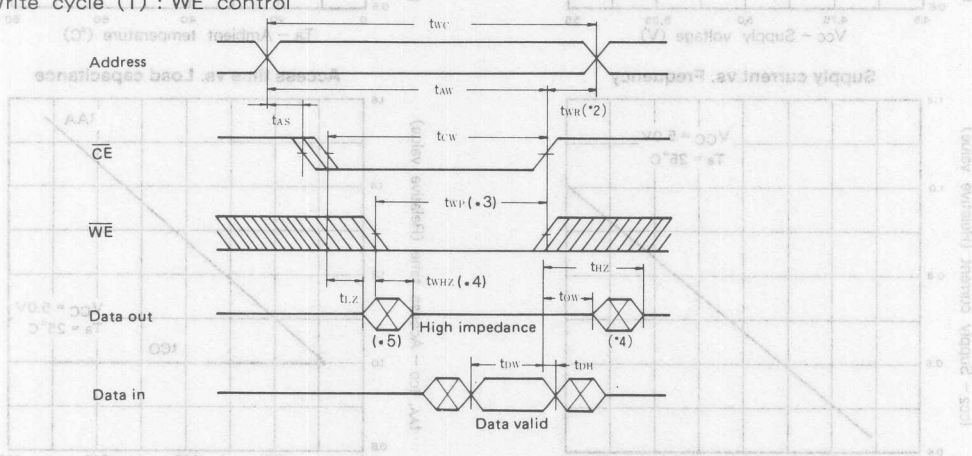
This parameter is sampled and is not 100% tested.

Timing Waveform

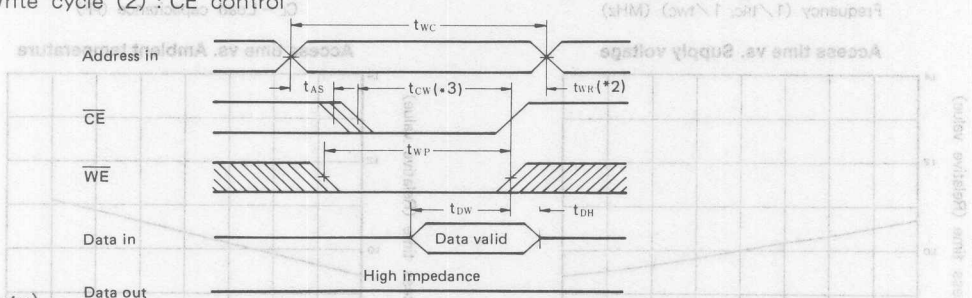
- Read cycle : $\overline{WE} = V_{IH}$



- Write cycle (1) : $\overline{WE}$ control



- Write cycle (2) : $\overline{CE}$ control

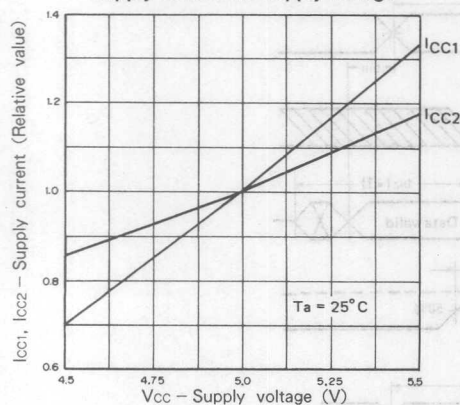


* Note)

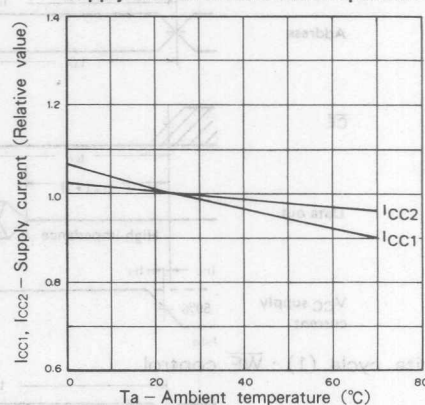
1. At any conditions, t_{DZ} is less than t_{DZ} .
2. t_{WR} is measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high to the end of write cycle.
3. A write occurs during the low overlap of $\overline{CE}$ and $\overline{WE}$.
4. If $\overline{CE}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, output remains in a high impedance state.
5. During this period, I/O pins are in the output state so that the input signals of opposite phase to the output must not be applied.

Example of Representative Characteristics

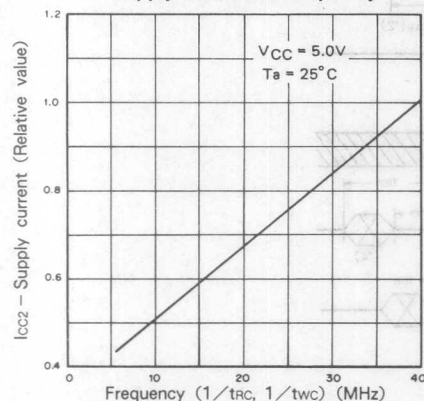
Supply current vs. Supply voltage



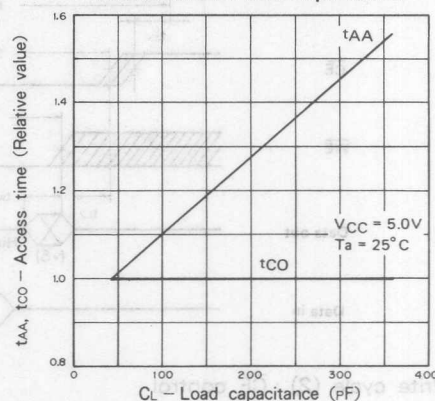
Supply current vs. Ambient temperature



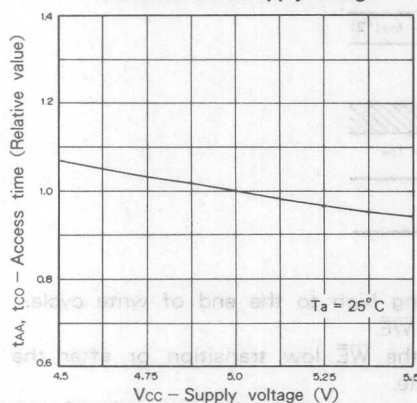
Supply current vs. Frequency



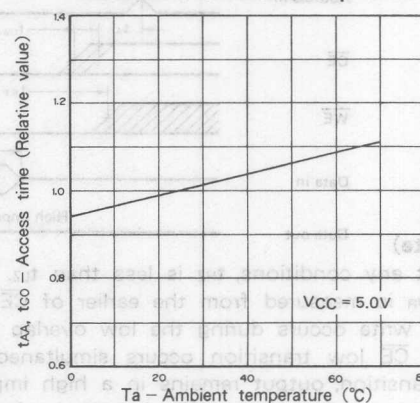
Access time vs. Load capacitance



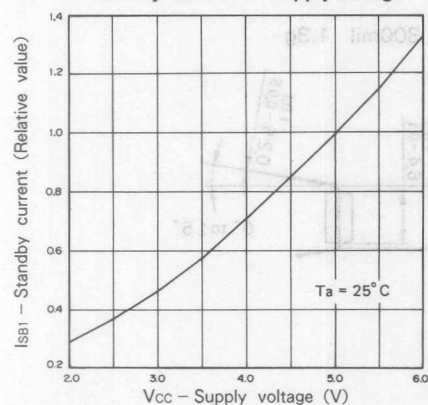
Access time vs. Supply voltage



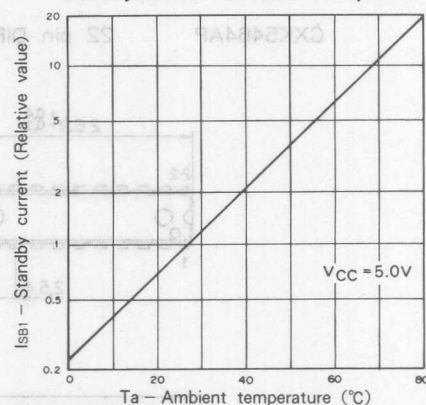
Access time vs. Ambient temperature



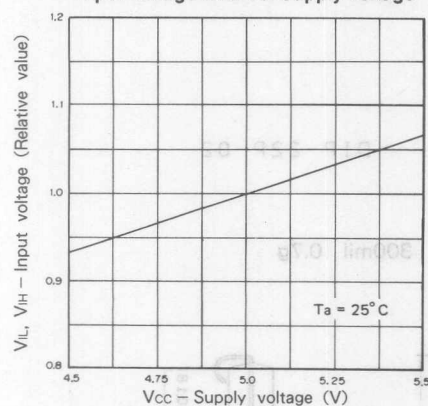
Standby current vs. Supply voltage



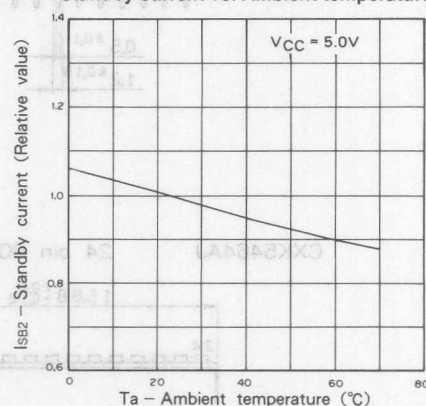
Standby current vs. Ambient temperature



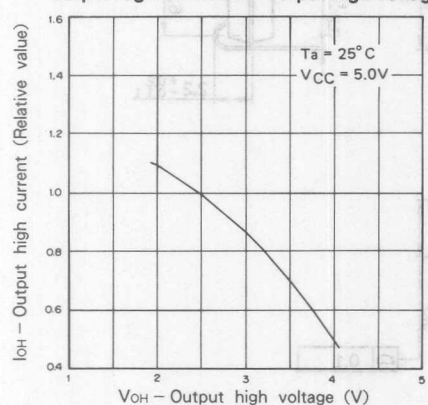
Input voltage level vs. Supply voltage



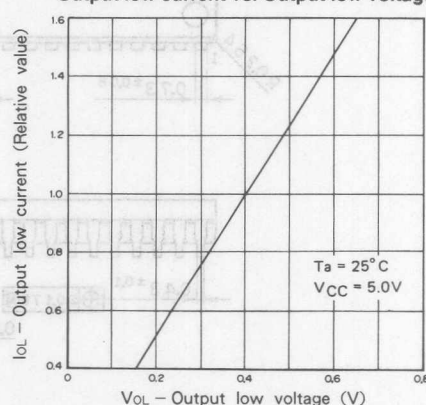
Standby current vs. Ambient temperature



Output high current vs. Output high voltage



Output low current vs. Output low voltage

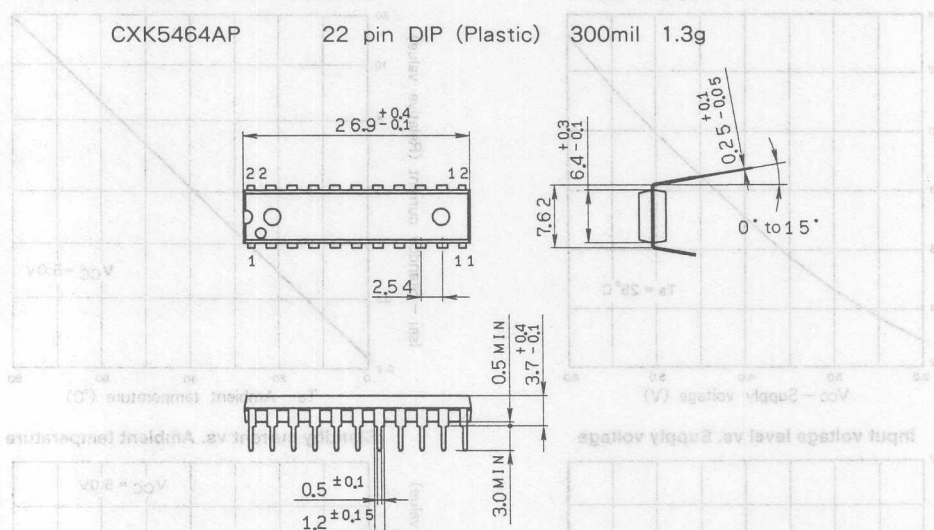


Package Outline Unit : mm

Unit : mm

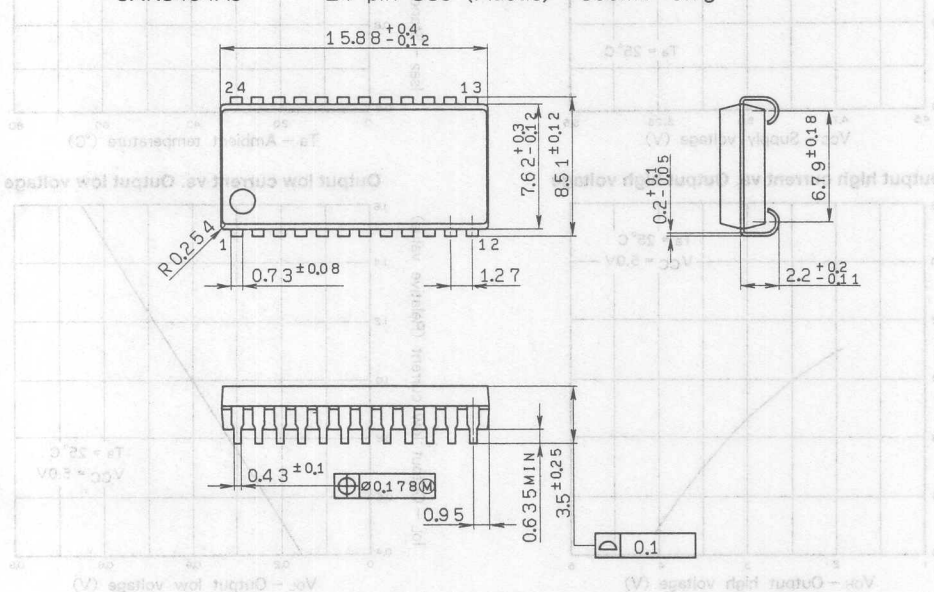
22 pin DIP (Plastic)

300mil	1.3g
--------	------



24 pin SOJ (Plastic)

300mil	0.7g
--------	------



SOJ-24P-01

16,384 word × 4-bit High Speed CMOS Static RAM

Description

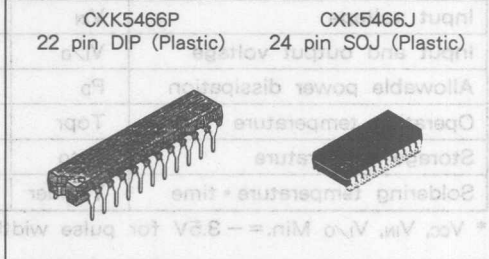
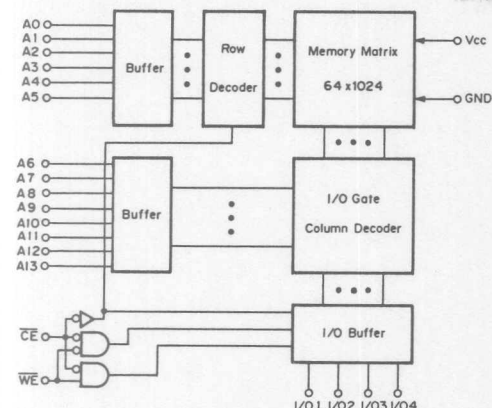
CXK5466P/J is a high speed CMOS static RAM with TTL compatible I/O organized as 16,384 words × 4 bits.

This IC operating on a single 5V supply turns to power down mode at no select time by means of chip enable signal.

Features

- Fast access time :
CXK5466P/J-15 15ns (Max.)
CXK5466P/J-20 20ns (Max.)
- Low power consumption : 150mW (Typ.)
During operation
- Single +5V supply : $+5V \pm 10\%$
- Fully static memory
...No clock or timing strobe required
- Equal access and cycle time
- Common data input and output :
three-state output
- Directly TTL compatible :
All inputs and outputs
- Compatible with various types of packages
- High density : 300 mil 22 pin plastic DIP
300 mil 24 pin plastic SOJ

Block Diagram



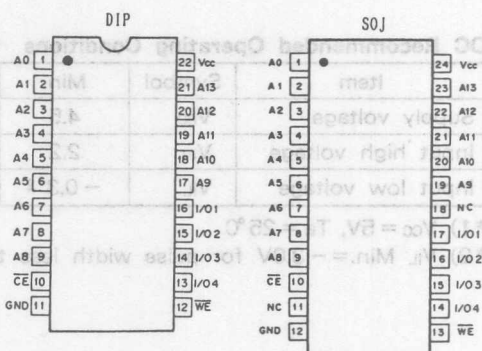
Functions

16,384 word × 4-bit static RAM

Structure

Silicon gate CMOS IC

Pin Configuration (Top View)



Pin Description

Symbol	Description
A0 to A13	Address input
I/O1 to I/O4	Data input/output
CE	Chip enable input
WE	Write enable input
Vcc	+5V power supply
GND	Ground
NC	No connection

Absolute Maximum Ratings ($T_a = 25^\circ\text{C}$, GND = 0V)

Item	Symbol	Ratings	Unit
Supply voltage	V_{CC}	- 0.5 * to + 7.0	V
Input voltage	V_{IN}	- 0.5 * to $V_{CC} + 0.5$	V
Input and output voltage	$V_{I/O}$	- 0.5 * to $V_{CC} + 0.5$	V
Allowable power dissipation	P_D	1.0	W
Operating temperature	T_{opr}	0 to + 70	$^\circ\text{C}$
Storage temperature	T_{stg}	- 55 to + 150	$^\circ\text{C}$
Soldering temperature * time	T_{solder}	260 * 10	$^\circ\text{C} \cdot \text{sec}$

* V_{CC} , V_{IN} , $V_{I/O}$ Min. = - 3.5V for pulse width less than 20ns.

Truth Table

$\overline{CE}$	$\overline{WE}$	Mode	I/O1 to I/O4	V_{CC} current
H	X	Not selected	High Z	I_{SB1} , I_{SB2}
L	H	Read	Data output	I_{CC1} , I_{CC2}
L	L	Write	Data input	I_{CC1} , I_{CC2}

X : "H" or "L"

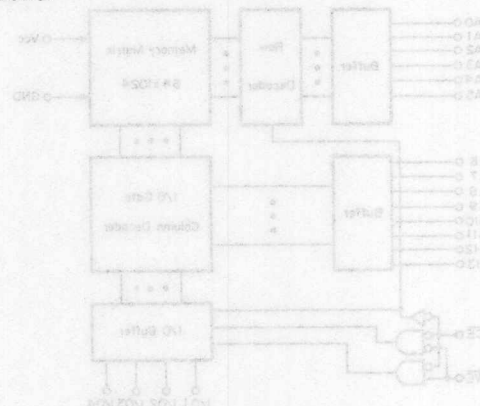
DC Recommended Operating Conditions ($T_a = 0$ to + 70 $^\circ\text{C}$, GND = 0V)

Item	Symbol	Min.	Typ.*1	Max.	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input high voltage	V_{IH}	2.2	—	$V_{CC} + 0.3$	V
Input low voltage	V_{IL}	- 0.3*2	—	0.8	V

*1) $V_{CC} = 5V$, $T_a = 25^\circ\text{C}$

*2) V_{IL} Min. = - 3.0V for pulse width less than 20ns.

Description	Symbol
Address input	A0 to A13
Data input/output	I/O1 to I/O4
Chip enable input	$\overline{CE}$
Write enable input	$\overline{WE}$
+ 5V power supply	V_{CC}
Ground	GND
No connection	NC



DC Electrical Characteristics

• DC and operating characteristics

(V_{CC} = 5V ± 10 %, GND = 0V, T_a = 0 to +70 °C)

Item	Symbol	Test Conditions	Min.	Typ.*	Max.	Unit
Input leak current	I _{LI}	V _{IN} = GND to V _{CC}	-1	—	1	μA
Output leak current	I _{LO}	CE = V _{IH} or WE = V _{IL} V _{I/O} = GND to V _{CC}	-1	—	1	μA
Operating power supply current	I _{CC1}	CE = V _{IL} , I _{OUT} = 0mA, V _{IN} = V _{IH} or V _{IL}	—	30	55	mA
Average operating current	I _{CC2}	Cycle = Min., Duty = 100 %, I _{OUT} = 0mA	-15	95	150	mA
			-20	90	140	mA
Standby current	I _{SB1}	CE ≥ V _{CC} - 0.2V, V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V	—	—	1	mA
	I _{SB2}	CE = V _{IH} , V _{IN} = V _{IH} /V _{IL} , Cycle = Min.	—	—	85	mA
Output high voltage	V _{OH}	I _{OH} = -4.0mA	2.4	—	—	V
Output low voltage	V _{OL}	I _{OL} = 8.0mA	—	—	0.4	V

* V_{CC} = 5.0V, T_a = 25 °C

I/O capacitance

(T_a = 25 °C, f = 1MHz)

Item	Symbol	Test Conditions	Min.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} = 0V	—	7	pF
Input/output capacitance	C _{I/O}	V _{I/O} = 0V	—	7	pF

Note) This parameter is sampled and is not 100 % tested.

AC characteristics

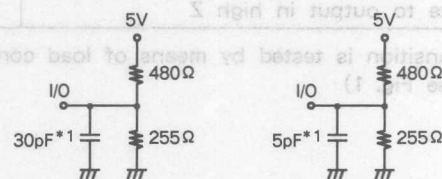
• AC test conditions

(V_{CC} = 5V ± 10 %, T_a = 0 to +70 °C)

Item	Conditions
Input pulse high level	V _{IH} = 3.0V
Input pulse low level	V _{IL} = 0V
Input rise time	t _r = 5ns
Input fall time	t _f = 5ns
Input and output reference level	1.5V
Output load conditions	Fig. 1

Output Load (1)

Output Load (2)*2



*1 including scope and jig capacitance

*2 for t_{LZ}, t_{HZ}, t_{OW}, t_{WHZ}

Fig. 1

• Read cycle

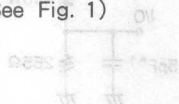
Item	Symbol	- 15		- 20		Unit
		Min.	Max.	Min.	Max.	
Read cycle time	t _{RC}	15	—	20	—	ns
Address access time	t _{AA}	—	15	—	20	ns
Chip enable access time (CE)	t _{CO}	—	15	—	20	ns
Output hold from address change	t _{OH}	3	—	3	—	ns
Chip enable to output in low Z (CE)	t _{LZ} *	2	—	3	—	ns
Chip disable to output in high Z	t _{HZ} *	0	6	0	8	ns
Chip enable to power up time	t _{PU}	0	—	0	—	ns
Chip disable to power down time	t _{PD}	—	15	—	20	ns

* Transition is tested by means of load conditions (2), from stationary condition at $\pm 200\text{mV}$ (See Fig. 1)

• Write cycle

Item	Symbol	- 15		- 20		Unit
		Min.	Max.	Min.	Max.	
Write cycle time	t _{WC}	15	—	20	—	ns
Address valid to end of write	t _{AW}	13	—	18	—	ns
Chip enable to end of write	t _{CW}	13	—	18	—	ns
Data to write time overlap	t _{DW}	8	—	11	—	ns
Data hold from write time	t _{DH}	0	—	0	—	ns
Write pulse width	t _{WP}	13	—	18	—	ns
Address setup time	t _{AS}	0	—	0	—	ns
Write recovery time	t _{WR}	0	—	0	—	ns
Output active from end of write	t _{OW} *	2	—	3	—	ns
Write to output in high Z	t _{WHZ} *	0	5	0	7	ns

* Transition is tested by means of load conditions (2), from stationary condition at $\pm 200\text{mV}$ (See Fig. 1)

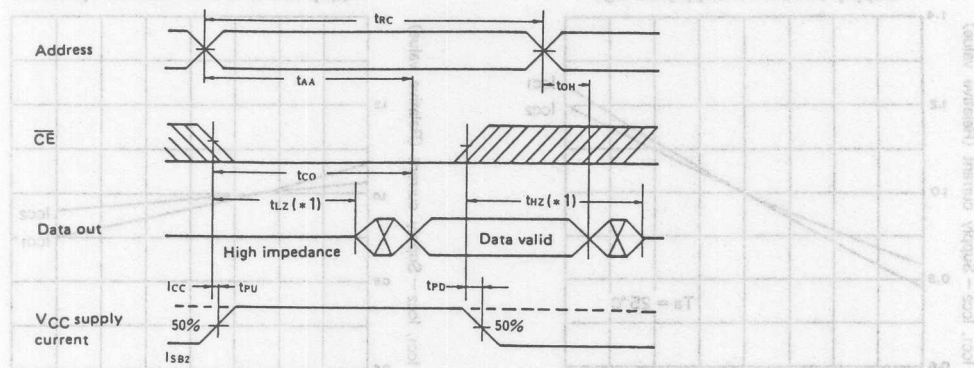


* 1 including scope and jig capacitance
* 2 for t_{LZ}, t_{HZ}, t_{OW}, t_{WHZ}

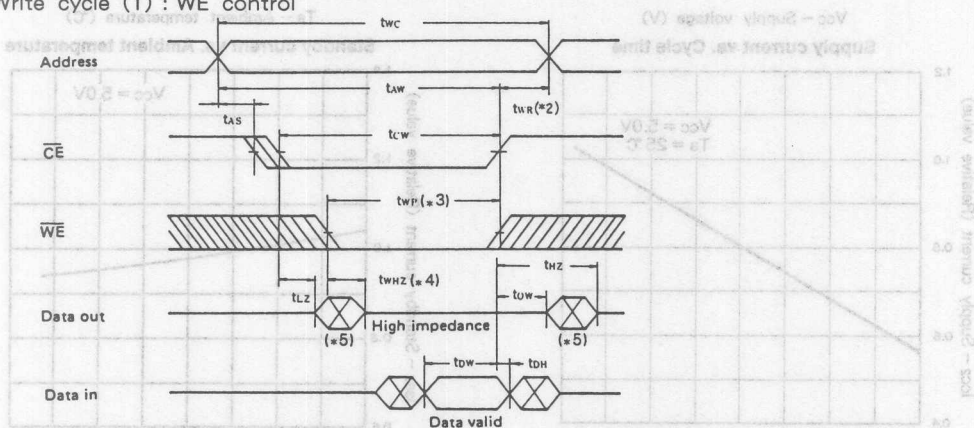
Fig. 1

Timing Waveform

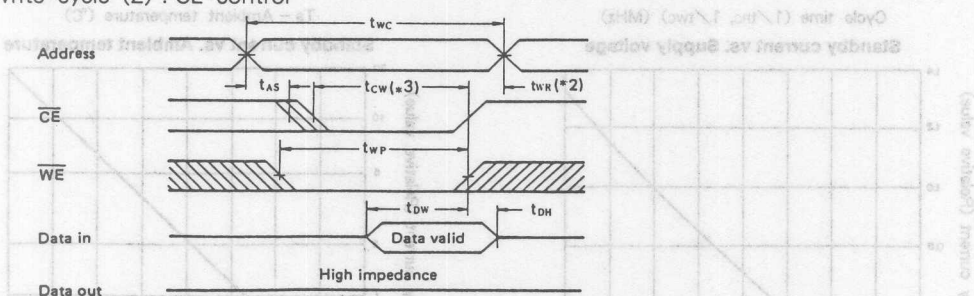
- Read cycle : $\overline{WE} = V_{IH}$



- Write cycle (1) : $\overline{WE}$ control



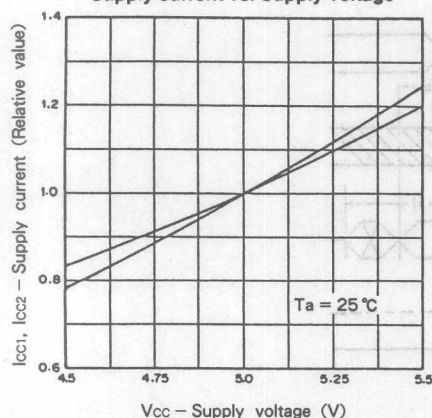
- Write cycle (2) : $\overline{CE}$ control



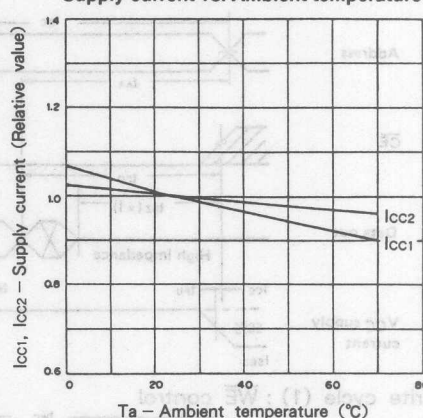
- *1) Whatever the conditions, t_{HZ} is smaller than t_{LZ} .
- *2) t_{WR} is tested from either $\overline{CE}$ or $\overline{WE}$ rise, whichever comes earlier, until the end of write cycle.
- *3) Write is performed when both $\overline{CE}$ and $\overline{WE}$ are in the low overlap.
- *4) When $\overline{WE}$ fall is performed simultaneously with $\overline{CE}$ fall, or before, output is kept to high impedance.
- *5) While I/O pins are in output state, do not apply data input signals with a phase opposite to that of the output.

Example of Representative Characteristics

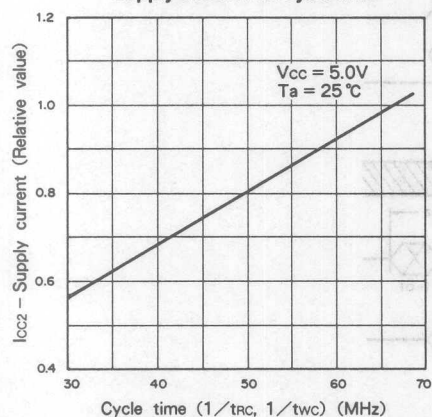
Supply current vs. Supply voltage



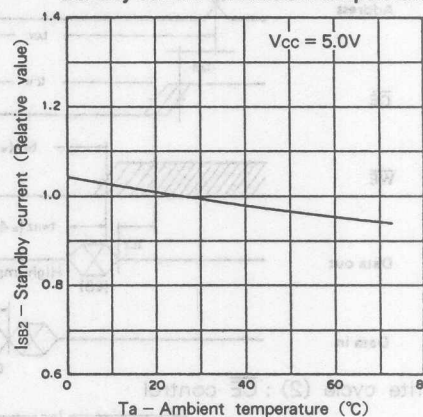
Supply current vs. Ambient temperature



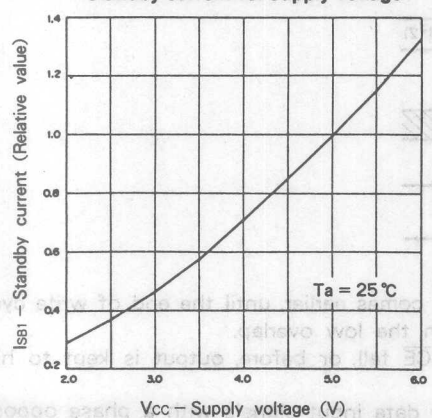
Supply current vs. Cycle time



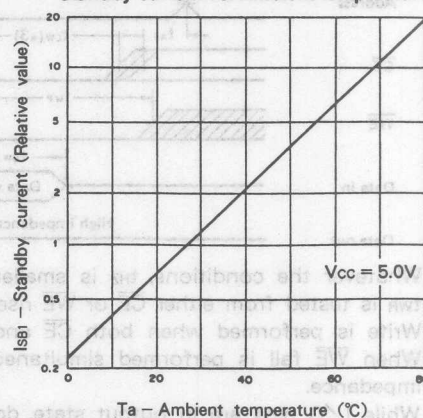
Standby current vs. Ambient temperature



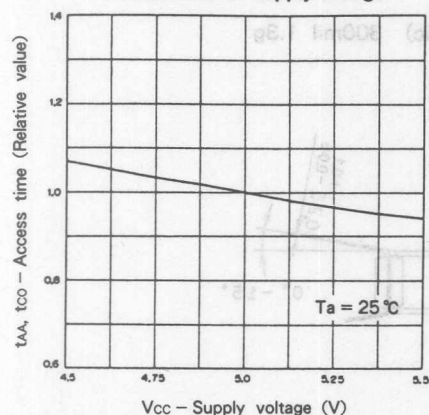
Standby current vs. Supply voltage



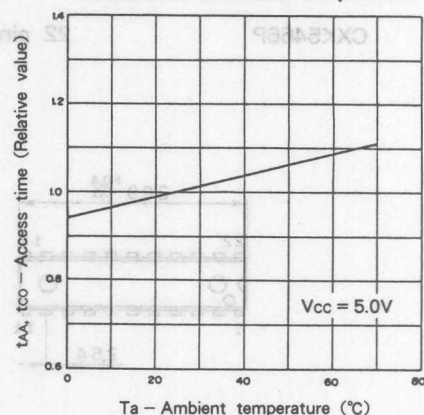
Standby current vs. Ambient temperature



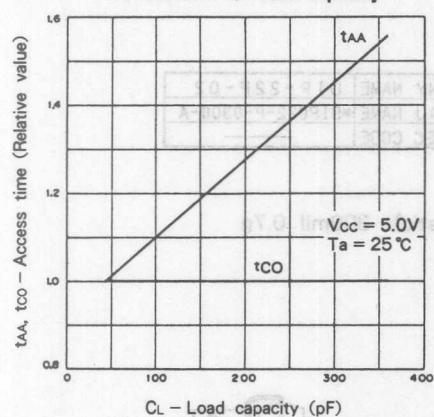
Access time vs. Supply voltage



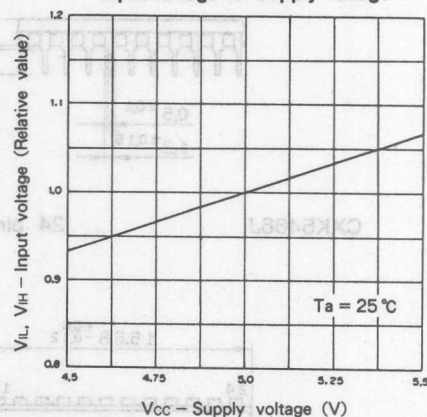
Access time vs. Ambient temperature



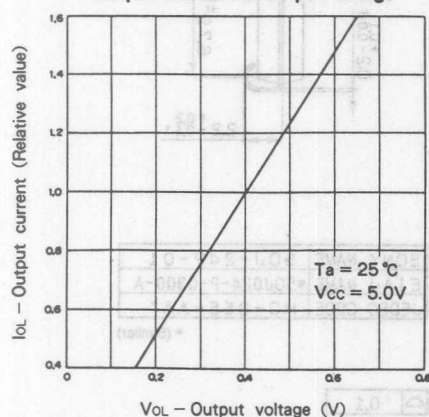
Access time vs. Load capacity



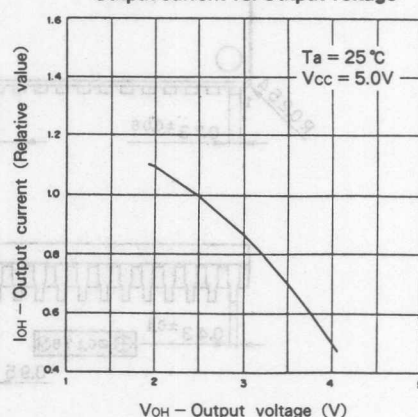
Input voltage vs. Supply voltage



Output current vs. Output voltage



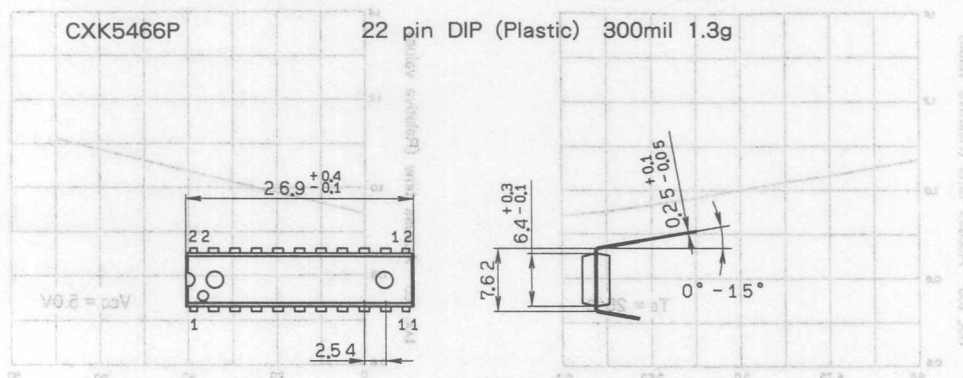
Output current vs. Output voltage



Package Outline Unit : mm

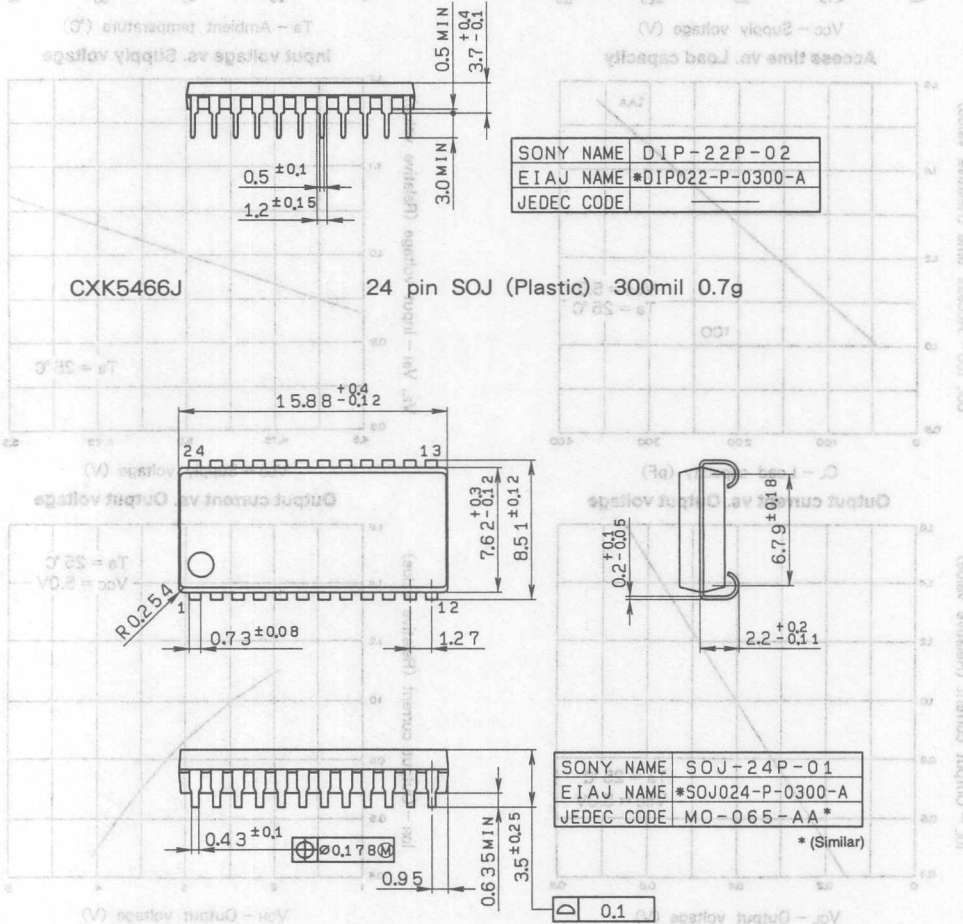
CXK5466P

22 pin DIP (Plastic) 300mil 1.3g



CXK5466J

24 pin SOJ (Plastic) 300mil 0.7g



16,384-word × 4-bit High Speed CMOS Static RAM

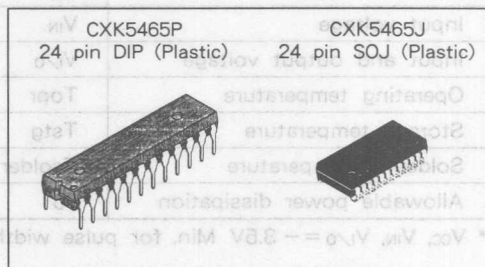
Description

CXK5465P/J are 65,536 bits high speed CMOS static RAMs organized as 16,384 words by 4 bits and operate from a single 5V supply.

These devices feature Output Enable (OE) to enhance their flexibility in high-speed memory applications.

Features

- Fast access time :
CXK5465P/J-25 25ns (Max.)
CXK5465P/J-30 30ns (Max.)
CXK5465P/J-35 35ns (Max.)
- Low power operation : 125mW (Typ.)
- Single + 5V supply : + 5V ± 10 %
- Fully static memory...No clock or timing strobe required.
- Output Enable (OE) control available.
- Equal access and cycle time.
- Common data input and output : three-state output.
- Directly TTL compatible : All inputs and outputs.
- High density : 300mil 24 pin plastic DIP
300mil 24 pin plastic SOJ



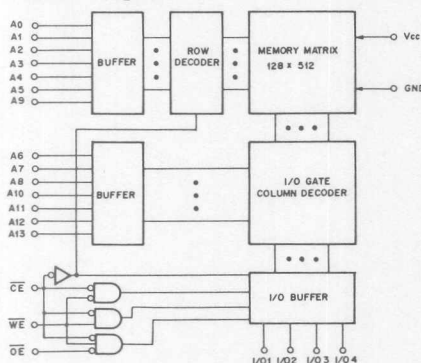
Function

16,384-word × 4-bit static RAM

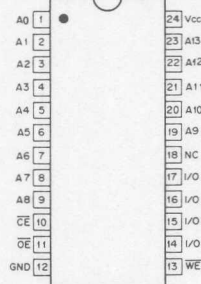
Structure

Silicon gate CMOS IC

Block Diagram



Pin Configuration (Top view)



Pin Description

Symbol	Description
A0 to A13	Address input
I/O1 to I/O4	Data input output
CE	Chip enable input
WE	Write enable input
OE	Output enable input
Vcc	+ 5V Power supply
GND	Ground
NC	Non connection

Absolute Maximum Ratings

(Ta = 25°C, GND = 0V)

Item	Symbol	Rating	Unit
Supply voltage	V _{CC}	- 0.5 * to + 7.0	V
Input voltage	V _{IN}	- 0.5 * to V _{CC} + 0.5	V
Input and output voltage	V _{I/O}	- 0.5 * to V _{CC} + 0.5	V
Operating temperature	T _{opr}	0 to + 70	°C
Storage temperature	T _{stg}	- 55 to + 150	°C
Soldering temperature	T _{solder}	260 • 10	°C • sec
Allowable power dissipation	P _D	1.0	W

* V_{CC}, V_{IN}, V_{I/O} = - 3.5V Min. for pulse width less than 20ns.

Truth Table

CE	OE	WE	Mode	I/O1 to I/O4	V _{CC} Current
H	X	X	Not selected	High Z	I _{SB1} , I _{SB2}
L	H	H	Output disable	High Z	I _{CC1} , I _{CC2}
L	L	H	Read	Data out	I _{CC1} , I _{CC2}
L	X	L	Write	Data in	I _{CC1} , I _{CC2}

X: "H" or "L"

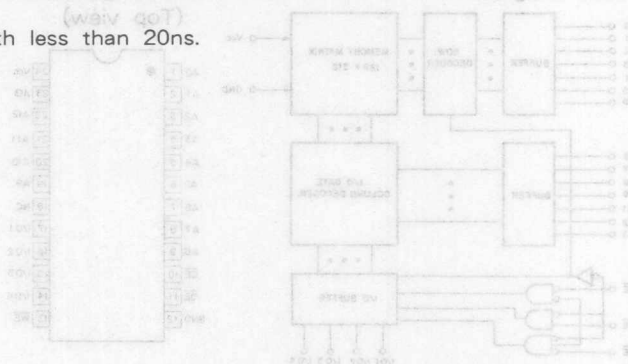
DC Recommended Operating Conditions

(Ta = 0 to + 70°C, GND = 0V)

Item	Symbol	Min.	Typ.*1	Max.	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Input high voltage	V _{IH}	2.2	—	V _{CC} + 0.3	V
Input low voltage	V _{IL}	- 0.3*2	—	0.8	V

*1. V_{CC} = 5V, Ta = 25°C*2. V_{IL} = - 3.0V Min. for pulse width less than 20ns.

Non connection	NC
Ground	GND
+ 5V Power supply	V _{CC}
Output enable input	OE
Write enable input	WE
Chip enable input	CE
Data input/output	I/O1 to I/O4
Address input	A0 to A15



Electrical Characteristics

● DC and operating characteristics (V_{CC} = 5V ± 10%, GND = 0V, T_a = 0 to +70°C)

Item	Symbol	Test conditions	- 25/30/35			Unit
			Min.	Typ.*	Max.	
Input leak current	I _{LI}	V _{IN} = GND to V _{CC}	- 1	—	1	μA
Output leak current	I _{LO}	$\overline{CE} = V_{IH}$ or $OE = V_{IH}$ or $\overline{WE} = V_{IL}$ V _{I/O} = GND to V _{CC}	- 1	—	1	μA
Operating supply current	I _{CC1}	$\overline{CE} = V_{IL}$, I _{OUT} = 0mA V _{IN} = V _{IH} /V _{IL}	—	25	45	mA
Average operating current	I _{CC2}	Cycle = Min., Duty = 100 % I _{OUT} = 0mA	—	60	90	mA
Standby current	I _{SB1}	$\overline{CE} \geq V_{CC} - 0.2V$, V _{IN} $\geq V_{CC} - 0.2V$ or V _{IN} $\leq 0.2V$	—	—	1	mA
	I _{SB2}	$\overline{CE} = V_{IH}$	—	15	30	mA
Output high voltage	V _{OH}	I _{OH} = - 4.0mA	2.4	—	—	V
Output low voltage	V _{OL}	I _{OL} = 8.0mA	—	—	0.4	V

* V_{CC} = 5V, T_a = 25°CI/O capacitance (T_a = 25°C, f = 1MHz)

Item	Symbol	Test conditions	Min.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} = 0V	—	7	pF
Input/Output capacitance	C _{I/O}	V _{I/O} = 0V	—	7	pF

(Note) This parameter is sampled and is not 100% tested.

AC characteristics

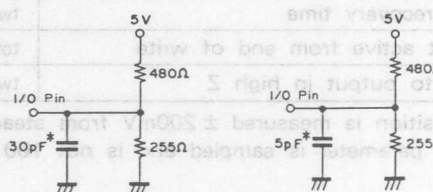
● AC test conditions

(V_{CC} = 5V ± 10%, T_a = 0 to +70°C)

Item	Conditions
Input pulse high level	V _{IH} = 3.0V
Input pulse low level	V _{IL} = 0V
Input rise time	t _r = 5ns
Input fall time	t _f = 5ns
Input and output reference level	1.5V
Output load conditions	Fig. 1

Output Load (1)

Output Load (2)**



* including scope and jig

** for t_{LZ}, t_{HZ}, t_{OHZ}, t_{OLZ}, t_{OW}, t_{WHZ}

Fig. 1

● Read cycle

Item	Symbol	- 25		- 30		- 35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t _{RC}	25	—	30	—	35	—	ns
Address access time	t _{AA}	—	25	—	30	—	35	ns
Chip enable access time (CE)	t _{CO}	—	25	—	30	—	35	ns
Output enable to output valid	t _{OE}	—	12	—	15	—	20	ns
Output hold from address change	t _{OH}	5	—	5	—	5	—	ns
Chip enable to output in low Z (CE)	t _{LZ} *	5	—	5	—	5	—	ns
Output enable to output in low Z (OE)	t _{OLZ} *	0	—	0	—	0	—	ns
Chip disable to output in high Z	t _{HZ} *	0	10	0	15	0	15	ns
Output disable to output in high Z (OE)	t _{OHZ} *	0	10	0	10	0	15	ns
Chip enable to power up time	t _{PU}	0	—	0	—	0	—	ns
Chip disable to power down time	t _{PD}	—	20	—	25	—	25	ns

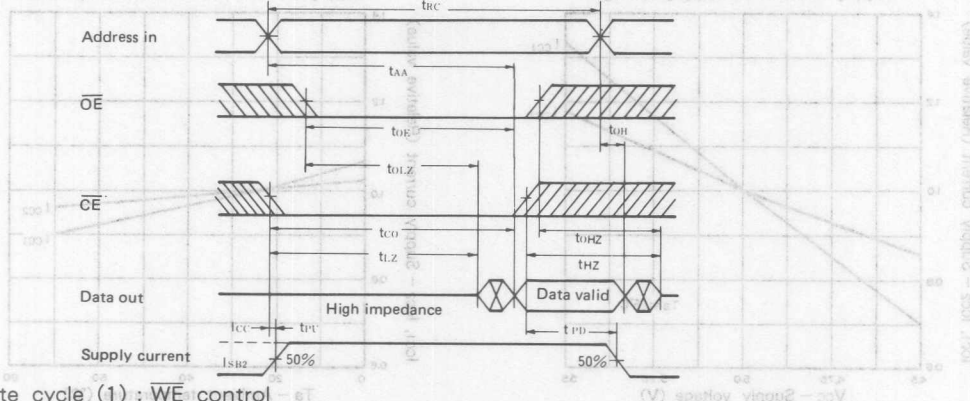
● Write cycle

Item	Symbol	- 25		- 30		- 35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t _{WC}	25	—	30	—	35	—	ns
Address valid to end of write	t _{AW}	20	—	25	—	30	—	ns
Chip enable to end of write	t _{CW}	20	—	25	—	30	—	ns
Data to write time overlap	t _{DW}	12	—	15	—	15	—	ns
Data hold from write time	t _{DH}	0	—	0	—	0	—	ns
Write pulse width	t _{WP}	20	—	25	—	30	—	ns
Address setup time	t _{AS}	0	—	0	—	0	—	ns
Write recovery time	t _{WR}	0	—	0	—	0	—	ns
Output active from end of write	t _{OW} *	5	—	5	—	5	—	ns
Write to output in high Z	t _{WHZ} *	0	10	0	10	0	15	ns

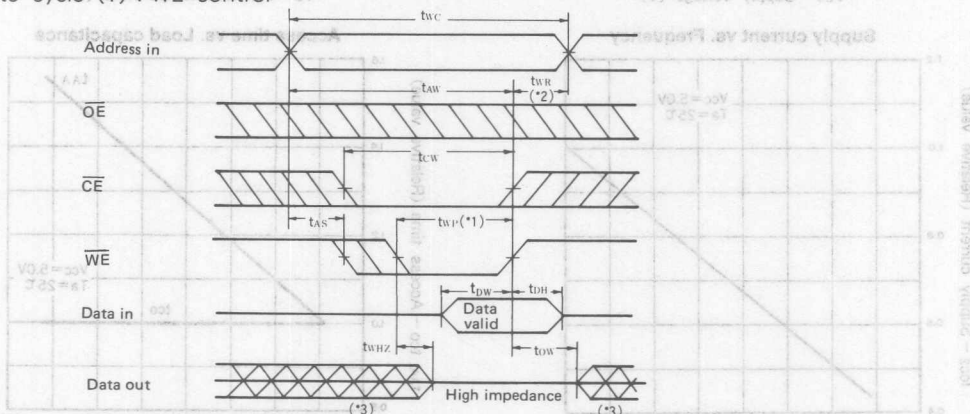
* Transition is measured $\pm 200\text{mV}$ from steady voltage with specified loading in Fig. 1.
This parameter is sampled and is not 100% tested.

Timing Waveform

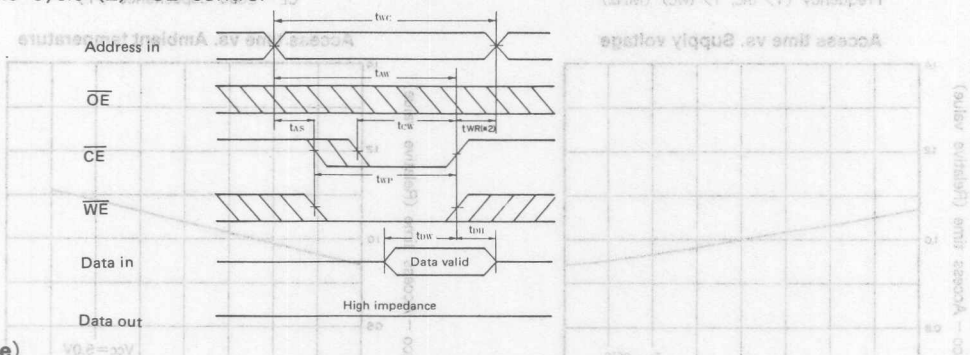
- Read cycle : $\overline{WE} = V_{IH}$



- Write cycle (1) : $\overline{WE}$ control



- Write cycle (2) : $\overline{CE}$ control

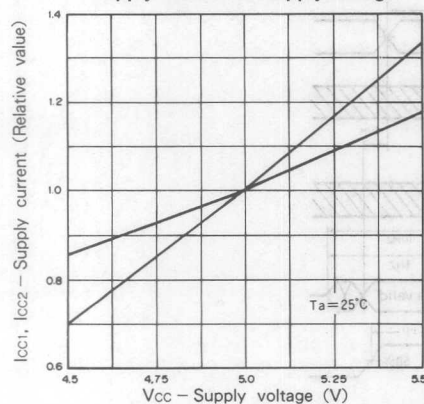


*** Note)**

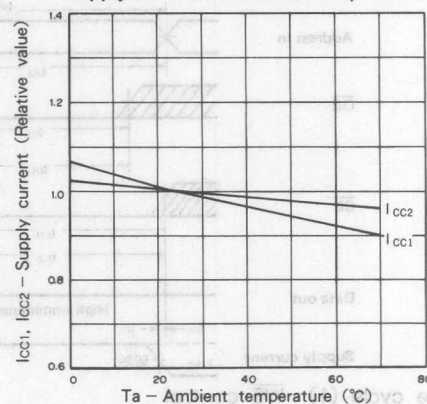
1. A write occurs during the low overlap of $\overline{CE}$ and $\overline{WE}$.
2. t_{wr} is measured from the rising of either $\overline{CE}$ or $\overline{WE}$, whichever is earlier, to the end of write cycle.
3. While I/O pins are in output state, a data input voltage of a phase opposite to the output must not be applied.

Example of Representative Characteristics

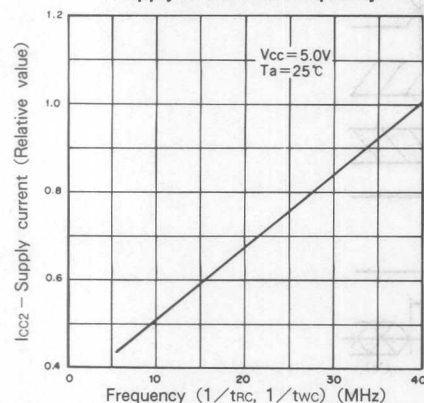
Supply current vs. Supply voltage



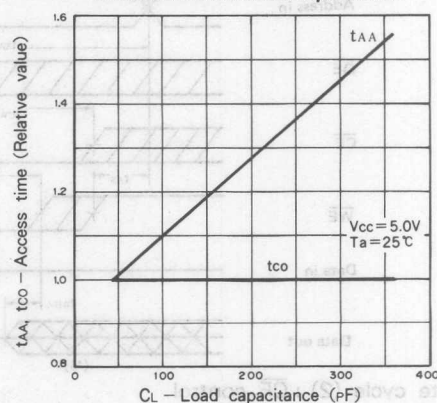
Supply current vs. Ambient temperature



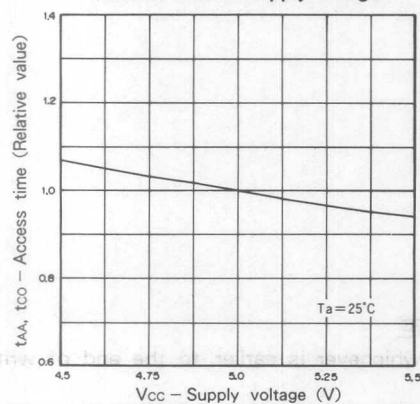
Supply current vs. Frequency



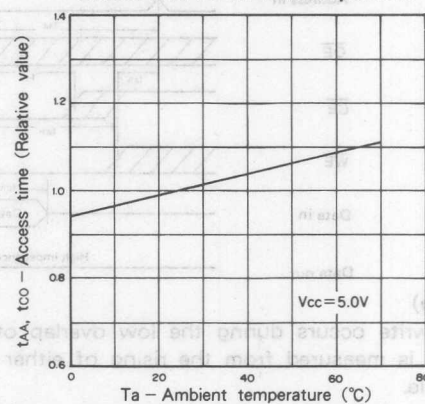
Access time vs. Load capacitance



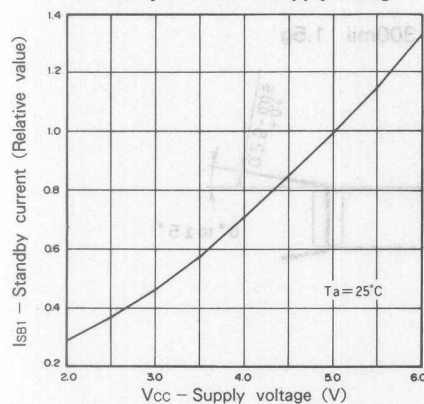
Access time vs. Supply voltage



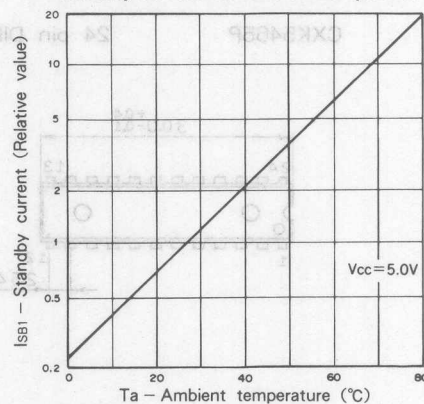
Access time vs. Ambient temperature



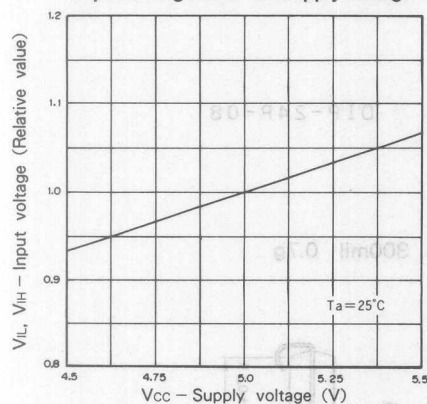
Standby current vs. Supply voltage



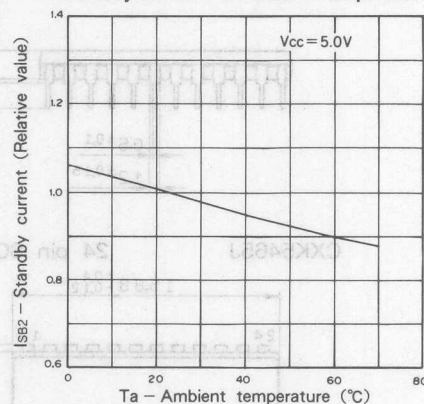
Standby current vs. Ambient temperature



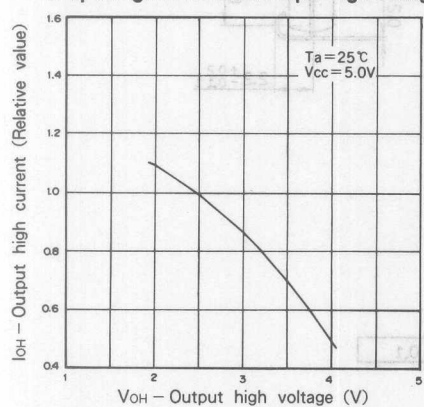
Input voltage level vs. Supply voltage



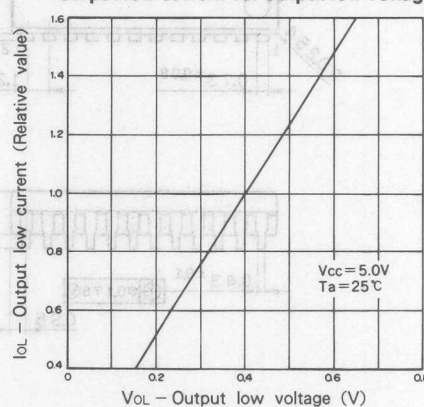
Standby current vs. Ambient temperature



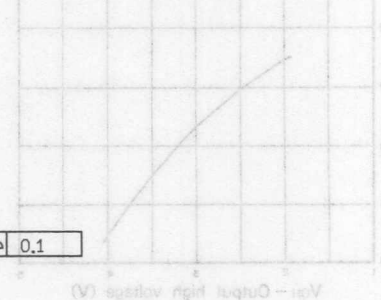
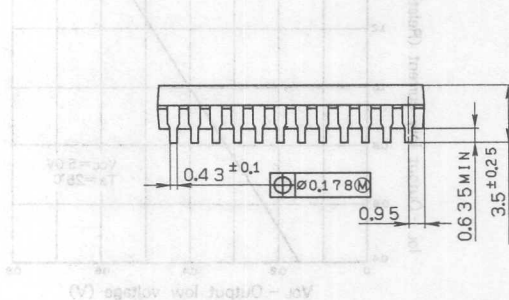
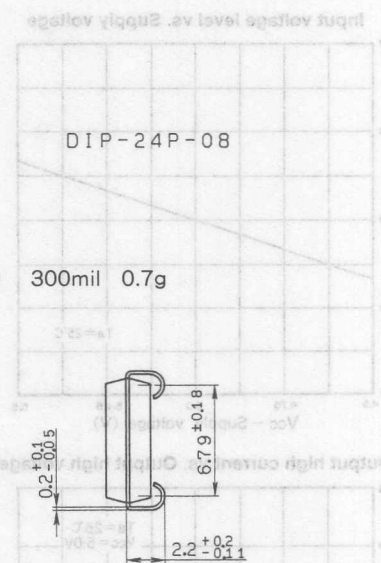
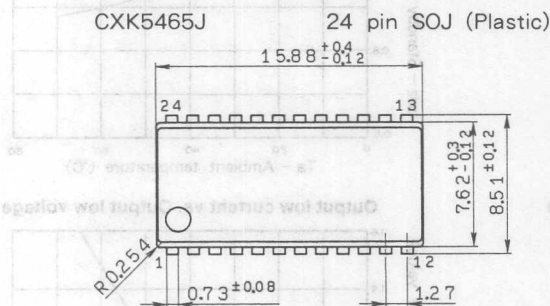
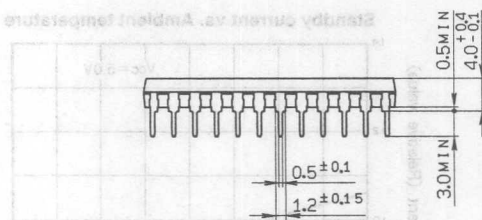
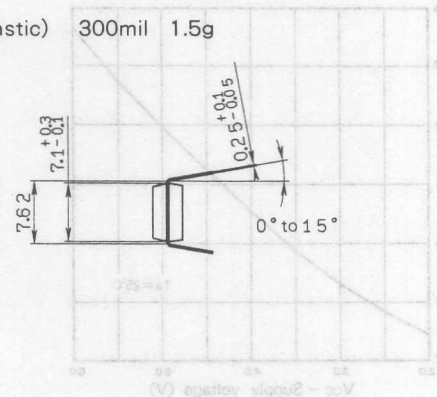
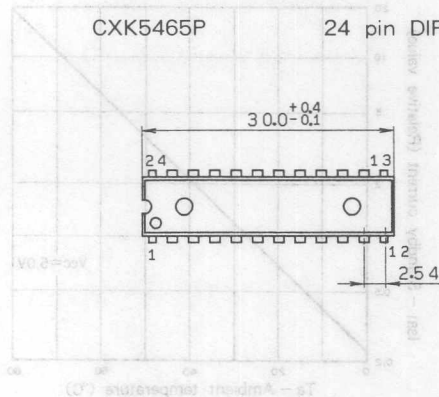
Output high current vs. Output high voltage



Output low current vs. Output low voltage



Package Outline Unit : mm



SOJ-24P-01

16,384 word × 4-bit High Speed CMOS Static RAM

Description

CXK5467P/J is a high speed CMOS static RAM with TTL compatible I/O organized as 16,384 words × 4 bits.

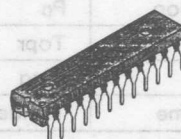
This IC operating on a single 5V supply turns to power down mode at no select time by means of chip enable signal. An output enable pin controls the output.

Features

- Fast access time :
CXK5467P/J-15 15ns (Max.)
CXK5467P/J-20 20ns (Max.)
- Low power consumption : 150mW (Typ.)
During operation
- Single +5V supply : +5V ± 10 %
- Fully static memory
...No clock or timing strobe required
- Output Enable ($\overline{OE}$) control available
- Equal access and cycle time
- Common data input and output :
three-state output
- Directly TTL compatible : All inputs and outputs
- Compatible with various types of packages
- High density : 300 mil 24 pin plastic DIP
300 mil 24 pin plastic SOJ

CXK5467P
24 pin DIP (Plastic)

CXK5467J
24 pin SOJ (Plastic)



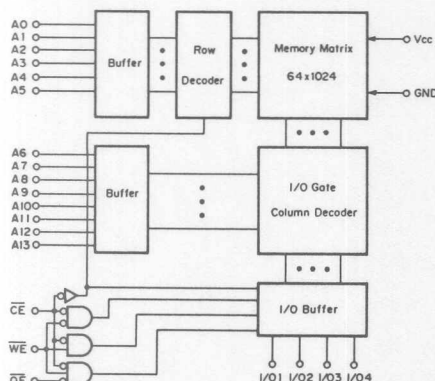
Functions

16,384 word × 4-bit static RAM

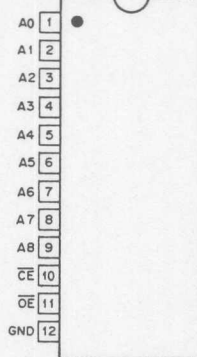
Structure

Silicon gate CMOS IC

Block Diagram



Pin Configuration
(Top View)



Pin Description

Symbol	Description
A0 to A13	Address input
I/O1 to I/O4	Data input/output
$\overline{CE}$	Chip enable input
WE	Write enable input
$\overline{OE}$	Output enable input
Vcc	+ 5V power supply
GND	Ground
NC	No connection

Absolute Maximum Ratings

(Ta = 25°C, GND = 0V)

Item	Symbol	Ratings	Unit
Supply voltage	V _{CC}	-0.5* to +7.0	V
Input voltage	V _{IN}	-0.5* to V _{CC} + 0.5	V
Input and output voltage	V _{I/O}	-0.5* to V _{CC} + 0.5	V
Allowable power dissipation	P _D	1.0	W
Operating temperature	T _{opr}	0 to +70	°C
Storage temperature	T _{stg}	-55 to +150	°C
Soldering temperature • time	T _{solder}	260 • 10	°C • sec

* V_{CC}, V_{IN}, V_{I/O} Min. = -3.5V for pulse width less than 20ns.

Truth Table

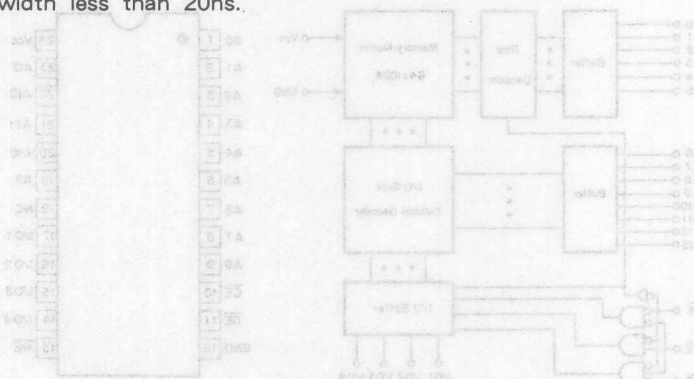
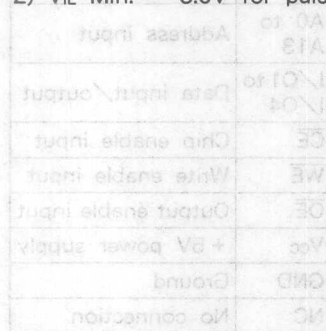
$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O1 to I/O4	V _{CC} current
H	X	X	Not selected	High Z	I _{SB1} , I _{SB2}
L	H	H	Output disable	High Z	I _{CC1} , I _{CC2}
L	L	H	Read	Data output	I _{CC1} , I _{CC2}
L	X	L	Write	Data input	I _{CC1} , I _{CC2}

X : "H" or "L"

DC Recommended Operating Conditions

(Ta = 0 to +70°C, GND = 0V)

Item	Symbol	Min.	Typ.*1	Max.	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Input high voltage	V _{IH}	2.2	—	V _{CC} + 0.3	V
Input low voltage	V _{IL}	-0.3*2	—	0.8	V

*1) V_{CC} = 5V, Ta = 25°C*2) V_{IL} Min. = -3.0V for pulse width less than 20ns.

DC Electrical Characteristics

●DC and operating characteristics

(V_{CC} = 5V ± 10 %, GND = 0V, T_a = 0 to +70 °C)

Item	Symbol	Test Conditions	Min.	Typ.*	Max.	Unit
Input leak current	I _{LI}	V _{IN} = GND to V _{CC}	-1	—	1	μA
Output leak current	I _{LO}	$\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$ V _{I/O} = GND to V _{CC}	-1	—	1	μA
Operating power supply current	I _{CC1}	$\overline{CE} = V_{IL}$, I _{OUT} = 0mA, V _{IN} = V _{IH} or V _{IL}	—	30	55	mA
Average operating current	I _{CC2}	Cycle = Min., Duty = 100 %, I _{OUT} = 0mA	-15	—	95	mA
			-20	—	90	mA
Standby current	I _{SB1}	$\overline{CE} \geq V_{CC} - 0.2V$, V _{IN} $\geq V_{CC} - 0.2V$ or V _{IN} $\leq 0.2V$	—	—	1	mA
	I _{SB2}	$\overline{CE} = V_{IH}$, V _{IN} = V _{IH} /V _{IL} Cycle = Min.	—	—	85	mA
Output high voltage	V _{OH}	I _{OH} = -4.0mA	2.4	—	—	V
Output low voltage	V _{OL}	I _{OL} = 8.0mA	—	—	0.4	V

* V_{CC} = 5.0V, T_a = 25 °C

I/O capacitance

(T_a = 25 °C, f = 1MHz)

Item	Symbol	Test Conditions	Min.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} = 0V	—	7	pF
Input/output capacitance	C _{I/O}	V _{I/O} = 0V	—	7	pF

Note) This parameter is sampled and is not 100 % tested.

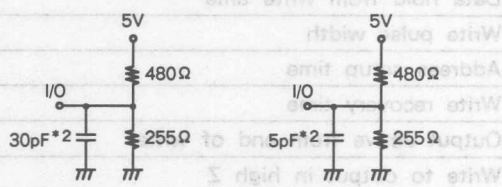
●AC test conditions

(V_{CC} = 5V ± 10 %*1, T_a = 0 to +70 °C)

Item	Conditions
Input pulse high level	V _{IH} = 3.0V
Input pulse low level	V _{IL} = 0V
Input rise time	t _r = 5ns
Input fall time	t _f = 5ns
Input and output reference level	1.5V
Output load conditions	Fig. 1

Output Load (1)

Output Load (2)*3

*1 V_{CC} = 5V ± 5 % for CXK5467P/J-15

*2 including scope and jig capacitance

*3 for t_{LZ}, t_{OLZ}, t_{THZ}, t_{OHZ}, t_{OW}, t_{TWHZ}

Fig. 1

• Read cycle

Item	Symbol	- 15		- 20		Unit
		Min.	Max.	Min.	Max.	
Read cycle time	t _{RC}	15	—	20	—	ns
Address access time	t _{AA}	—	15	—	20	ns
Chip enable access time (CE)	t _{CO}	—	15	—	20	ns
Output enable to output valid	t _{OE}	—	8	—	10	ns
Output hold from address change	t _{OH}	3	—	3	—	ns
Chip enable to output in low Z ($\overline{\text{CE}}$)	t _{LZ} *	2	—	3	—	ns
Output enable to output in low Z ($\overline{\text{OE}}$)	t _{OLZ} *	2	—	3	—	ns
Chip disable to output in high Z	t _{HZ} *	0	6	0	8	ns
Output disable to output in high Z ($\overline{\text{OE}}$)	t _{OHZ} *	0	6	0	8	ns
Chip enable to power up time	t _{PU}	0	—	0	—	ns
Chip disable to power down time	t _{PD}	—	15	—	20	ns

* Transition is tested by means of load conditions (2), from stationary condition at $\pm 200\text{mV}$ (See Fig. 1)

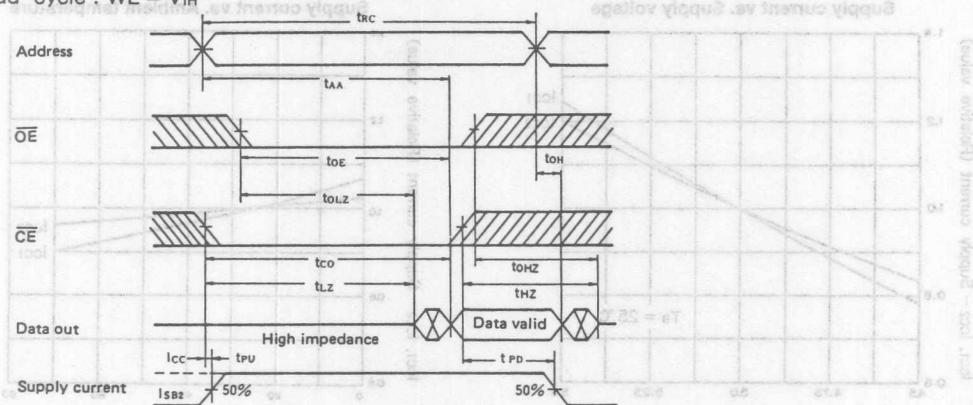
• Write cycle

Item	Symbol	- 15		- 20		Unit
		Min.	Max.	Min.	Max.	
Write cycle time	t _{WC}	15	—	20	—	ns
Address valid to end of write	t _{AW}	13	—	18	—	ns
Chip enable to end of write	t _{CW}	13	—	18	—	ns
Data to write time overlap	t _{DW}	8	—	11	—	ns
Data hold from write time	t _{DH}	0	—	0	—	ns
Write pulse width	t _{WP}	13	—	18	—	ns
Address setup time	t _{AS}	0	—	0	—	ns
Write recovery time	t _{WR}	0	—	0	—	ns
Output active from end of write	t _{OW} *	2	—	3	—	ns
Write to output in high Z	t _{WHZ}	0	5	0	7	ns

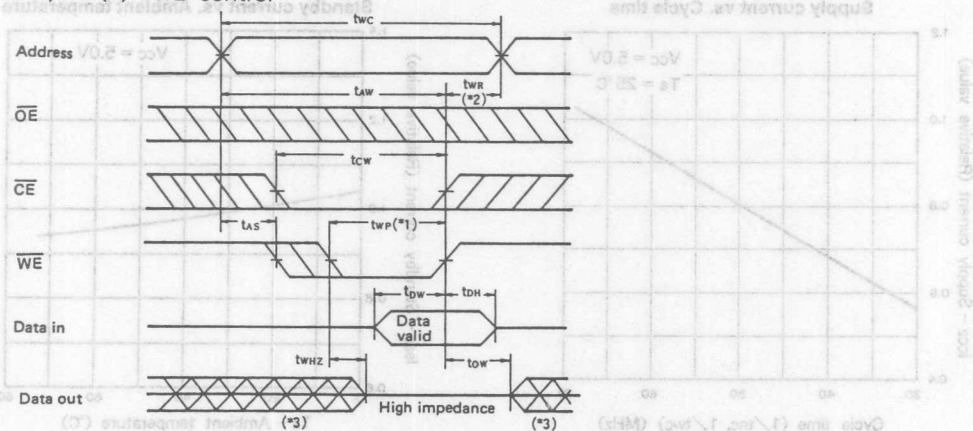
* Transition is tested by means of load conditions (2), from stationary condition at $\pm 200\text{mV}$ (See Fig. 1)

Timing Waveform

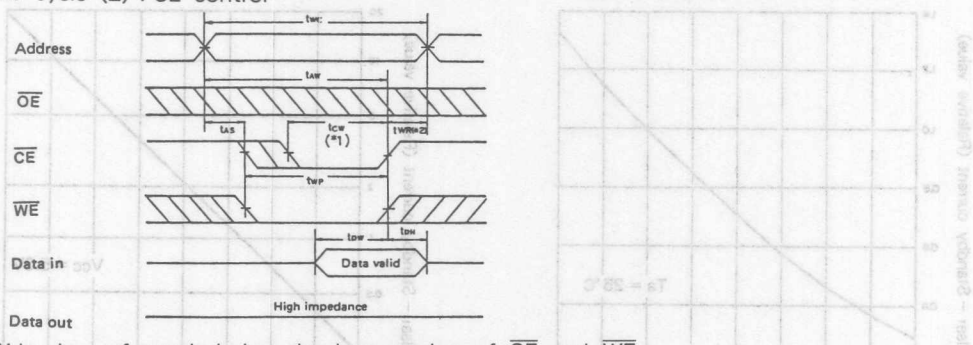
- Read cycle : $\overline{WE} = V_{IH}$



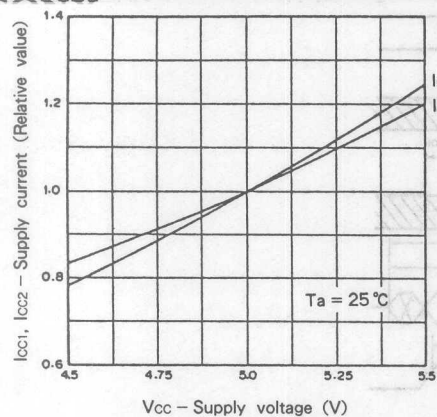
- Write cycle (1) : $\overline{WE}$ control



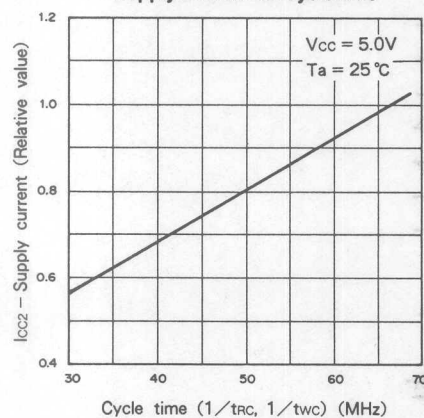
- Write cycle (2) : $\overline{CE}$ control



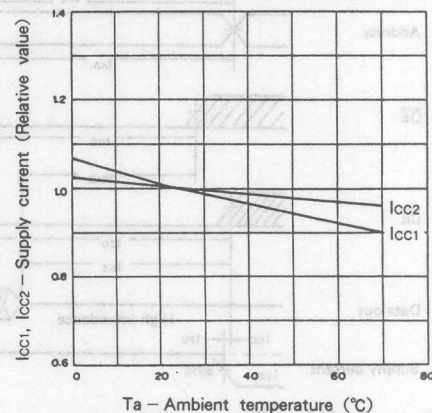
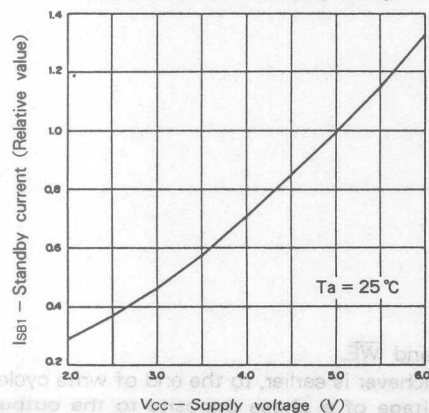
- *1) Write is performed during the low overlap of $\overline{CE}$ and $\overline{WE}$.
- *2) t_{WR} is measured from the rising of either $\overline{CE}$ or $\overline{WE}$, whichever is earlier, to the end of write cycle.
- *3) While I/O pins are in output state, a data input voltage of a phase opposite to the output must not be applied.



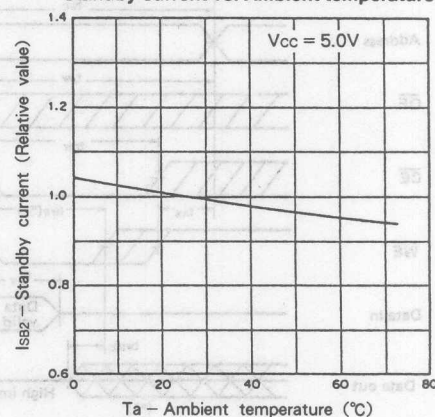
Supply current vs. Cycle time



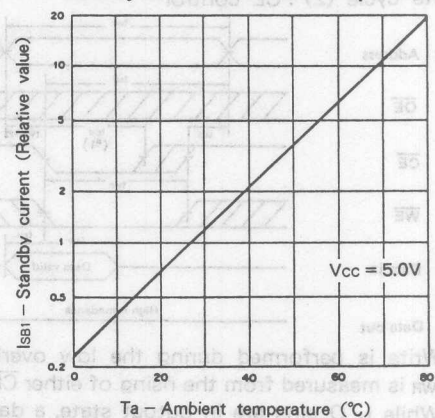
Standby current vs. Supply voltage



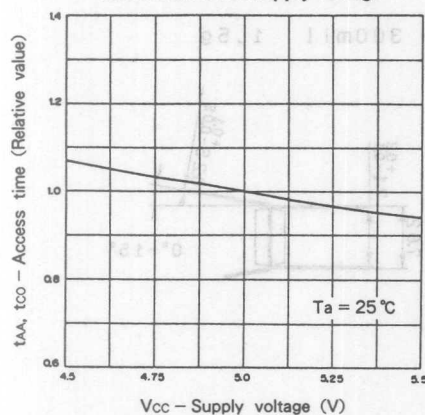
Standby current vs. Ambient temperature



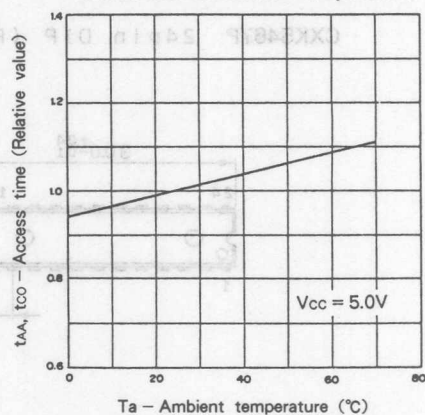
Standby current vs. Ambient temperature



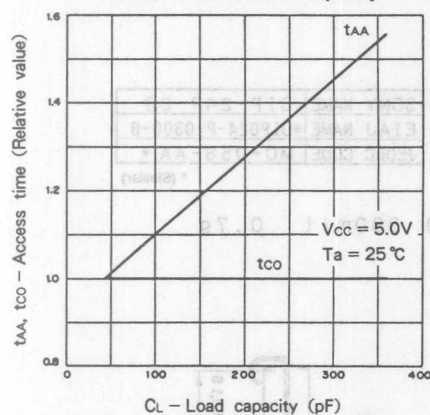
Access time vs. Supply voltage



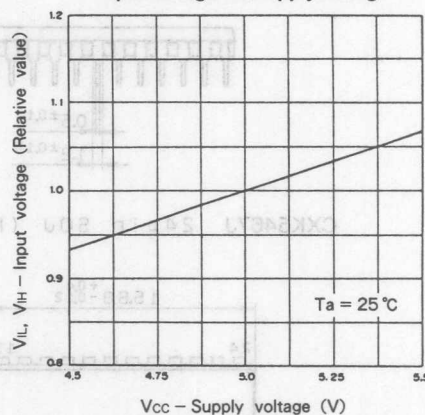
Access time vs. Ambient temperature



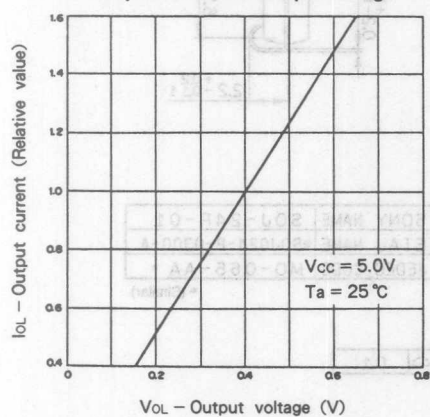
Access time vs. Load capacity



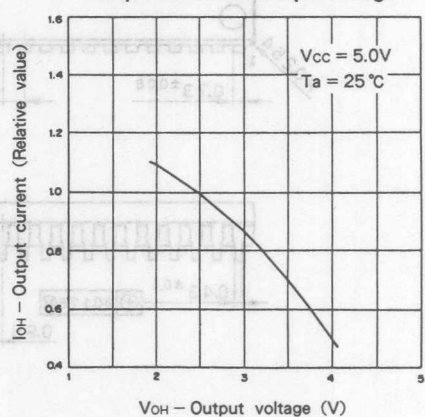
Input voltage vs. Supply voltage



Output current vs. Output voltage

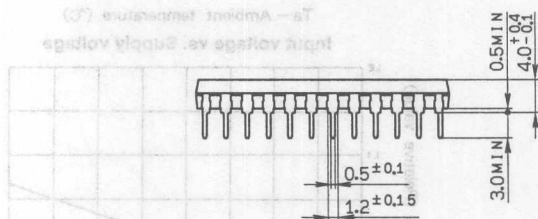
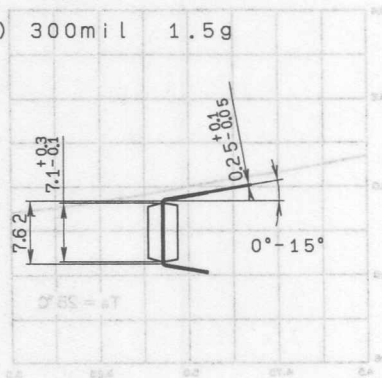
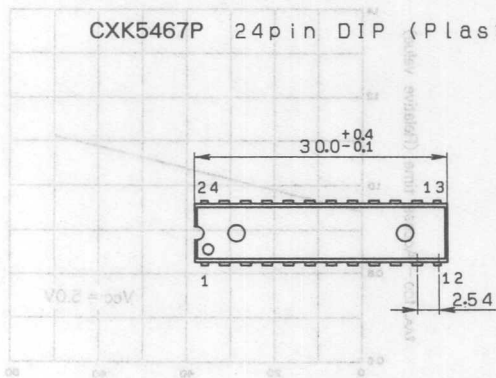


Output current vs. Output voltage



Unit : mm

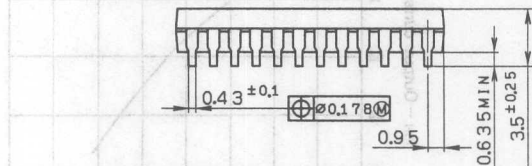
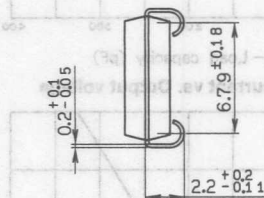
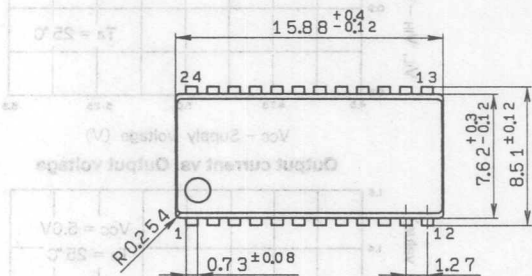
CXK5467P 24pin DIP (Plastic) 300mil 1.5g



SONY NAME	DIP-24P-08
EIAJ NAME	*DIP024-P-0300-B
JEDEC CODE	MO-058-AA*

* (Similar)

CXK5467J 24pin SOJ (Plastic) 300mil 0.7g



SONY NAME	SOJ-24P-01
EIAJ NAME	*SOJ024-P-0300-A
JEDEC CODE	MO-065-AA *

* (Similar)

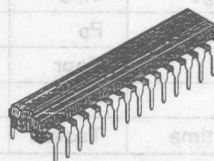
are 65,536 bits high speed organized as 8,192 words from a single 5V supply. suitable for use in high such as cash memory.

20ns/25ns/30ns (Max.)
250mW (Typ)

Part Number	Package Type
CXK5863AP	28 pin DIP (Plastic)
CXK5863AJ	28 pin SOJ (Plastic)

The image shows two integrated circuit packages. On the left is the CXK5863AP, a 28-pin DIP (Dual In-line Package) with pins extending from both sides of a rectangular plastic body. On the right is the CXK5863AJ, a 28-pin SOJ (Small Outline Junction) package, which is a smaller, more compact package with pins extending from one side.

CXK5863AP	CXK5863AJ
28 pin DIP (Plastic)	28 pin SOJ (Plastic)



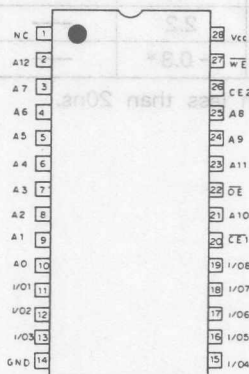
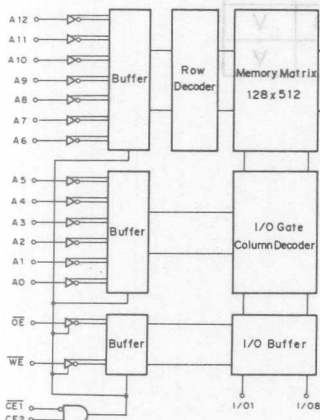
Structure

Silicon gate CMOS IC

8192 word X 8-bit static RAM

- | Function | CE1 | CE2 | CE | WE | OE |
|------------------------------|-----|-----|----|----|----|
| 8192 word × 8-bit static RAM | X | L | L | X | X |
| Output disable | L | H | H | H | H |
| Fast | L | H | L | H | H |
| Write | L | H | X | L | L |

Pin Configuration (Top View)



Symbol	Description
A0 to A12	Address input
I/O1 to I/O8	Data input output
CE1, CE2	Chip enable 1, 2 input
WE	Write enable input
OE	Output enable input
Vcc	+ 5V Power supply
GND	Ground
NC	Non connection

Absolute Maximum Ratings

(Ta = 25°C, GND = 0V)

Item	Symbol	Rating	Unit
Supply voltage	V _{CC}	- 0.5* to + 7.0	V
Input voltage	V _{IN}	- 0.5* to V _{CC} + 0.5	V
Input and output voltage	V _{I/O}	- 0.5* to V _{CC} + 0.5	V
Allowable power dissipation	P _D	1.0	W
Operating temperature	T _{opr}	0 to + 70	°C
Storage temperature	T _{stg}	- 55 to + 150	°C
Soldering temperature • time	T _{solder}	260 • 10	°C • sec

* V_{CC}, V_{IN}, V_{I/O} = - 3.5V Min. for pulse width less than 20ns.

Truth Table

CET	CE2	OE	WE	Mode	I/O1 to I/O8	V _{CC} Current
H	X	X	X	Not selected	High Z	I _{SB1} , I _{SB2}
X	L	X	X	Not selected	High Z	I _{SB1} , I _{SB2}
L	H	H	H	Output disable	High Z	I _{CC1} , I _{CC2}
L	H	L	H	Read	Data out	I _{CC1} , I _{CC2}
L	H	X	L	Write	Data in	I _{CC1} , I _{CC2}

X : "H" or "L"

DC Recommended Operating Conditions

(Ta = 0 to + 70°C, GND = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Input high voltage	V _{IH}	2.2	—	V _{CC} + 0.3	V
Input low voltage	V _{IL}	- 0.3*	—	0.8	V

* V_{IL} = - 3.0V Min. for pulse width less than 20ns.

Electrical Characteristics

DC and operating characteristics

(V_{CC} = 5V ± 10 %, GND = 0V, T_a = 0 to +70 °C)

Item	Symbol	Test condition	- 20			- 25/- 30			Unit
			Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Input leakage current	I _{LI}	V _{IN} = GND to V _{CC}	- 1	—	1	- 1	—	1	μA
Output leakage current	I _{LO}	V _{I/O} = GND to V _{CC} , CE1 = V _{IH} or CE2 = V _{IL} or OE = V _{IH} or WE = V _{IL}	- 1	—	1	- 1	—	1	μA
Operating power supply current	I _{CC1}	CE1 = V _{IL} , CE2 = V _{IH} , V _{IN} = V _{IH} or V _{IL} , I _{OUT} = 0mA	—	50	80	—	50	80	mA
Average operating current	I _{CC2}	Cycle = Min, Duty = 100 %, I _{OUT} = 0mA	—	95	130	—	70	90	mA
Standby current	I _{SB1}	CE1 ≥ V _{CC} - 0.2V or CE2 ≤ 0.2V V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V	—	—	1	—	—	1	mA
	I _{SB2}	CE1 = V _{IH} or CE2 = V _{IL} , V _{IN} = V _{IL} or V _{IH}	—	10	25	—	10	25	mA
Output high voltage	V _{OH}	I _{OH} = - 4.0mA	2.4	—	—	2.4	—	—	V
Output low voltage	V _{OL}	I _{OL} = 8.0mA	—	—	0.4	—	—	0.4	V

* V_{CC} = 5V, T_a = 25 °C

I/O capacitance

(T_a = 25 °C, f = 1MHz)

Item	Symbol	Test conditions	Min.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} = 0V	—	7	pF
I/O capacitance	C _{I/O}	V _{I/O} = 0V	—	7	pF

Note) This parameter is sampled and is not 100 % tested.

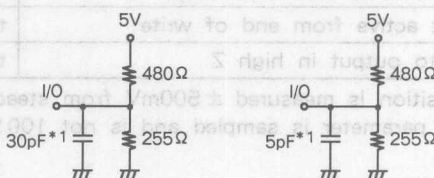
AC characteristics

• AC test conditions

(V_{CC} = 5V ± 10 %, T_a = 0 to +70 °C)

Item	Conditions
Input pulse high level	V _{IH} = 3.0V
Input pulse low level	V _{IL} = 0V
Input rise time	t _r = 5ns
Input fall time	t _f = 5ns
Input and output reference level	1.5V
Output load conditions	Fig. 1

Output Load (1) Output Load (2) *2



*1 including scope and jig capacitance

*2 for t_{LZ1}, t_{LZ2}, t_{OLZ}, t_{HZ1}, t_{HZ2}, t_{OHZ}, t_{OW}, t_{WHZ}

Fig. 1

1) Read cycle

Item	Symbol	- 20		- 25		- 30		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t _{RC}	20	—	25	—	30	—	ns
Address access time	t _{AA}	—	20	—	25	—	30	ns
Chip enable access time ($\overline{\text{CE1}}$)	t _{CO1}	—	20	—	25	—	30	ns
Chip enable access time (CE2)	t _{CO2}	—	20	—	25	—	30	ns
Output enable to output valid	t _{OE}	—	10	—	12	—	12	ns
Output hold from address change	t _{OH}	5	—	5	—	5	—	ns
Chip enable to output in low Z ($\overline{\text{CE1}}$, CE2)	t _{LZ1} *, t _{LZ2} *	5	—	5	—	5	—	ns
Output enable to output in low Z ($\overline{\text{OE}}$)	t _{OLZ} *	0	—	0	—	0	—	ns
Chip disable to output in high Z ($\overline{\text{CE1}}$, CE2)	t _{HZ1} *, t _{HZ2} *	0	10	0	12	0	12	ns
Chip disable to output in high Z ($\overline{\text{OE}}$)	t _{OHZ} *	0	8	0	10	0	10	ns
Chip enable to power up time ($\overline{\text{CE1}}$, CE2)	t _{PU}	0	—	0	—	0	—	ns
Chip disable to power down time ($\overline{\text{CE1}}$, CE2)	t _{PD}	—	20	—	20	—	20	ns

2) Write cycle

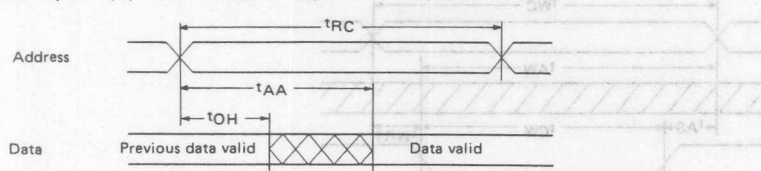
Item	Symbol	- 20		- 25		- 30		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t _{WC}	20	—	25	—	30	—	ns
Address valid to end of write	t _{AW}	15	—	20	—	20	—	ns
Chip enable to end of write	t _{CW}	15	—	20	—	20	—	ns
Data to write time overlap	t _{DW}	10	—	12	—	12	—	ns
Data hold from write time	t _{DH}	0	—	0	—	0	—	ns
Write pulse width	t _{WP}	15	—	20	—	20	—	ns
Address set up time	t _{AS}	0	—	0	—	0	—	ns
Write recovery time ($\overline{\text{WE}}$)	t _{WR}	0	—	0	—	0	—	ns
Write recovery time (CE1, CE2)	t _{WR1}	0	—	0	—	0	—	ns
Output active from end of write	t _{OW} *	5	—	5	—	5	—	ns
Write to output in high Z	t _{WHZ} *	0	10	0	12	0	12	ns

* Transition is measured $\pm 500\text{mV}$ from steady voltage with specified loading in Fig. 1-(2).
This parameter is sampled and is not 100% tested.

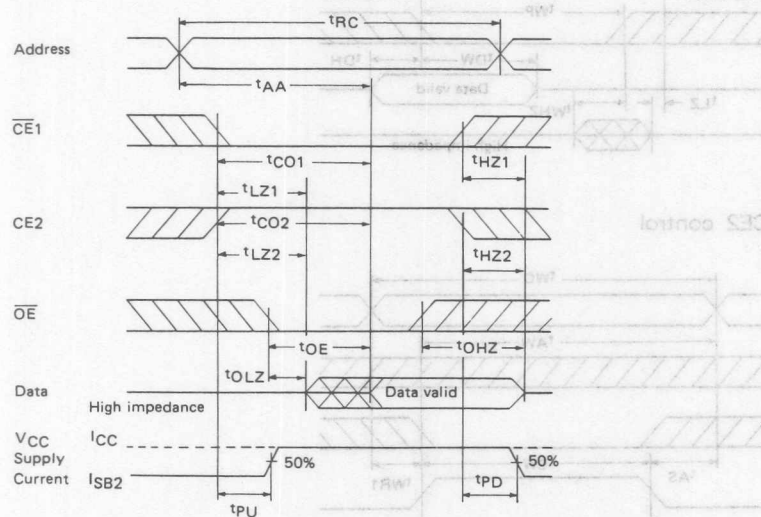
Timing Waveform

1) Read cycle

- Read cycle (1) : $\overline{CE1} = \overline{OE} = V_{IL}$, $CE2 = V_{IH}$, $\overline{WE} = V_{IH}$

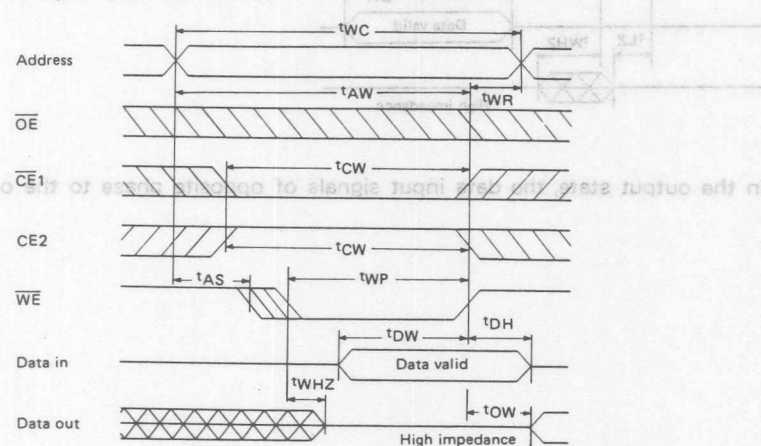


- Read cycle (2) : $\overline{WE} = V_{IH}$

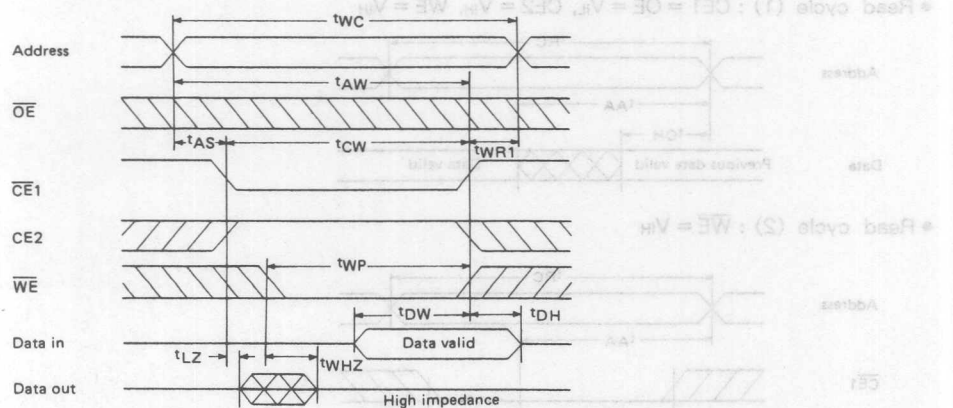


2) Write cycle

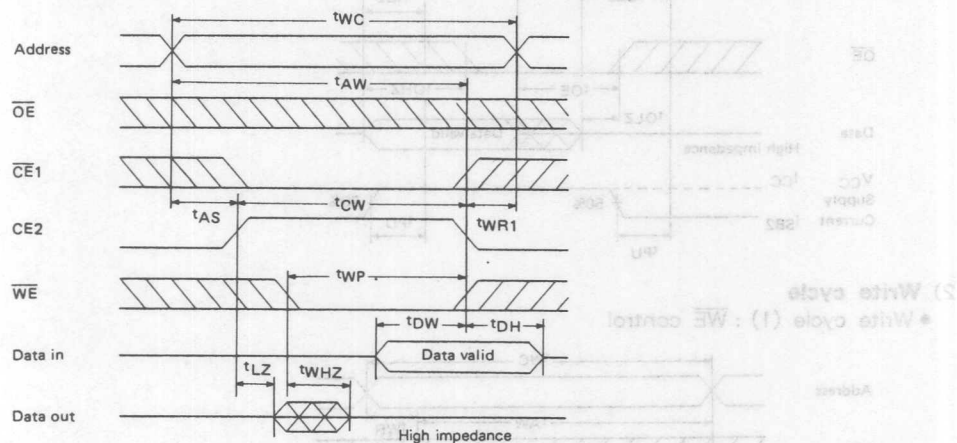
- Write cycle (1) : $\overline{WE}$ control



• Write cycle (2) : $\overline{\text{CE1}}$ control



• Write cycle (3) : CE2 control

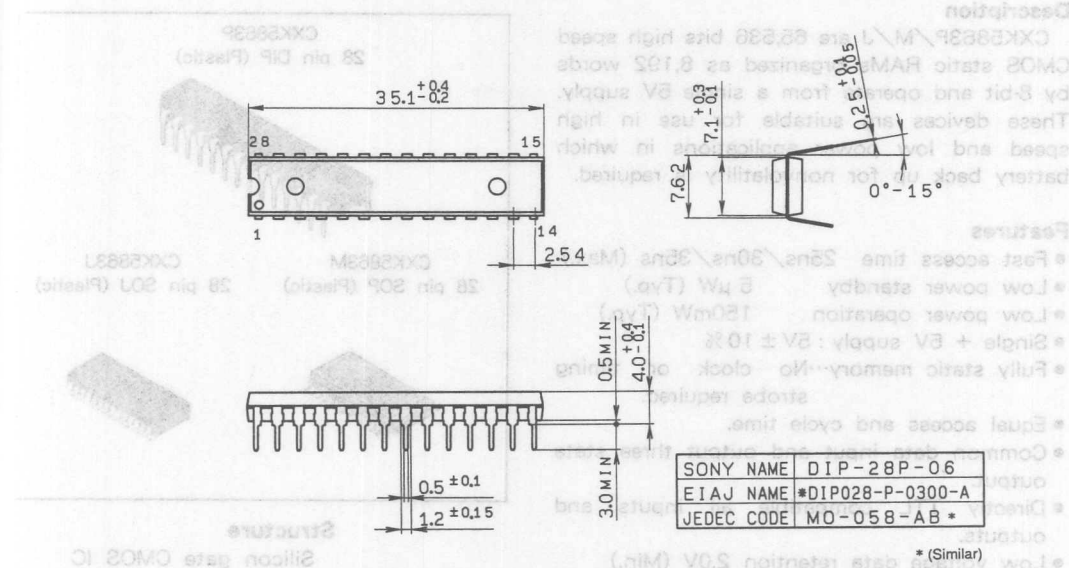


During I/O pins are in the output state, the data input signals of opposite phase to the output must not be applied.

Package Outline Unit : mm

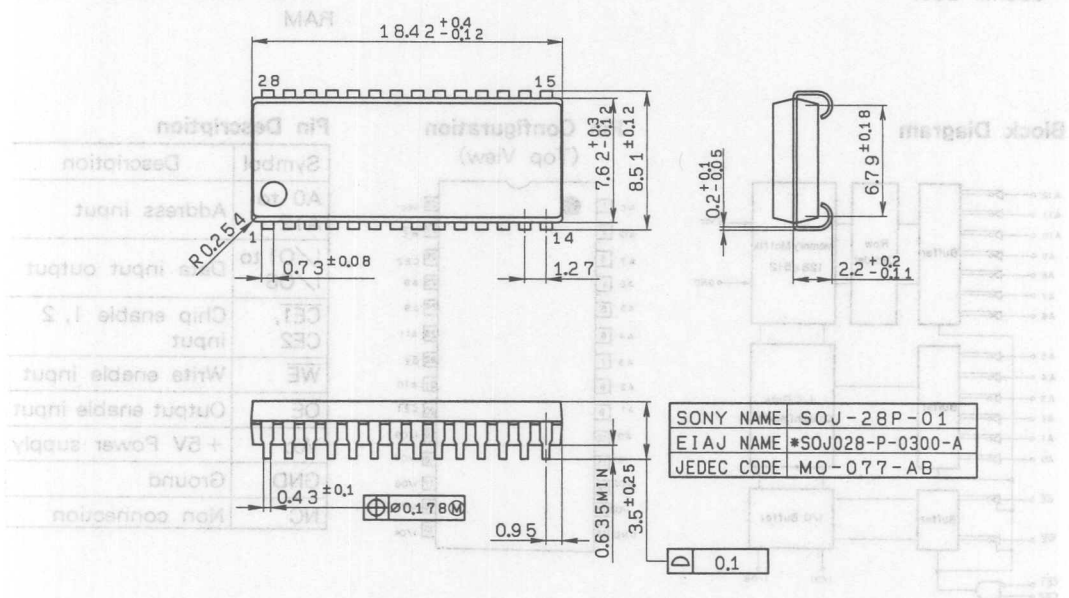
CXK5863AP

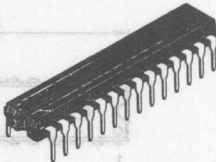
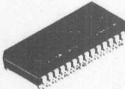
28pin DIP (Plastic) 300mil 2.0g



CXK5863AJ

28pin SOJ (Plastic) 300mil 0.8g



- CXK5863P
28 pin DIP (Plastic)
- 
- CXK5863M
28 pin SOP (Plastic)
- 
- CXK5863J
28 pin SOJ (Plastic)
- 

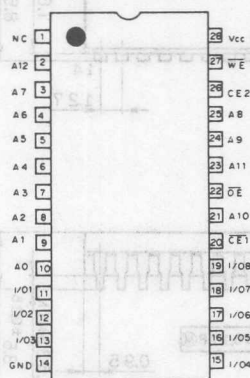
CXK5863M
28 pin SOP (Plastic)

CXK5863J
28 pin SOJ (Plastic)

Function

8192-word $\times$ 8-b
RAM

Pin Configuration (Top View)



Symbol	Description
A0 to A12	Address input
I/O1 to I/O8	Data input output
$\overline{CE}1$, CE2	Chip enable 1, 2 input
$\overline{WE}$	Write enable input
$\overline{OE}$	Output enable input
V _{cc}	+ 5V Power supply
GND	Ground
NC	Non connection

Absolute Maximum Ratings

Ta = 25 °C, GND = 0V

Item	Symbol	Rating	Unit	
Supply voltage	V _{CC}	- 0.5* to + 7.0	V	
Input voltage	V _{IN}	- 0.5* to V _{CC} + 0.5	V	
Input and output voltage	V _{I/O}	- 0.5* to V _{CC} + 0.5	V	
Allowable power dissipation	P _D	CXK5863P/J	1.0	W
		CXK5863M	0.7	W
Operating temperature	T _{opr}	0 to + 70	℃	
Storage temperature	T _{stg}	- 55 to + 150	℃	
Soldering temperature	T _{solder}	260 • 10	℃ • sec	

*Note) V_{CC}, V_{IN}, V_{I/O} = -3.5V Min. for pulse width less than 20ns.

Truth Table

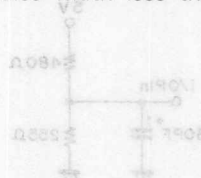
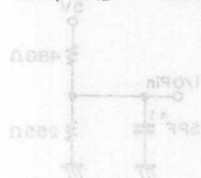
CE1	CE2	OE	WE	Mode	I/O1 to I/O8	V _{CC} Current
H	X	X	X	Not selected	High Z	Isb1, Isb2
X	L	X	X	Not selected	High Z	Isb1, Isb2
L	H	H	H	Output disable	High Z	Icc1, Icc2
L	H	L	H	Read	Data out	Icc1, Icc2
L	H	X	L	Write	Data in	Icc1, Icc2

X: "H" or "L"

DC Recommended Operating Conditions

Ta = 0 to +70 °C, GND = 0V

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Input high voltage	V _{IH}	2.2	—	V _{CC} + 0.3	V
Input low voltage	V _{IL}	-0.3*	—	0.8	V

*Note) V_{IL} = -3.0V Min. for pulse width less than 20ns.

Item	Condition
Input pulse high level	V _{IH} = 3.0V
Input pulse low level	V _{IL} = 0V
Input rise time	t _r = 5ns
Input fall time	t _f = 5ns
Input and output reference level	1.5V
Output load conditions	Fig. 1

Fig. 1

Electrical Characteristics

DC and operating characteristics

 $V_{CC} = 5V \pm 10\%$, $GND = 0V$, $T_a = 0$ to $+70^\circ C$

Item	Symbol	Test condition	- 25/30/35			Unit
			Min.	Typ.*	Max.	
Input leakage current	I_{LI}	$V_{IN} = GND$ to V_{CC}	-1	—	1	μA
Output leakage current	I_{LO}	$V_{I/O} = GND$ to V_{CC} , $\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$ or $OE = V_{IH}$ or $WE = V_{IL}$	-1	—	1	μA
Operating power supply current	I_{CC1}	$\overline{CE1} = V_{IL}$, $CE2 = V_{IH}$, $V_{IN} = V_{IH}$ or V_{IL} $I_{OUT} = 0mA$	—	30	60	mA
Average operating current	I_{CC2}	Cycle = Min, Duty = 100%, $I_{OUT} = 0mA$	—	60	90	mA
Standby current	I_{SB1}	$\overline{CE1} \geq V_{CC} - 0.2V$ or $CE2 \leq 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	—	1	100	μA
	I_{SB2}	$\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$, $V_{IN} = V_{IL}$ or V_{IH}	—	10	25	mA
Output high voltage	V_{OH}	$I_{OH} = -4.0mA$	2.4	—	—	V
Output low voltage	V_{OL}	$I_{OL} = 8.0mA$	—	—	0.4	V

* $V_{CC} = 5V$, $T_a = 25^\circ C$

I/O capacitance

 $T_a = 25^\circ C$, $f = 1MHz$

Item	Symbol	Test condition	Min.	Max.	Unit
Input capacitance	C_{IN}	$V_{IN} = 0V$	—	7	pF
I/O capacitance	$C_{I/O}$	$V_{I/O} = 0V$	—	10	pF

Note) This parameter is sampled and is not 100% tested.

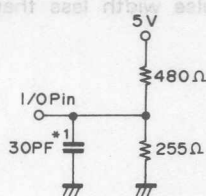
AC characteristics

● AC test conditions

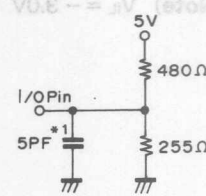
 $V_{CC} = 5V \pm 10\%$, $T_a = 0$ to $+70^\circ C$

Item	Condition
Input pulse high level	$V_{IH} = 3.0V$
Input pulse low level	$V_{IL} = 0V$
Input rise time	$t_r = 5ns$
Input fall time	$t_f = 5ns$
Input and output reference level	1.5V
Output load conditions	Fig. 1

Output Load (1)



Output Load (2)*2



* 1. including scope and jig capacitance

* 2. for t_{LZ1} , t_{LZ2} , t_{OLZ} , t_{HZ1} , t_{HZ2} , t_{OHZ} , t_{OW} , t_{WHZ}

Fig. 1

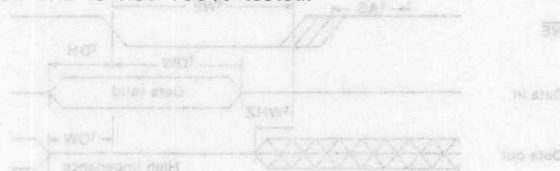
• Read cycle

Item	Symbol	- 25		- 30		- 35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t _{RC}	25	—	30	—	35	—	ns
Address access time	t _{AA}	—	25	—	30	—	35	ns
Chip enable access time (CE1)	t _{CO1}	—	25	—	30	—	35	ns
Chip enable access time (CE2)	t _{CO2}	—	25	—	30	—	35	ns
Output enable to output valid	t _{OE}	—	15	—	15	—	20	ns
Output hold from address change	t _{OH}	5	—	5	—	5	—	ns
Chip enable to output in low Z (CE1, CE2)	t _{LE1} * t _{LE2} *	5	—	5	—	5	—	ns
Output enable to output in low Z (OE)	t _{OLZ} *	0	—	0	—	0	—	ns
Chip disable to output in high Z (CE1, CE2)	t _{HE1} * t _{HE2} *	0	15	0	15	0	20	ns
Chip disable to output in high Z (OE)	t _{OHZ} *	0	13	0	13	0	15	ns
Chip enable to power up time (CE1, CE2)	t _{PU}	0	—	0	—	0	—	ns
Chip disable to power down time (CE1, CE2)	t _{PD}	—	20	—	20	—	20	ns

• Write cycle

Item	Symbol	- 25		- 30		- 35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t _{WC}	25	—	30	—	35	—	ns
Address valid to end of write	t _{AW}	20	—	20	—	30	—	ns
Chip enable to end of write	t _{CW}	20	—	20	—	30	—	ns
Data to write time overlap	t _{DW}	12	—	12	—	15	—	ns
Data hold from write time	t _{DH}	0	—	0	—	0	—	ns
Write pulse width	t _{WP}	20	—	20	—	25	—	ns
Address set up time	t _{AS}	0	—	0	—	0	—	ns
Write recovery time (WE)	t _{WR}	0	—	0	—	0	—	ns
Write recovery time (CE1, CE2)	t _{WR1}	0	—	0	—	0	—	ns
Output active from end of write	t _{OW} *	5	—	5	—	5	—	ns
Write to output in high Z	t _{WHZ} *	0	13	0	13	0	15	ns

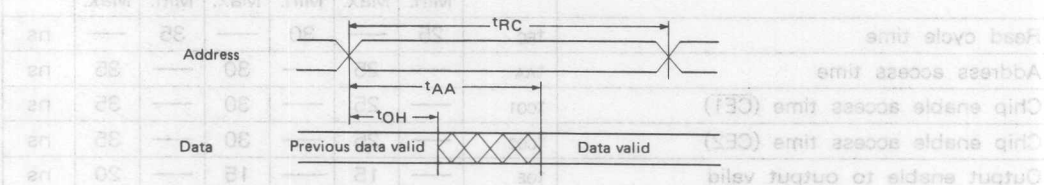
* Transition is measured $\pm 500\text{mV}$ from steady voltage with specified loading in Fig. 1-(2).
This parameter is sampled and is not 100% tested.



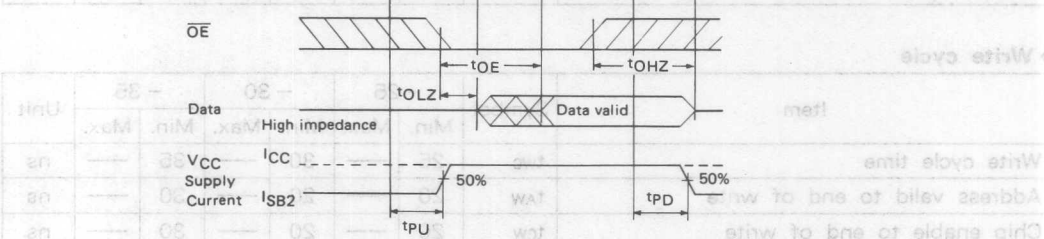
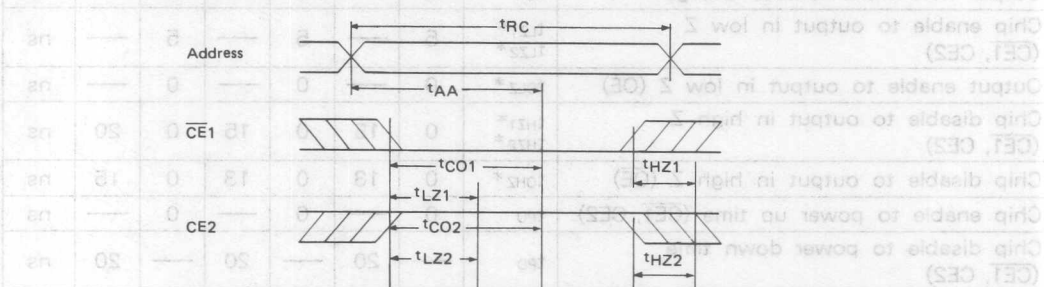
Timing Waveform

1) Read cycle

- Read cycle No. 1 : [$\overline{CE1} = \overline{OE} = V_{IL}$, $CE2 = V_{IH}$, $\overline{WE} = V_{IH}$]

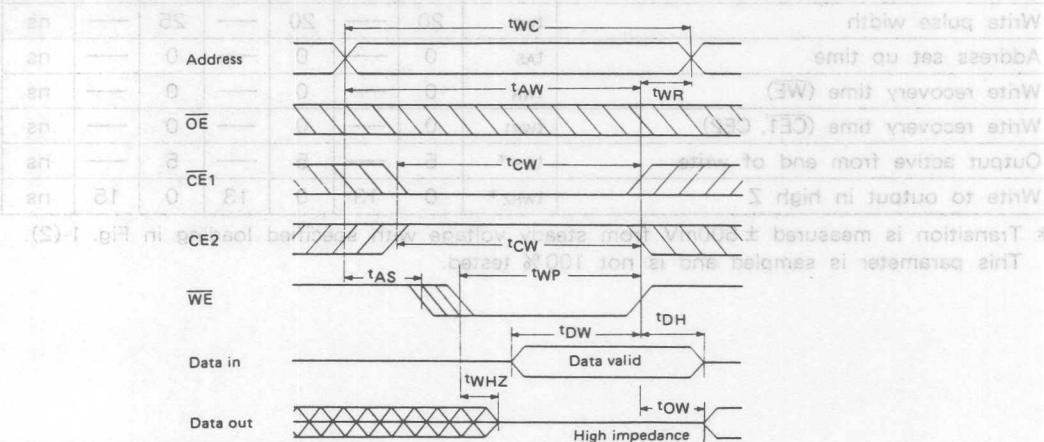


- Read cycle No. 2 : [$\overline{WE} = V_{IH}$]

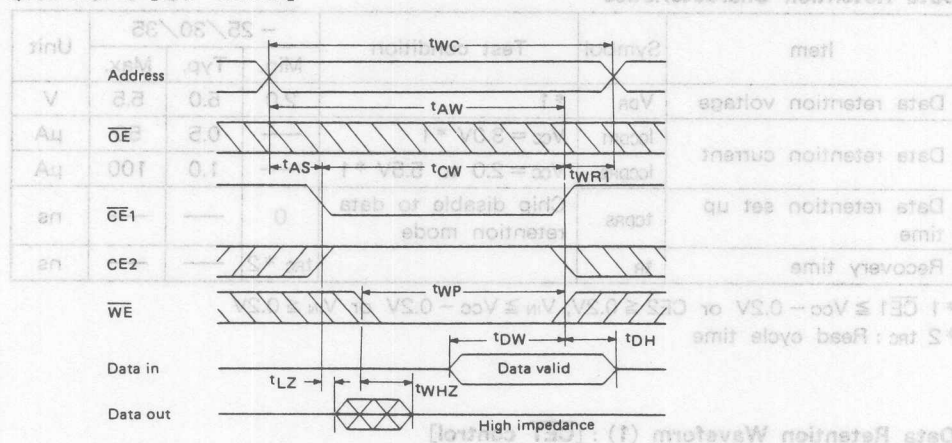


2) Write cycle

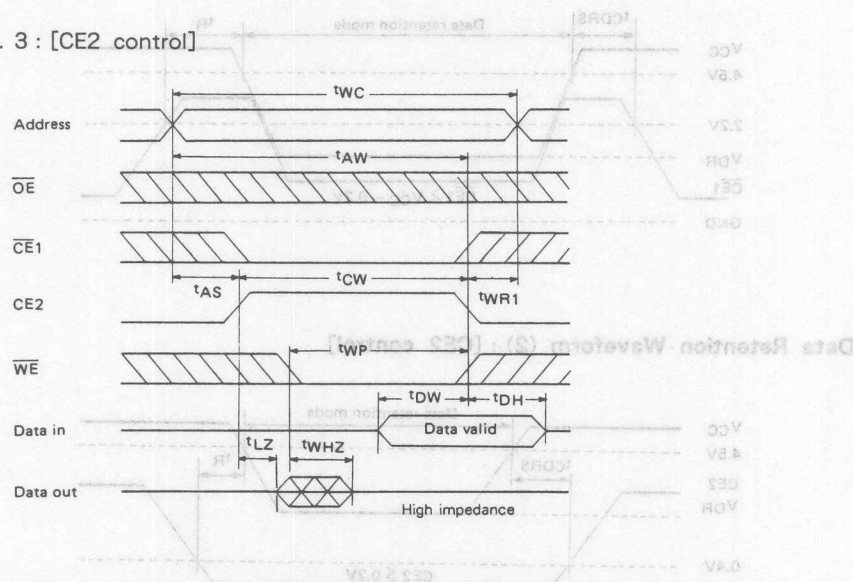
- Write cycle No. 1 : [$\overline{WE}$ control]



• Write cycle No. 2: [$\overline{\text{CE1}}$ control]



• Write cycle No. 3: [CE2 control]



During I/O pins are in the output state, the data input signals of opposite phase to the output must not be applied.

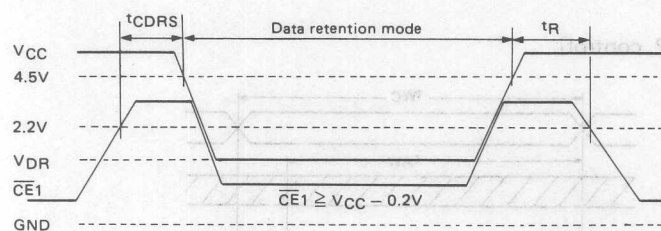
Data Retention Characteristics

Ta = 0 to +70°C

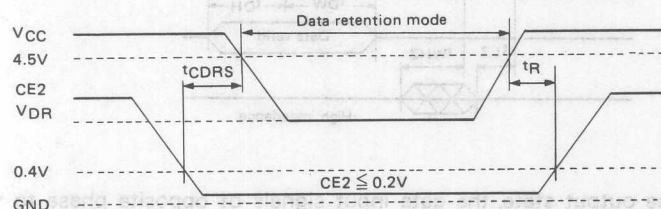
Item	Symbol	Test condition	-25/30/35			Unit
			Min.	Typ.	Max.	
Data retention voltage	V _{DR}	*1	2.0	5.0	5.5	V
Data retention current	I _{CCDR1}	V _{CC} = 3.0V *1	—	0.5	50	μA
	I _{CCDR2}	V _{CC} = 2.0 to 5.5V *1	—	1.0	100	μA
Data retention set up time	t _{CDRS}	Chip disable to data retention mode	0	—	—	ns
Recovery time	t _R		t _{RC} *2	—	—	ns

*1 $\overline{CE1} \geq V_{CC} - 0.2V$ or $CE2 \leq 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$ *2 t_{RC}: Read cycle time

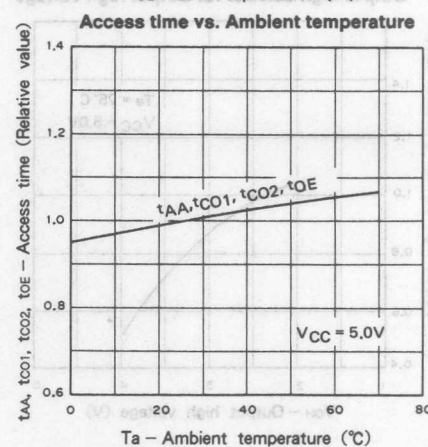
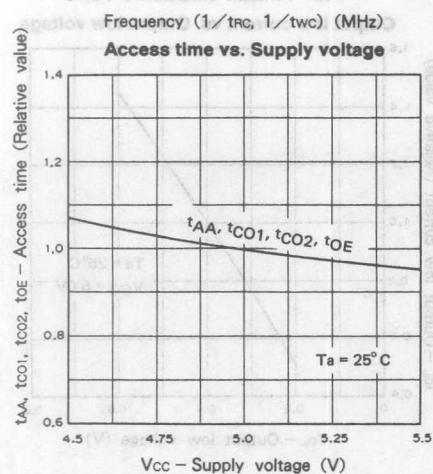
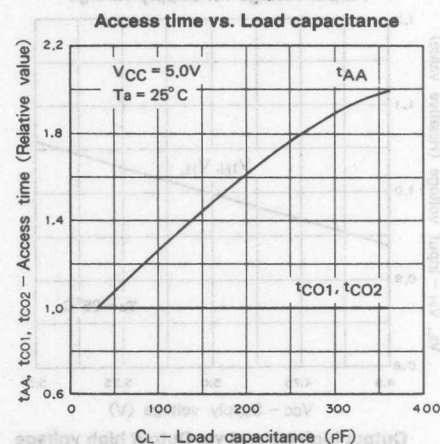
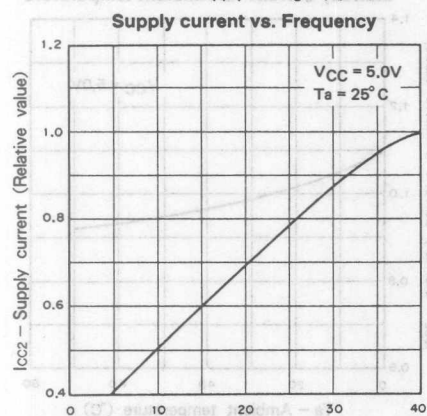
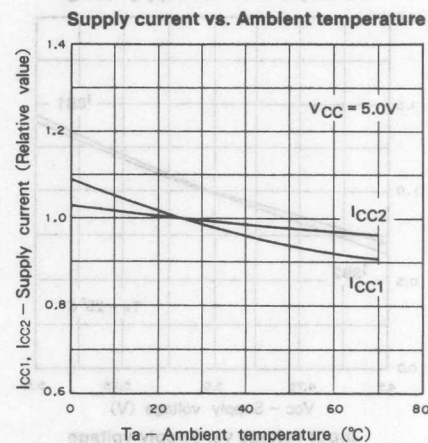
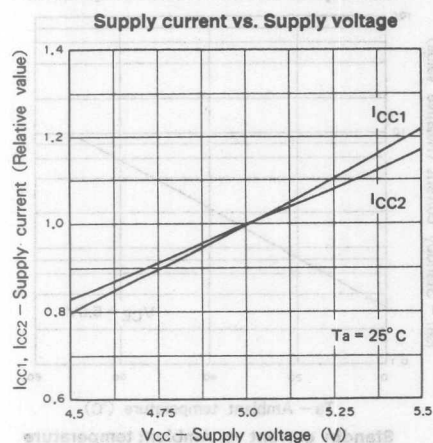
Data Retention Waveform (1) : [CE1 control]



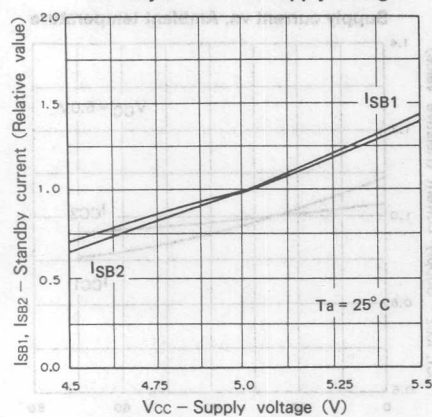
Data Retention Waveform (2) : [CE2 control]



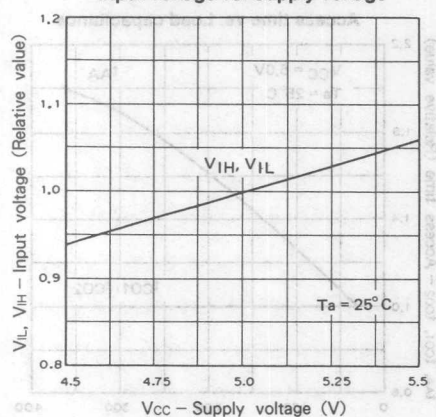
Example of Representative Characteristics



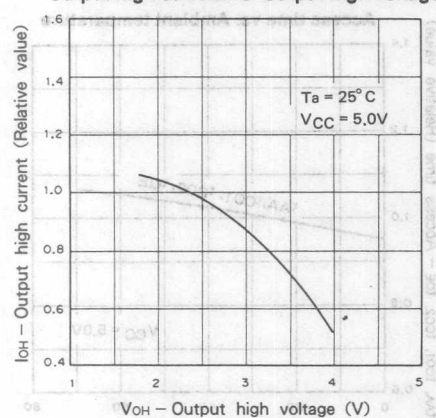
Standby current vs. Supply voltage



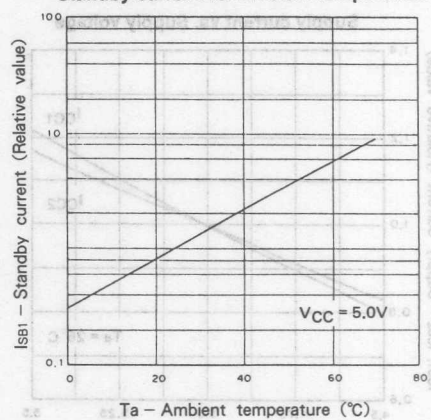
Input voltage vs. Supply voltage



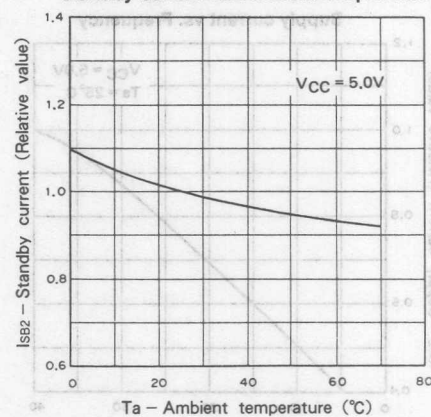
Output high current vs. Output high voltage



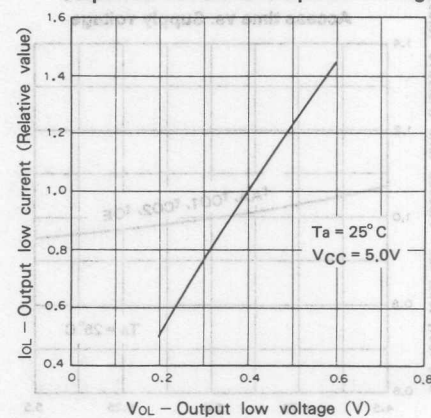
Standby current vs. Ambient temperature



Standby current vs. Ambient temperature

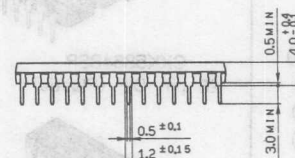
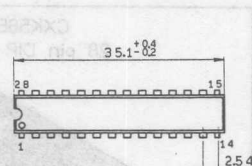


Output low current vs. Output low voltage



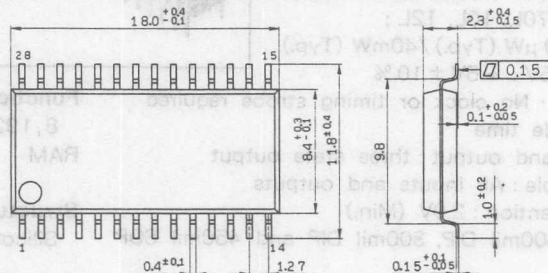
Package Outline Unit : mm

CXK5863P 28 pin DIP (Plastic) 300mil 2.0g



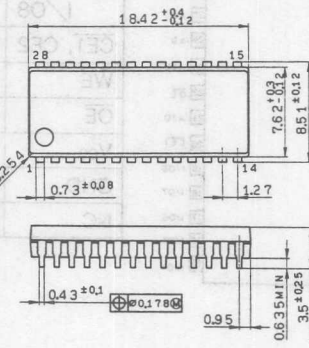
DIP-28P-06

CXK5863M 28 pin SOP (Plastic) 450mil 0.7g



SOP-28P-L05

CXK5863J 28 pin SOJ (Plastic) 300mil 0.8g



SOJ-28P-01

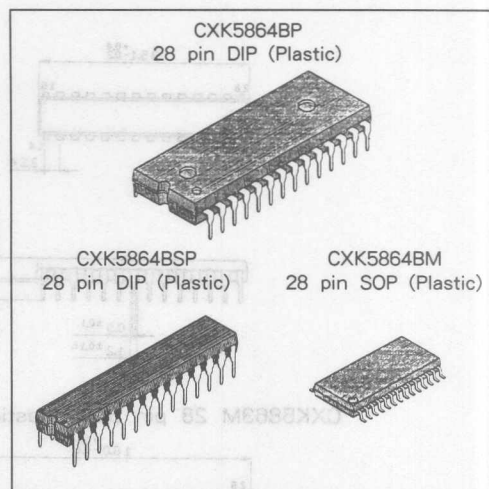
SONY
CXK5864BP/BSP/BM
**70L/10L/12L/
70LL/10LL/12LL**
8,192-word × 8-bit High Speed CMOS Static RAM

Description

CXK5864BP/BSP/BM are 65,536 bits high speed CMOS static RAMs organized as 8,192 words by 8 bits and operates from a single 5V supply. These IC are suitable for use in high speed and low power applications in which battery back up for nonvolatility is required.

Features

- Fast access time (Access time)
CXK5864BP/BSP/BM-70L, 70LL 70ns(Max.)
CXK5864BP/BSP/BM-10L, 10LL 100ns(Max.)
CXK5864BP/BSP/BM-12L, 12LL 120ns(Max.)
- Low power operation :
CXK5864BP/BSP/BM-70LL, 10LL, 12LL ;
Standby/Operation : 5 μ W (Typ.) / 40mW (Typ.)
CXK5864BP/BSP/BM-70L, 10L, 12L ;
Standby/Operation : 10 μ W (Typ.) / 40mW (Typ.)
- Single power supply 5V : +5V $\pm$ 10 %
- Fully static memory ... No clock or timing strobe required
- Equal access and cycle time
- Common data input and output : three state output
- Directly TTL compatible : All inputs and outputs
- Low voltage data retention : 2.0V (Min.)
- Available in 28 pin 600mil DIP, 300mil DIP and 450mil SOP



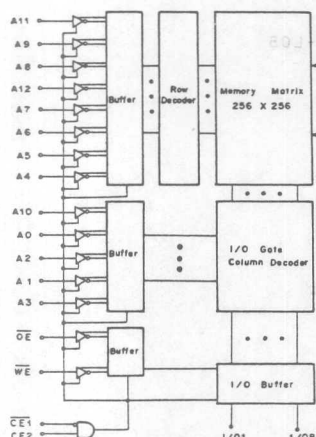
Function

8,192-word × 8-bit static RAM

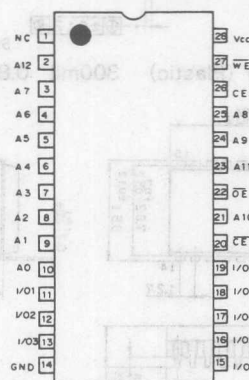
Structure

Silicon gate CMOS IC

Block Diagram



Pin Configuration (Top view)



Pin Description

Symbol	Description
A0 to A12	Address input
I/O1 to I/O8	Data input output
CE1, CE2	Chip enable 1, 2 input
WE	Write enable input
OE	Output enable input
Vcc	+ 5V Power supply
GND	Ground
NC	No connection

Absolute Maximum Ratings

(Ta = 25°C, GND = 0V)

Item	Symbol	Rating	Unit
Supply voltage	V _{CC}	- 0.5 to + 7.0	V
Input voltage	V _{IN}	- 0.5 * to V _{CC} + 0.5	V
Input and output voltage	V _{I/O}	- 0.5 * to V _{CC} + 0.5	V
Allowable power dissipation	P _D	CXK5864BP /BSP	1.0
		CXK5864BM	0.7
Operating temperature	T _{opr}	0 to + 70	°C
Storage temperature	T _{stg}	- 55 to + 150	°C
Soldering temperature • time	T _{solder}	260 • 10	°C • sec

* V_{IN}, V_{I/O} = -3.0V Min. for pulse width less than 50ns.

Truth Table

CE1	CE2	OE	WE	Mode	I/O1 to I/O8	V _{CC} Current
H	X	X	X	Not selected	High Z	I _{SB1} , I _{SB2}
X	L	X	X	Not selected	High Z	I _{SB1} , I _{SB2}
L	H	H	H	Output disable	High Z	I _{CC1} , I _{CC2}
L	H	L	H	Read	Data out	I _{CC1} , I _{CC2}
L	H	X	L	Write	Data in	I _{CC1} , I _{CC2}

X: "H" or "L"

DC Recommended Operating Conditions (Ta = 0 to +70°C, GND = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Input high voltage	V _{IH}	2.2	—	V _{CC} + 0.3	V
Input low voltage	V _{IL}	-0.3*	—	0.8	V

* V_{IL} = -3.0V Min. for pulse width less than 50ns.

Electrical Characteristics

● DC and operating characteristics

(V_{CC} = 5V ± 10%, GND = 0V, T_a = 0 to +70 °C)

Item	Symbol	Test conditions	- 70L/10L/12L - 70LL/10LL/12LL			Unit
			Min.	Typ.*	Max.	
Input leak current	I _{LI}	V _{IN} = GND to V _{CC}	- 500	—	500	nA
Output leak current	I _{LO}	V _{I/O} = GND to V _{CC} CE1 = V _{IH} or CE2 = V _{IL} or OE = V _{IH} or WE = V _{IL}	- 500	—	500	nA
Operating supply current	I _{CC1}	CE1 = V _{IL} , CE2 = V _{IH} , V _{IN} = V _{IH} or V _{IL} , I _{OUT} = 0mA	—	8	15	mA
Average operating current	I _{CC2}	Min. cycle Duty = 100 %, I _{OUT} = 0mA	—	30	50	mA
Standby current	I _{SB1}	CE2 ≤ 0.2V	- L	—	2	μA
		or { CE1 ≥ V _{CC} - 0.2V CE2 ≥ V _{CC} - 0.2V	- LL	—	1	
	I _{SB2}	CE1 = V _{IH} or CE2 = V _{IL}	—	0.1	2	mA
Output high voltage	V _{OH}	I _{OH} = - 1.0mA	2.4	—	—	V
Output low voltage	V _{OL}	I _{OL} = 2.1mA	—	—	0.4	V

* V_{CC} = 5V, T_a = 25 °C

Pin capacitance

(T_a = 25 °C, f = 1MHz)

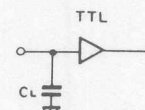
Item	Symbol	Test conditions	Min.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} = 0V	—	7	pF
Input/Output capacitance	C _{I/O}	V _{I/O} = 0V	—	7	pF

Note) This parameter is sampled and is not 100 % tested.

AC characteristics

● AC test conditions (V_{CC} = 5V ± 10%, T_a = 0 to +70 °C)

Item	Conditions
Input pulse high level	V _{IH} = 2.2V
Input pulse low level	V _{IL} = 0.8V
Input rise time	t _r = 5ns
Input fall time	t _f = 5ns
Input and output reference level	1.5V
Output load conditions	10L/10LL/12L/12LL C _L * = 100pF, 1TTL
	70L/70LL C _L * = 30pF, 1TTL

* C_L includes scope and jig capacitances.

●Read cycle

Item	Symbol	- 70L/70LL		- 10L/10LL		- 12L/12LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t _{RC}	70	—	100	—	120	—	ns
Address access time	t _{AA}	—	70	—	100	—	120	ns
Chip enable access time ($\overline{\text{CE1}}$, CE2)	t _{CO1} t _{CO2}	—	70	—	100	—	120	ns
Output enable to output valid	t _{OE}	—	35	—	50	—	60	ns
Output hold from address change	t _{OH}	10	—	10	—	10	—	ns
Chip enable to output in low Z ($\overline{\text{CE1}}$, CE2)	t _{LZ1} t _{LZ2}	10	—	10	—	10	—	ns
Output enable to output in low Z ($\overline{\text{OE}}$)	t _{OLZ}	5	—	5	—	5	—	ns
Chip disable to output in high Z ($\overline{\text{CE1}}$, CE2)	t _{HZ1} * t _{HZ2} *	0	30	0	35	0	45	ns
Output disable to output in high Z ($\overline{\text{OE}}$)	t _{OHZ} *	0	30	0	35	0	45	ns

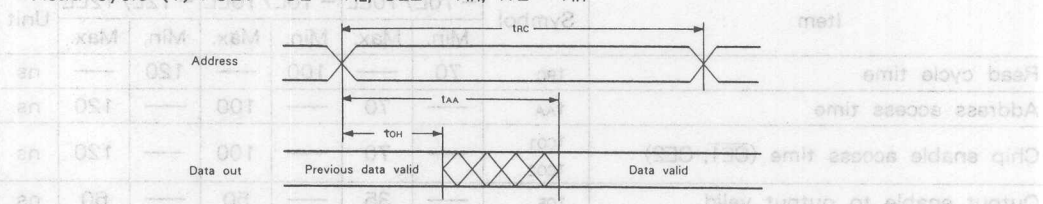
* t_{HZ1}, t_{HZ2} and t_{OHZ} are defined as the time at which the outputs become the high impedance state and are not referred to output voltage levels.

●Write cycle

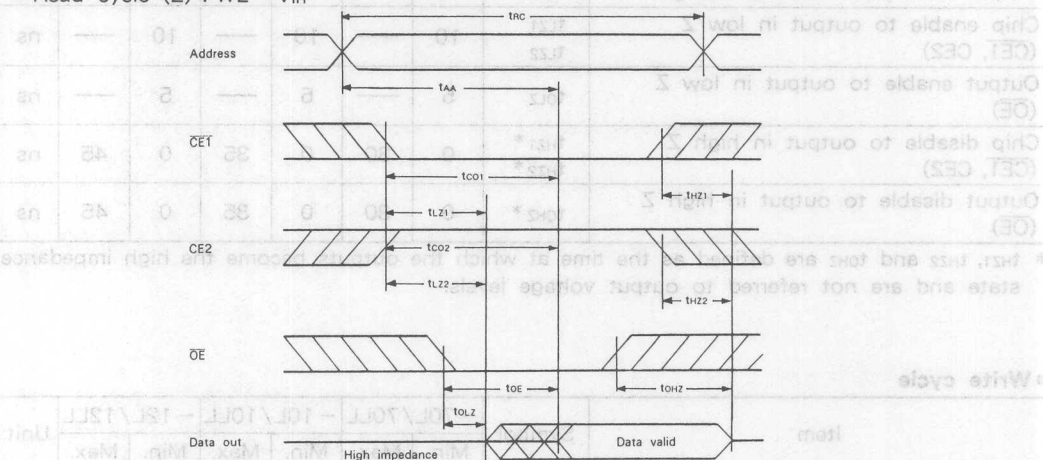
Item	Symbol	- 70L/70LL		- 10L/10LL		- 12L/12LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t _{WC}	70	—	100	—	120	—	ns
Address valid to end of write	t _{AW}	60	—	80	—	85	—	ns
Chip enable to end of write	t _{CW}	60	—	80	—	85	—	ns
Data to write time overlap	t _{DW}	30	—	35	—	50	—	ns
Data hold from write time	t _{DH}	0	—	0	—	0	—	ns
Write pulse width	t _{WP}	40	—	60	—	70	—	ns
Address setup time	t _{AS}	0	—	0	—	0	—	ns
Write recovery time ($\overline{\text{WE}}$)	t _{WR}	0	—	0	—	0	—	ns
Write recovery time ($\overline{\text{CE1}}$, CE2)	t _{WR1}	0	—	0	—	0	—	ns
Output active from end of write	t _{OW}	5	—	5	—	5	—	ns
Write to output in high Z	t _{WHZ} *	0	30	0	35	0	45	ns

* t_{WHZ} is defined as the time at which the outputs become the high impedance state and are not referred to output voltage levels.

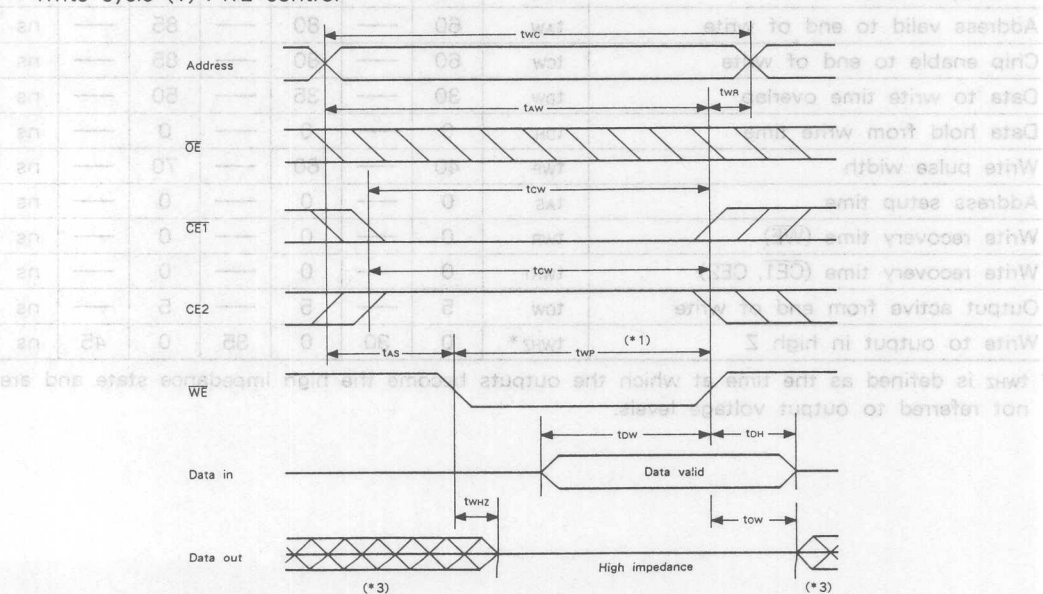
- Read cycle (1) : $\overline{CE1} = \overline{OE} = V_{IL}$, $CE2 = V_{IH}$, $\overline{WE} = V_{IH}$



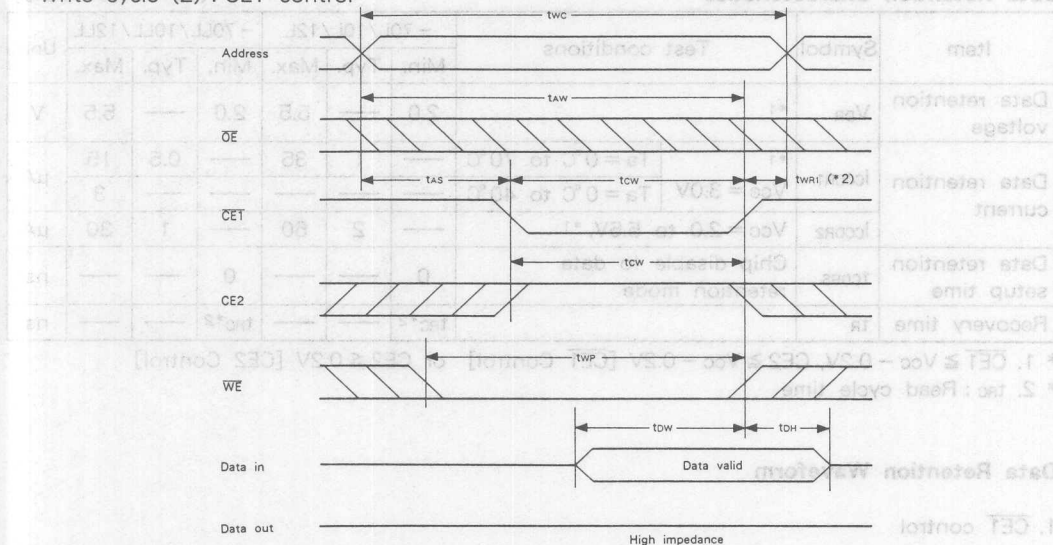
- Read cycle (2) : $\overline{WE} = V_{IH}$



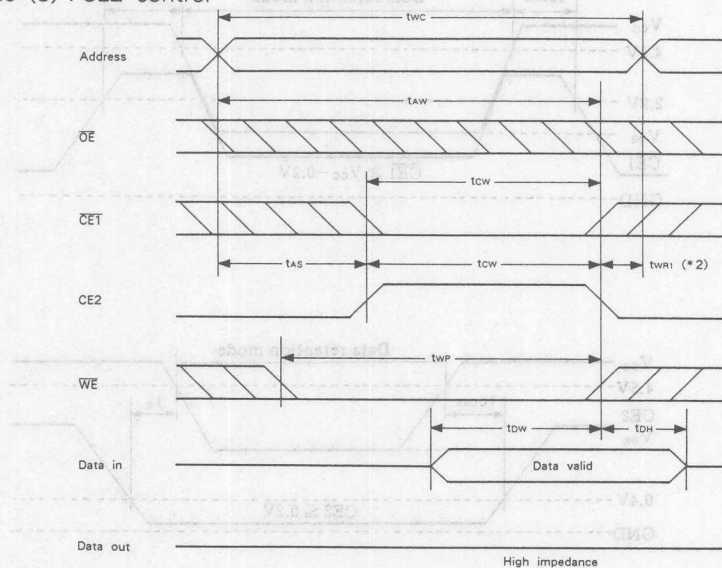
- Write cycle (1) : $\overline{WE}$ control



• Write cycle (2) : $\overline{\text{CE1}}$ control



• Write cycle (3) : CE2 control



Note)

- *1. Write is executed when both $\overline{\text{CE1}}$ and $\overline{\text{WE}}$ are at low and CE2 is at high simultaneously.
- *2. twr1 is tested from either the rising edge of $\overline{\text{CE1}}$ or the falling edge of CE2, whichever comes earlier, until the end of the write cycle.
- *3. Do not apply the data input voltage of the opposite phase to the output while the I/O pin is in output condition.

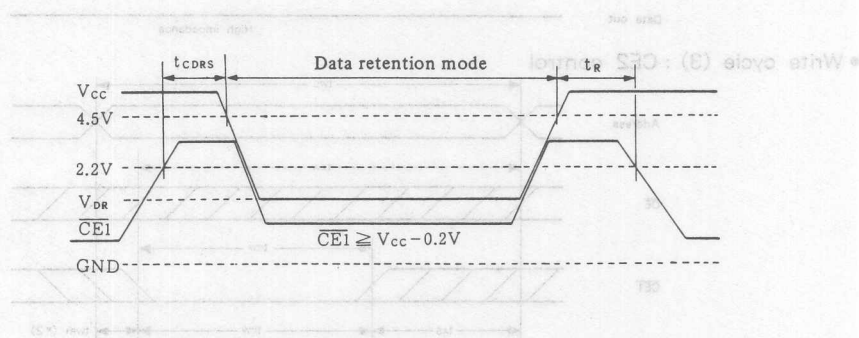
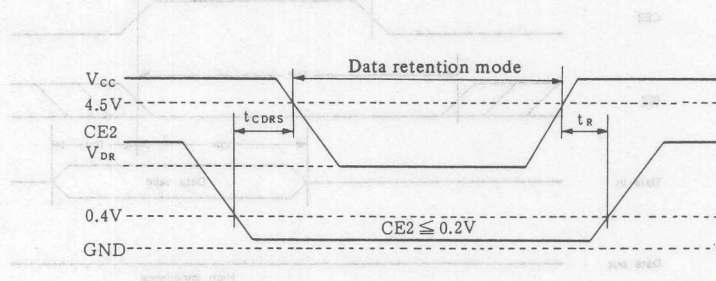
Data Retention Characteristics

(Ta = 0 to +70°C)

Item	Symbol	Test conditions	-70L/10L/12L			-70LL/10LL/12LL			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Data retention voltage	V _{DR}	*1	2.0	—	5.5	2.0	—	5.5	V
Data retention current	I _{CCDR1}	*1 Ta = 0°C to 70°C V _{CC} = 3.0V	—	1	35	—	0.5	15	μA
	I _{CCDR2}	V _{CC} = 2.0 to 5.5V, *1	—	2	60	—	1	30	μA
Data retention setup time	t _{CDRS}	Chip disable to data retention mode	0	—	—	0	—	—	ns
Recovery time	t _R		t _{RC} *2	—	—	t _{RC} *2	—	—	ns

* 1. $\overline{CE1} \geq V_{CC} - 0.2V$, $CE2 \geq V_{CC} - 0.2V$ [$\overline{CE1}$ Control] or $CE2 \leq 0.2V$ [$CE2$ Control]* 2. t_{RC}: Read cycle time

Data Retention Waveform

1. $\overline{CE1}$ control2. $CE2$ control

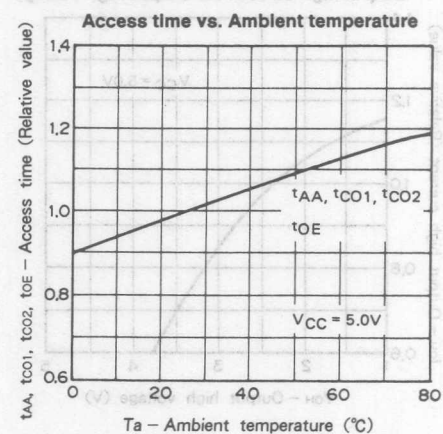
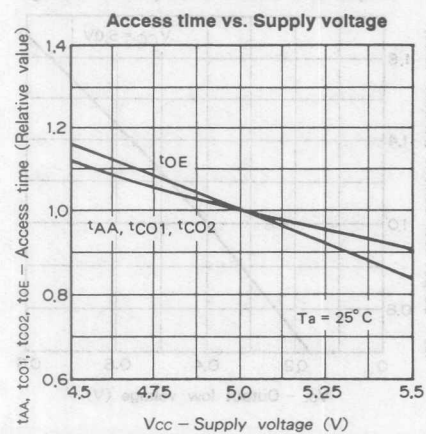
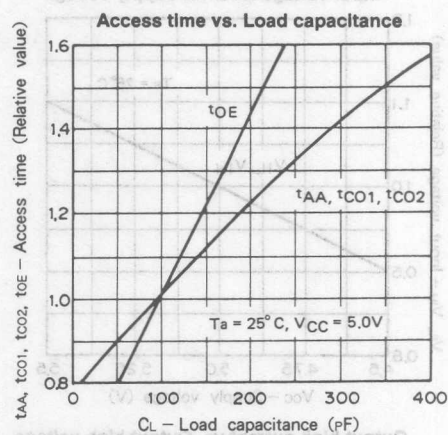
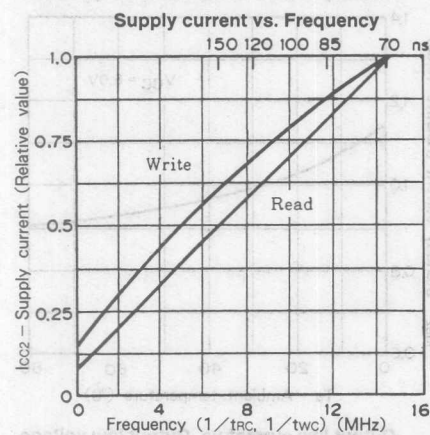
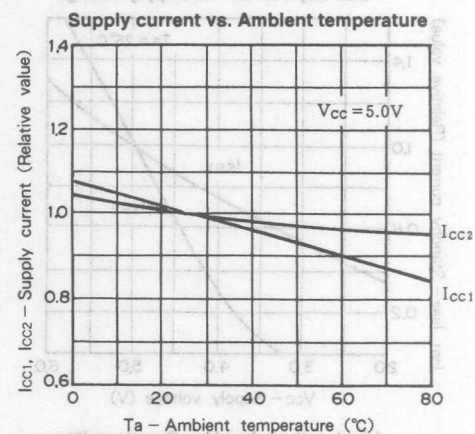
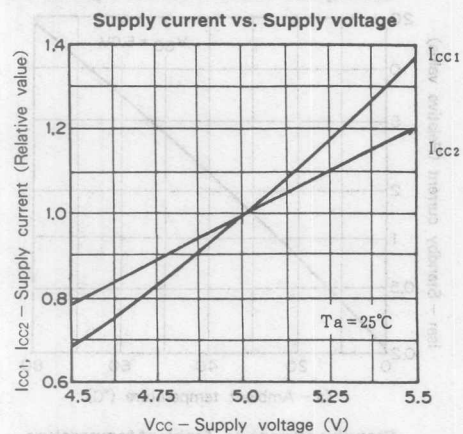
Note:

* 1. Write is executed when both $\overline{CE1}$ and $\overline{WE}$ are at low and $CE2$ is at high simultaneously.

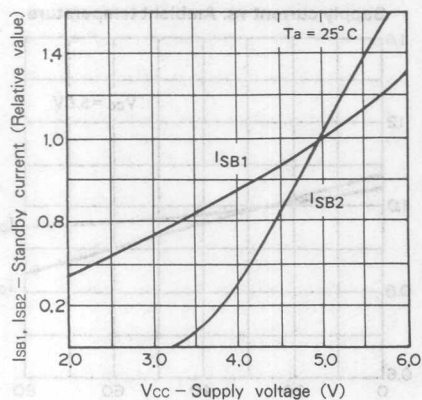
* 2. t_{RC} is tested from either the rising edge of $\overline{CE1}$ or the falling edge of $CE2$, whichever comes earlier, until the end of the write cycle.

* 3. Do not apply the data input voltage of the opposite phase to the output while the I/O pin is in output condition.

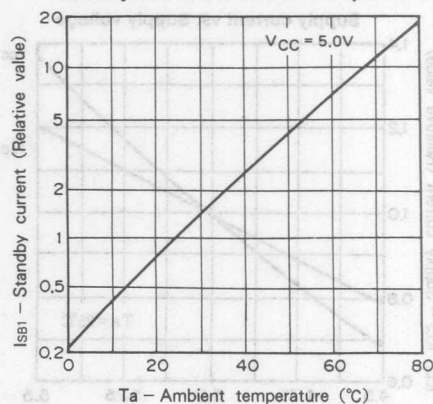
Example of Representative Characteristics



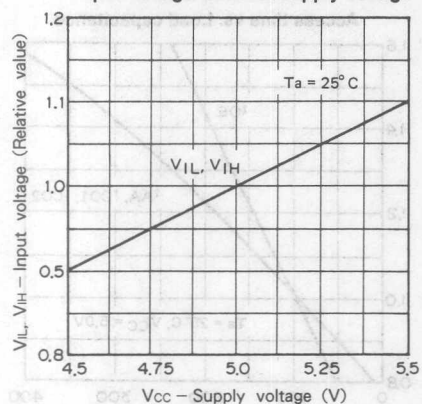
Standby current vs. Supply voltage



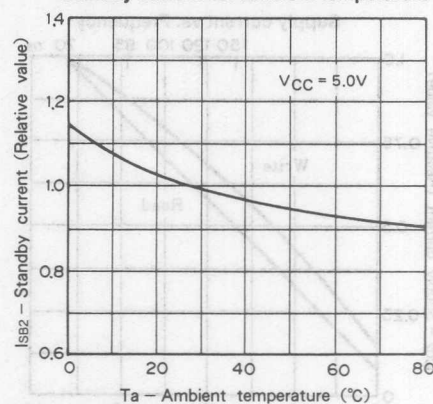
Standby current vs. Ambient temperature



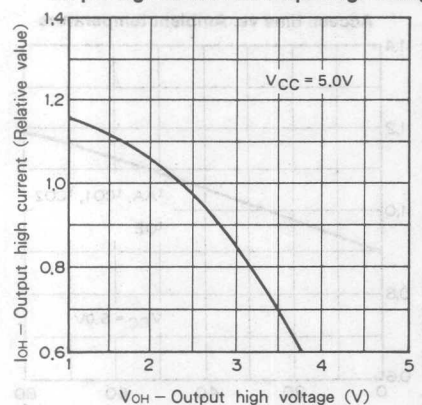
Input voltage level vs. Supply voltage



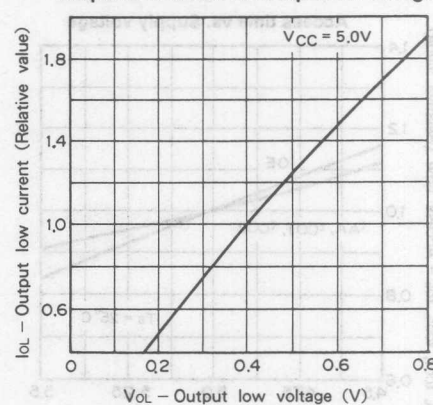
Standby current vs. Ambient temperature



Output high current vs. Output high voltage



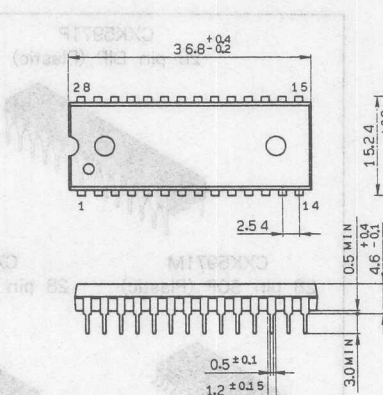
Output low current vs. Output low voltage



Package Outline Unit : mm

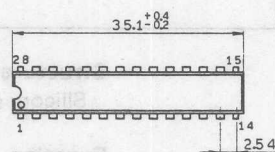
CXK5864BP

28 pin DIP (Plastic) 600mil 4.2g



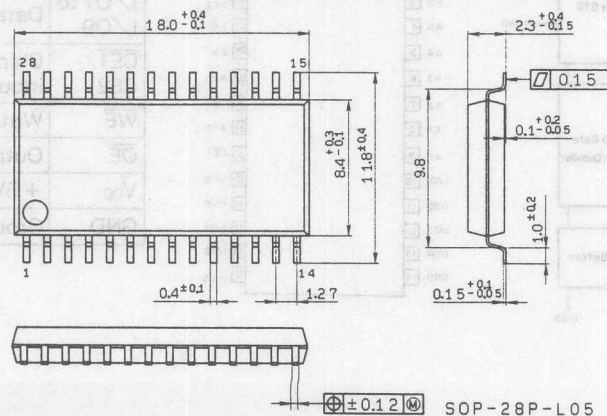
CXK5864BSP

28 pin DIP (Plastic) 300mil 2.0g



CXK5864BM

28 pin SOP (Plastic) 450mil 0.7g



SOP-28P-L05

CXK5971P
 28 pin DIP (Plastic)

CXK5971M
 28 pin SOP (Plastic)

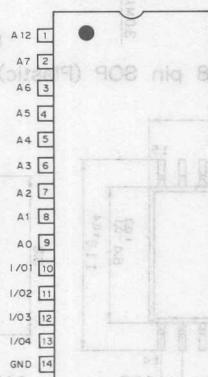
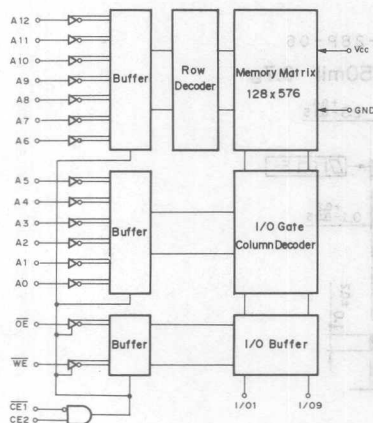
CXK5971J
 28 pin SOJ (Plastic)

- ## Structure

Silicon gate CMOS IC

8192-word X 9-bit static RAM

Pin Configuration (Top View)



Symbol	Description
A0 to A12	Address input
I/O1 to I/O9	Data input output
CE1, CE2	Chip enable 1, 2 input
WE	Write enable input
OE	Output enable input
Vcc	+ 5V Power supply
GND	Ground

Absolute Maximum Ratings

$T_a = 25^\circ\text{C}$, $\text{GND} = 0\text{V}$

Item	Symbol	Rating	Unit
Supply voltage	V_{CC}	$-0.5^* \text{ to } +7.0$	V
Input voltage	V_{IN}	$-0.5^* \text{ to } V_{CC} + 0.5$	V
Input and output voltage	$V_{I/O}$	$-0.5^* \text{ to } V_{CC} + 0.5$	V
Allowable power dissipation	P_D	1.0	W
		0.7	
Operating temperature	T_{opr}	$0 \text{ to } +70$	$^{\circ}\text{C}$
Storage temperature	T_{stg}	$-55 \text{ to } +150$	$^{\circ}\text{C}$
Soldering temperature • time	T_{solder}	$260 \cdot 10$	$^{\circ}\text{C} \cdot \text{sec}$

* **Note)** V_{CC} , V_{IN} , $V_{I/O} = -3.5V$ Min. for pulse width less than 20ns.

Truth Table

CE1	CE2	OE	WE	Mode	I/O1 to I/O9	V _{CC} Current
H	X	X	X	Not selected	High Z	IsB1, IsB2
X	L	X	X	Not selected	High Z	IsB1, IsB2
L	H	H	H	Output disable	High Z	Icc1, Icc2
L	H	L	H	Read	Data out	Icc1, Icc2
L	H	X	L	Write	Data in	Icc1, Icc2

X: "H" or "L"

DC Recommended Operating Conditions

$T_a = 0$ to $+70^{\circ}\text{C}$, GND = 0V

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Input high voltage	V _{IH}	2.2	—	V _{CC} + 0.3	V
Input low voltage	V _{IL}	− 0.3 *	—	0.8	V

* **Note)** $V_{IL} = -3.0V$ Min. for pulse width less than 20ns.

Electrical Characteristics

DC and operating characteristics

 $V_{CC} = 5V \pm 10\%$, $GND = 0V$, $T_a = 0$ to $+70^\circ C$

Item	Symbol	Test condition	-25/30/35			Unit
			Min.	Typ.*	Max.	
Input leakage current	I_{LI}	$V_{IN} = GND$ to V_{CC}	-1	—	1	μA
Output leakage current	I_{LO}	$V_{I/O} = GND$ to V_{CC} , $\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$	-1	—	1	μA
Operating power supply current	I_{CC1}	$\overline{CE1} = V_{IL}$, $CE2 = V_{IH}$, $V_{IN} = V_{IH}$ or V_{IL} , $I_{OUT} = 0mA$	—	30	60	mA
Average operating current	I_{CC2}	Cycle = Min, Duty = 100%, $I_{OUT} = 0mA$	—	60	90	mA
Standby current	I_{SB1}	$\overline{CE1} \geq V_{CC} - 0.2V$ or $CE2 \leq 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	—	1	100	μA
	I_{SB2}	$\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$, $V_{IN} = V_{IL}$ or V_{IH}	—	10	25	mA
Output high voltage	V_{OH}	$I_{OH} = -4.0mA$	2.4	—	—	V
Output low voltage	V_{OL}	$I_{OL} = 8.0mA$	—	—	0.4	V

* $V_{CC} = 5V$, $T_a = 25^\circ C$

I/O capacitance

 $T_a = 25^\circ C$, $f = 1MHz$

Item	Symbol	Test condition	Min.	Max.	Unit
Input capacitance	C_{IN}	$V_{IN} = 0V$	—	7	pF
Input/Output capacitance	$C_{I/O}$	$V_{I/O} = 0V$	—	10	pF

Note) This parameter is sampled and is not 100% tested.

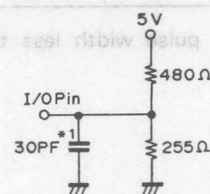
AC characteristics

● AC test conditions

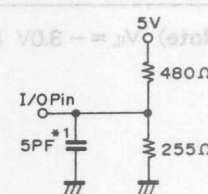
 $V_{CC} = 5V \pm 10\%$, $T_a = 0$ to $+70^\circ C$

Item	Condition
Input pulse high level	$V_{IH} = 3.0V$
Input pulse low level	$V_{IL} = 0V$
Input rise time	$t_r = 5ns$
Input fall time	$t_f = 5ns$
Input and output reference level	1.5V
Output load conditions	Fig. 1

Output Load (1)



Output Load (2)*2



* 1. including scope and jig capacitance

* 2. for t_{LZ1} , t_{LZ2} , t_{OLZ} , t_{HZ1} , t_{HZ2} , t_{OHZ} , t_{OW} , t_{WHZ}

Fig. 1

1) Read cycle

Item	Symbol	- 25		- 30		- 35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t _{RC}	25	—	30	—	35	—	ns
Address access time	t _{AA}	—	25	—	30	—	35	ns
Chip enable access time (CE1)	t _{CO1}	—	25	—	30	—	35	ns
Chip enable access time (CE2)	t _{CO2}	—	25	—	30	—	35	ns
Output enable to output valid	t _{OE}	—	15	—	15	—	20	ns
Output hold from address change	t _{OH}	5	—	5	—	5	—	ns
Chip enable to output in low Z (CE1, CE2)	t _{LEZ1} * t _{LEZ2} *	5	—	5	—	5	—	ns
Output enable to output in low Z (OE)	t _{OLZ} *	0	—	0	—	0	—	ns
Chip disable to output in high Z (CE1, CE2)	t _{HZ1} * t _{HZ2} *	0	15	0	15	0	20	ns
Chip disable to output in high Z (OE)	t _{OHZ} *	0	13	0	13	0	15	ns
Chip enable to power up time (CE1, CE2)	t _{PU}	0	—	0	—	0	—	ns
Chip disable to power down time (CE1, CE2)	t _{PD}	—	20	—	20	—	20	ns

2) Write cycle

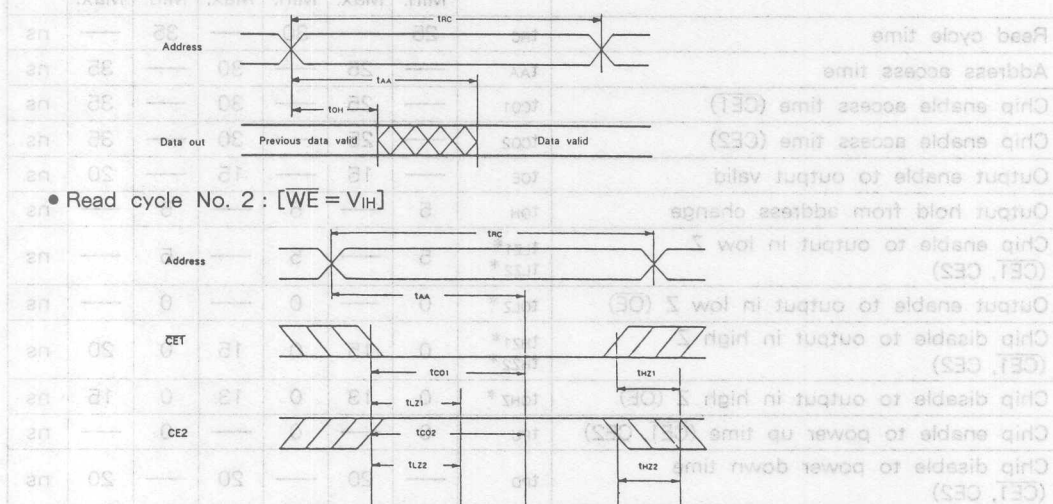
Item	Symbol	- 25		- 30		- 35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t _{WC}	25	—	30	—	35	—	ns
Address valid to end of write	t _{AW}	20	—	20	—	30	—	ns
Chip enable to end of write	t _{CW}	20	—	20	—	30	—	ns
Data to write time overlap	t _{DW}	12	—	12	—	15	—	ns
Data hold from write time	t _{DH}	0	—	0	—	0	—	ns
Write pulse width	t _{WP}	20	—	20	—	25	—	ns
Address set up time	t _{AS}	0	—	0	—	0	—	ns
Write recovery time (WE)	t _{WR}	0	—	0	—	0	—	ns
Write recovery time (CE1, CE2)	t _{WR1}	0	—	0	—	0	—	ns
Output active from end of write	t _{OW} *	5	—	5	—	5	—	ns
Write to output in high Z	t _{WHZ} *	0	13	0	13	0	15	ns

* Transition is measured $\pm 500\text{mV}$ from steady voltage with specified loading in Fig. 1-(2).
This parameter is sampled and is not 100% tested.

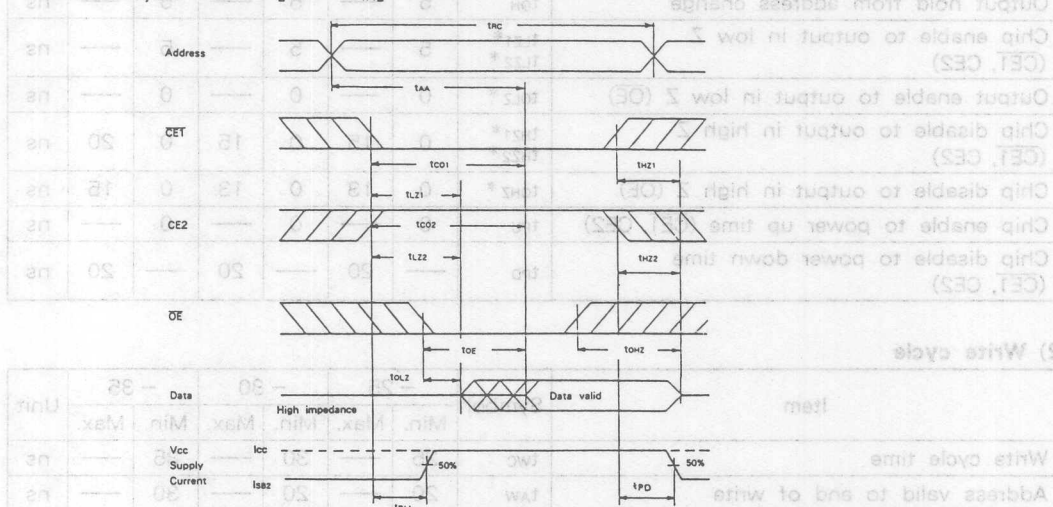
Timing Waveform

1) Read cycle

- Read cycle No. 1 : $[\overline{CE1} = \overline{OE} = V_{IL}, CE2 = V_{IH}, \overline{WE} = V_{IH}]$

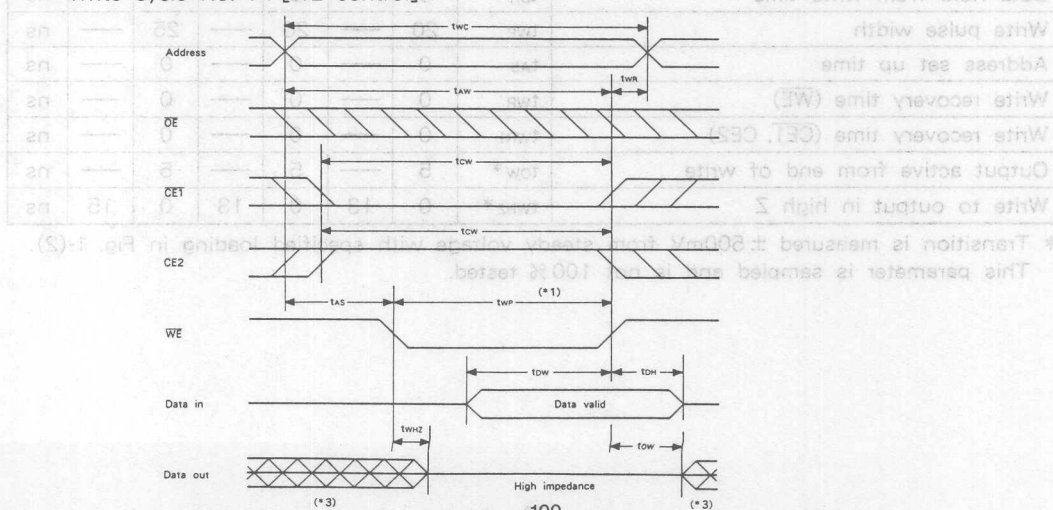


- Read cycle No. 2 : $[\overline{WE} = V_{IH}]$

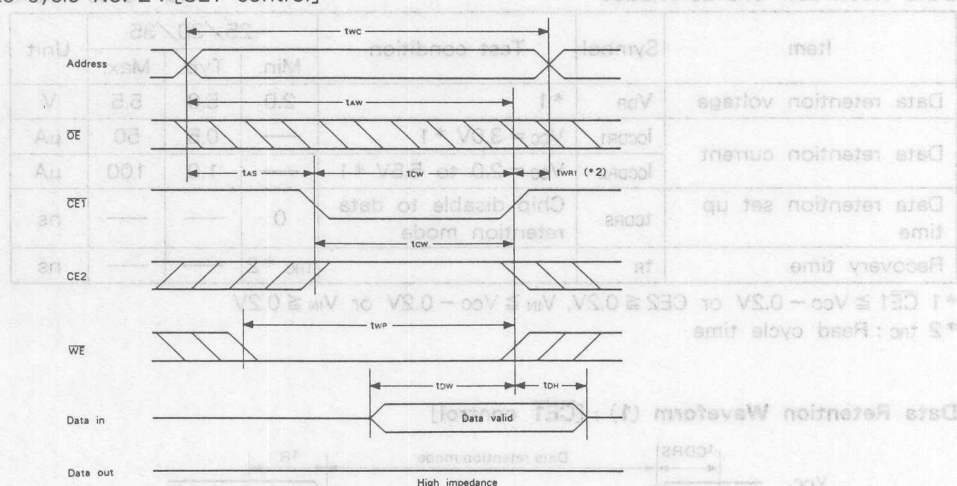


2) Write cycle

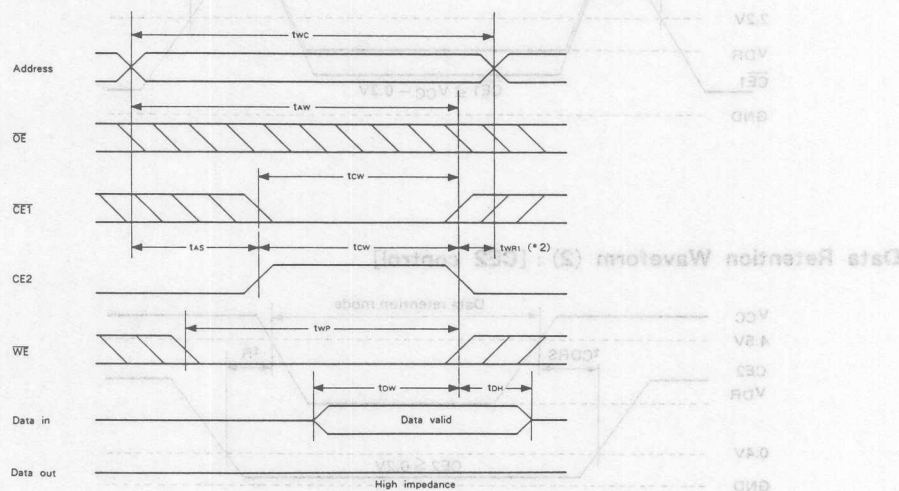
- Write cycle No. 1 : $[\overline{WE} \text{ control}]$



• Write cycle No. 2 : $\overline{\text{CE1}}$ control



• Write cycle No. 3 : $\overline{\text{CE2}}$ control



Note)

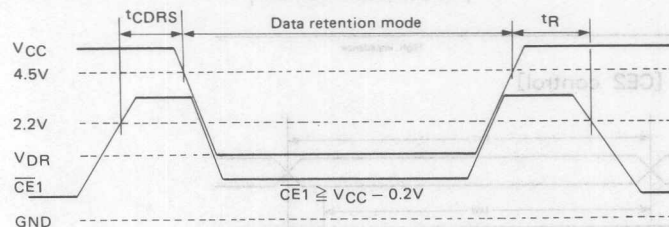
- *1. Write is executed when both $\overline{\text{CE1}}$ and $\overline{\text{WE}}$ are at low and CE2 is at high simultaneously.
- *2. twr1 is tested from either the rising edge of $\overline{\text{CE1}}$ or the falling edge of CE2, whichever comes earlier, until the end of the write cycle.
- *3. Do not apply the data input voltage of the opposite phase to the output while the I/O pin is in output condition.

Item	Symbol	Test condition	- 25/30/35			Unit
			Min.	Typ.	Max.	
Data retention voltage	V_{DR}	*1	2.0	5.0	5.5	V
Data retention current	I_{CCDR1}	$V_{CC} = 3.0V$ *1	—	0.5	50	μA
	I_{CCDR2}	$V_{CC} = 2.0$ to $5.5V$ *1	—	1.0	100	μA
Data retention set up time	t_{CDRS}	Chip disable to data retention mode	0	—	—	ns
Recovery time	t_R		t_{RC} *2	—	—	ns

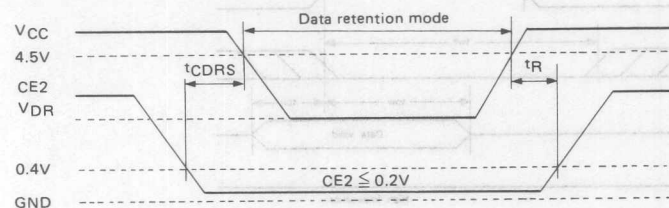
*1 $\overline{CE1} \geq V_{CC} - 0.2V$ or $CE2 \leq 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$

*2 t_{RC} : Read cycle time

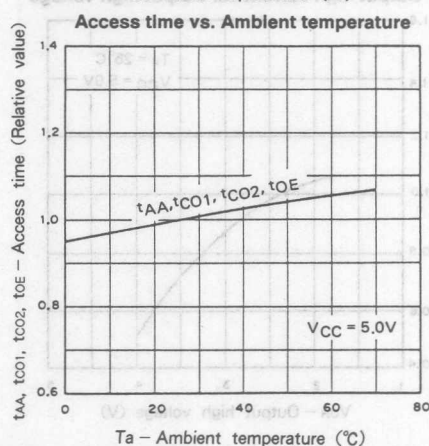
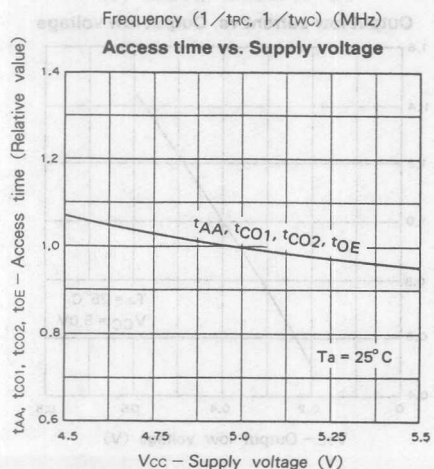
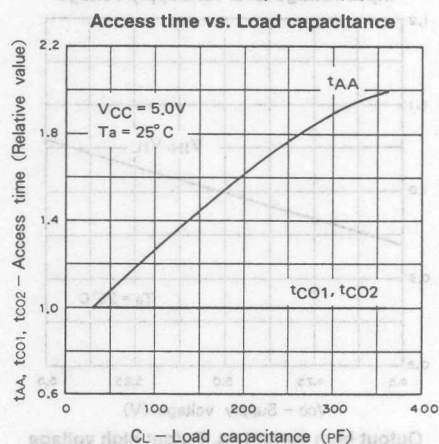
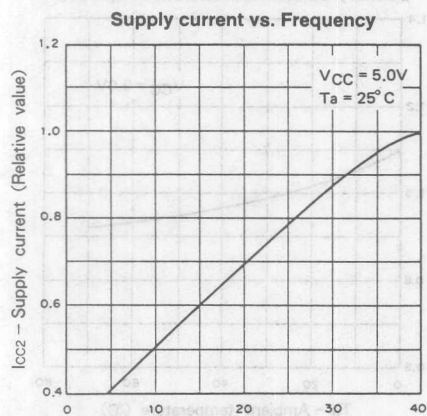
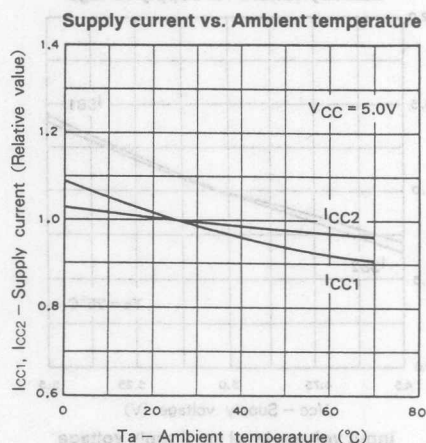
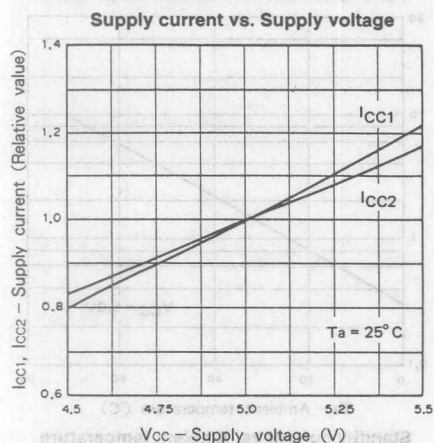
Data Retention Waveform (1) : [$\overline{CE1}$ control]



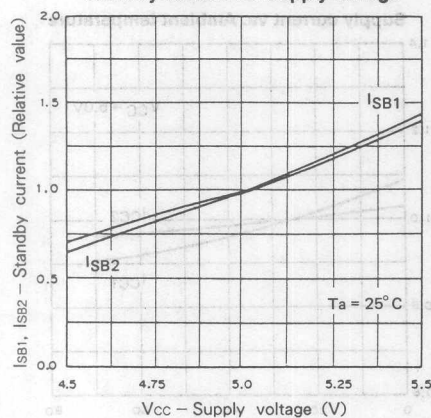
Data Retention Waveform (2) : [$CE2$ control]



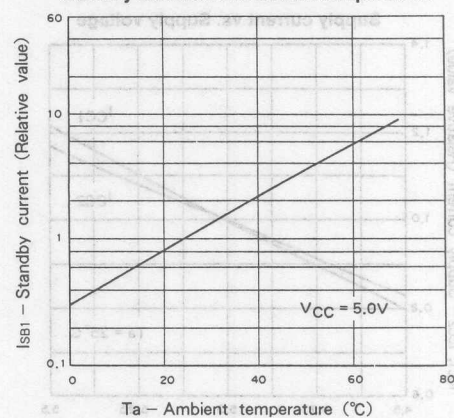
Example of Representative Characteristics



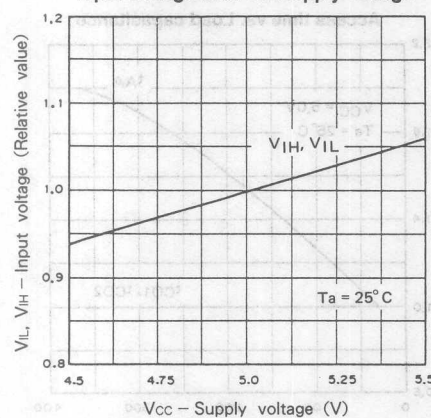
Standby current vs. Supply voltage



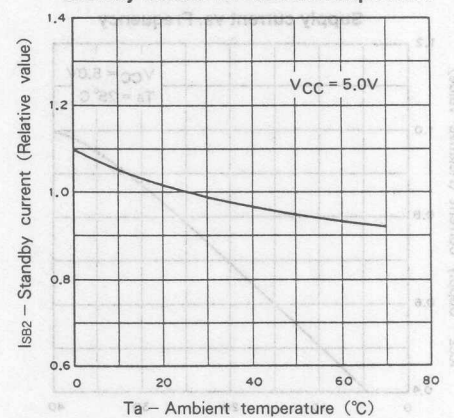
Standby current vs. Ambient temperature



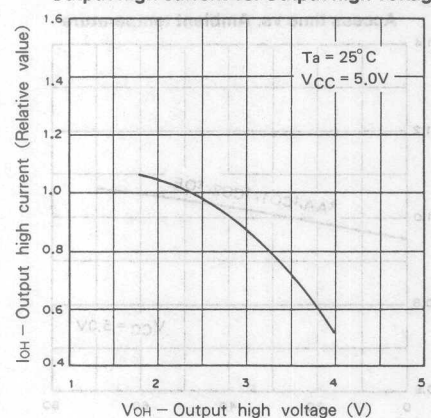
Input voltage level vs. Supply voltage



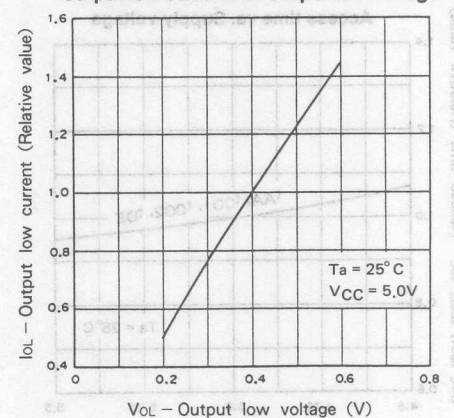
Standby current vs. Ambient temperature



Output high current vs. Output high voltage

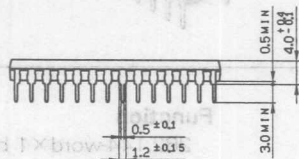
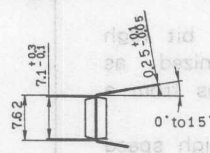
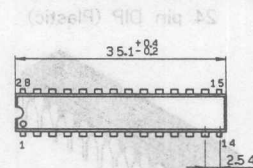


Output low current vs. Output low voltage



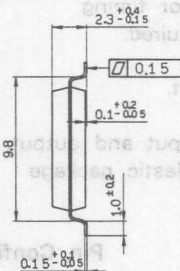
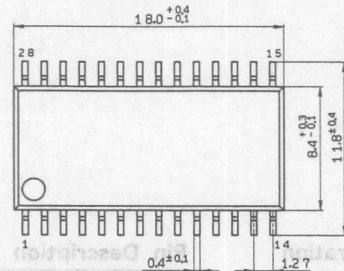
Package Outline Unit : mm

CXK5971P 28 pin DIP (Plastic) 300mil 2.0g



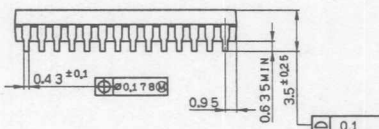
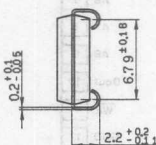
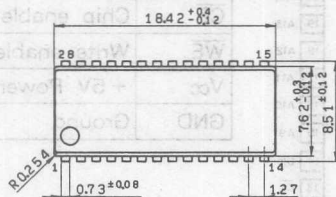
DIP-28P-06

CXK5971M 28 pin SOP (Plastic) 450mil 0.7g



SOP-28P-L05

CXK5971J 28 pin SOJ (Plastic) 300mil 0.8g



SOJ-28P-01

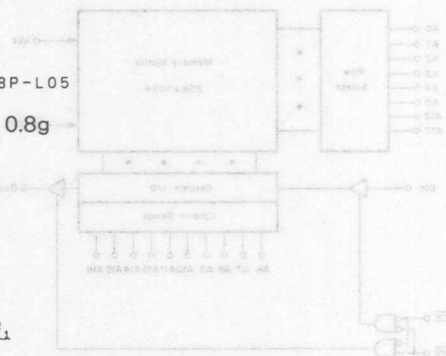
105

Description
CXK51256P is 285,144-word x 1 bit high speed CMOS static RAM organized as 285,144-word by 1 bit and operates at single 5V supply. This device is suitable for use in high speed and low power applications.

Features
• Fast access time (Access time)
CXK51256P-35 35ns (Max.)
CXK51256P-45 45ns (Max.)
CXK51256P-55 55ns (Max.)
• Low power consumption (operation)
100mW (Typ.)

• Single +5V supply: $5V \pm 10\%$
• Fully static memory. No clock or strobe required.
• Equal access and cycle time.
• Separate data input and output.
• Tri-state output.
• Directly TTL compatible: All input and output.
• High density: 300mil 28 pin plastic package.

Block Diagram



Description

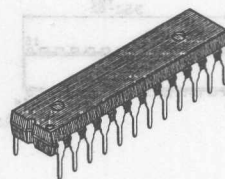
CXK51256P is 262,144-word × 1 bit high speed CMOS static RAM organized as 262,144-word by 1 bit and operates from a single 5V supply.

This device is suitable for use in high speed and low power applications.

Features

- Fast access time (Access time)
CXK51256P-35 35ns (Max.)
CXK51256P-45 45ns (Max.)
CXK51256P-55 55ns (Max.)
- Low power consumption (operation) :
100mW (Typ.)
- Single + 5V supply : $5V \pm 10\%$
- Fully static memory...No clock or timing strobe required.
- Equal access and cycle time.
- Separate data input and output.
- Three-state output.
- Directly TTL compatible : All input and output.
- High density : 300mil 24 pin plastic package

24 pin DIP (Plastic)



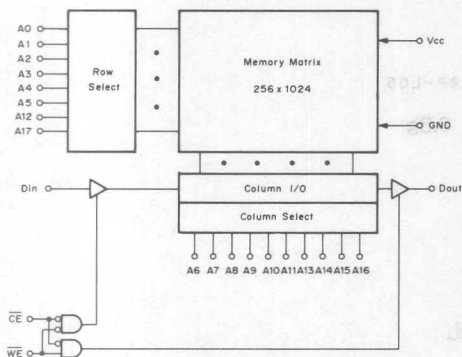
Function

262,144-word × 1 bit static RAM

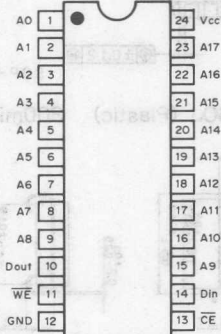
Structure

Silicon gate CMOS IC

Block Diagram



Pin Configuration (Top View)



Pin Description

Symbol	Description
A0 to A17	Address input
Din	Data input
Dout	Data output
CE	Chip enable input
WE	Write enable input
Vcc	+ 5V Power supply
GND	Ground

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply voltage	V_{CC}	-0.5^* to $+7.0$	V
Input voltage	V_{IN}	-0.5^* to $V_{CC} + 0.5$	V
Voltage applied to output	V_{OUT}	-0.5^* to $V_{CC} + 0.5$	V
Allowable power dissipation	P_D	1.0	W
Operating temperature	T_{opr}	0 to $+70$	$^{\circ}\text{C}$
Storage temperature	T_{stg}	-55 to $+150$	$^{\circ}\text{C}$
Soldering temperature	T_{solder}	260 ± 10	$^{\circ}\text{C} \cdot \text{sec}$

* **Note)** V_{CC} , V_{IN} , V_{OUT} min = -3.5V for pulse width less than 20ns.

Truth Table

$\overline{\text{CE}}$	$\overline{\text{WE}}$	Mode	Data out	V_{CC} Current
H	X	Not selected	High Z	I_{SB1} , I_{SB2}
L	H	Read	Data out	I_{CC1} , I_{CC2}
L	L	Write	High Z	I_{CC1} , I_{CC2}

X: "H" or "L"

DC Recommended Operating Conditions $T_a = 0$ to $+70^{\circ}\text{C}$, $\text{GND} = 0\text{V}$

Item	Symbol	Min.	Typ.*1	Max.	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input high voltage	V_{IH}	2.2	—	$V_{CC} + 0.3$	V
Input low voltage	V_{IL}	-0.3^{*2}	—	0.8	V

Note) *1. $V_{CC} = 5\text{V}$, $T_a = 25^{\circ}\text{C}$

*2. V_{IL} min = -3.0V for pulse width less than 20ns.

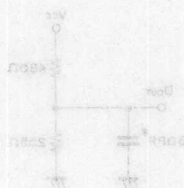
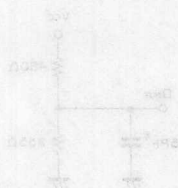


Fig. 1

Condition	Item
$V_{IH} = 3.0\text{V}$	Input pulse high level
$V_{IL} = 0\text{V}$	Input pulse low level
$t_R = 5\text{ns}$	Input rise time
$t_F = 5\text{ns}$	Input fall time
1.5V	Input and output timing reference level
Fig. 1	Output load

Electrical Characteristics

DC and operating characteristics

 $V_{CC} = 5V \pm 10\%$, $GND = 0V$, $T_a = 0$ to $+70^\circ C$

Item	Symbol	Test condition	- 35/45/55			Unit
			Min.	Typ.	Max.	
Input leakage current	I_{LI}	$V_{IN} = GND$ to V_{CC} $V_{CC} = 5.5V$	-1	—	1	μA
Output leakage current	I_{LO}	$\overline{CE} = V_{IH}$, $V_{OUT} = GND$ to V_{CC}	-1	—	1	μA
Operating power supply current	I_{CC1}	$\overline{CE} = V_{IL}$, $I_{OUT} = 0mA$, $V_{IN} = V_{IH}/V_{IL}$	—	20	45	mA
Average operating current	I_{CC2}	Cycle = Min, Duty = 100 % $I_{OUT} = 0mA$	—	55	85	mA
Standby current	I_{SB1}	$\overline{CE} \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	—	—	2	mA
	I_{SB2}	$\overline{CE} = V_{IH}$	—	15	30	mA
Output high voltage	V_{OH}	$I_{OH} = -4.0mA$	2.4	—	—	V
Output low voltage	V_{OL}	$I_{OL} = 8.0mA$	—	—	0.4	V

I/O capacitance

 $T_a = 25^\circ C$, $f = 1MHz$

Item	Symbol	Test condition	Min.	Max.	Unit
Input capacitance	C_{IN}	$V_{IN} = 0V$	—	7	pF
Output capacitance	C_{OUT}	$V_{OUT} = 0V$	—	7	pF

Note) This parameter is sampled and is not 100% tested.

AC characteristics

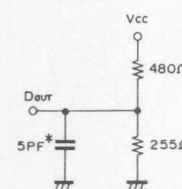
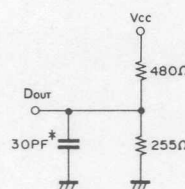
● AC test conditions

 $V_{CC} = 5V \pm 10\%$, $T_a = 0$ to $+70^\circ C$

Item	Condition
Input pulse high level	$V_{IH} = 3.0V$
Input pulse low level	$V_{IL} = 0V$
Input rise time	$t_R = 5ns$
Input fall time	$t_F = 5ns$
Input and output timing reference level	1.5V
Output load	Fig. 1

Output Load (1)

Output Load (2)**



* Including scope and jig
 ** For t_{LZ} , t_{HZ} , t_{OW} , t_{WHZ}

Fig. 1

Read cycle

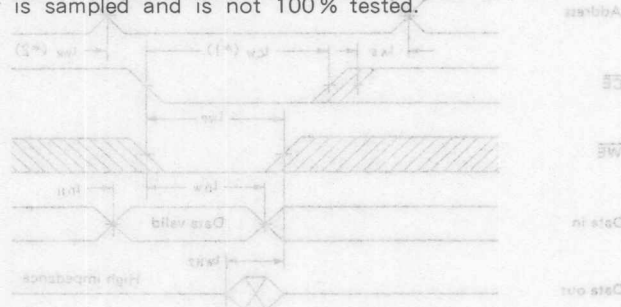
Item	Symbol	- 35		- 45		- 55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t _{RC}	35	—	45	—	55	—	ns
Address access time	t _{AA}	—	35	—	45	—	55	ns
Chip enable access time (CE)	t _{CO}	—	35	—	45	—	55	ns
Output hold from address change	t _{OH}	5	—	5	—	5	—	ns
Chip enable to output in low Z (CE)	t _{LZ} *	5	—	5	—	5	—	ns
Chip disable to output in high Z	t _{HZ} *	0	20	0	20	0	25	ns
Chip enable to power up time	t _{PU}	0	—	0	—	0	—	ns
Chip disable to power down time	t _{PD}	—	30	—	30	—	30	ns

* **Note)** Transition is measured $\pm 200\text{mV}$ from steady voltage with specified loading in Fig. 1.
This parameter is sampled and is not 100% tested.

Write cycle

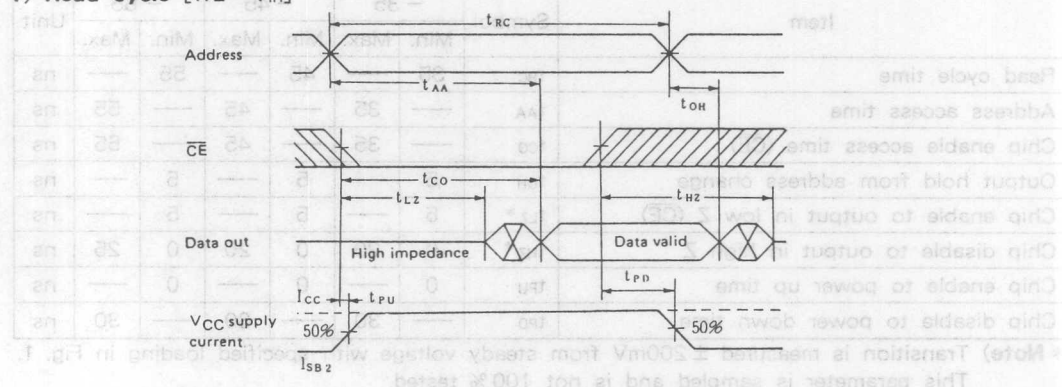
Item	Symbol	- 35		- 45		- 55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t _{WC}	35	—	45	—	55	—	ns
Address valid to end of write	t _{AW}	30	—	35	—	45	—	ns
Chip enable to end of write	t _{CW}	30	—	35	—	45	—	ns
Data to write time overlap	t _{DW}	20	—	25	—	25	—	ns
Data hold from write time	t _{DH}	0	—	0	—	0	—	ns
Write pulse width	t _{WP}	25	—	25	—	35	—	ns
Address setup time	t _{AS}	0	—	0	—	0	—	ns
Write recovery time	t _{WR}	0	—	0	—	0	—	ns
Output active from end of write	t _{OW} *	5	—	5	—	5	—	ns
Write to output in high Z	t _{WHZ} *	0	20	0	20	0	25	ns

* **Note)** Transition is measured $\pm 200\text{mV}$ from steady voltage with specified loading in Fig. 1.
This parameter is sampled and is not 100% tested.

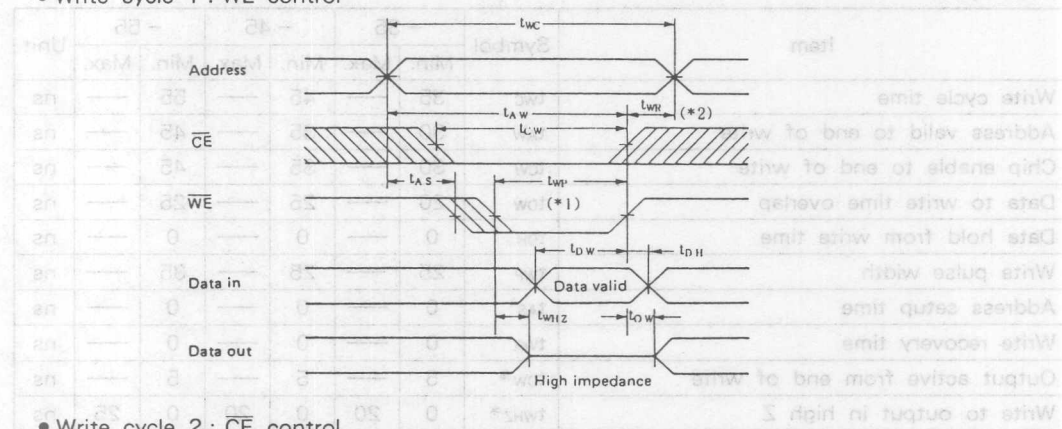
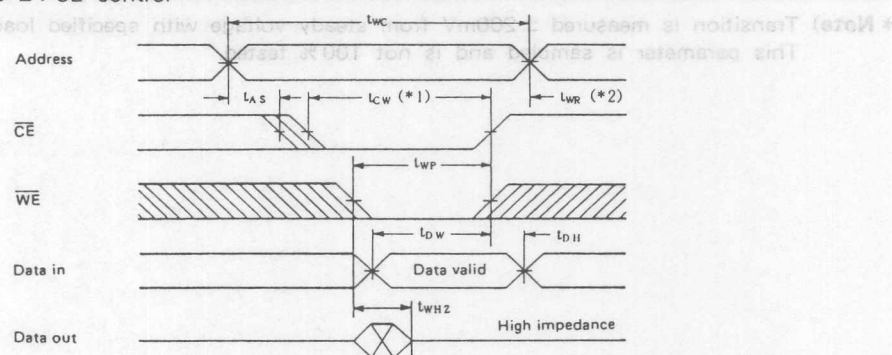


* **Note)**
1. A write occurs during the low overlap of CE and WE.
2. t_{WHZ} is measured from the earlier of CE or WE going high to the end of write cycle.

Timing Waveform

1) Read cycle [$\overline{WE} = V_{IH}$]

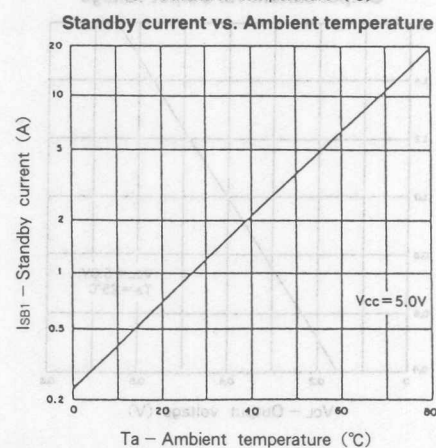
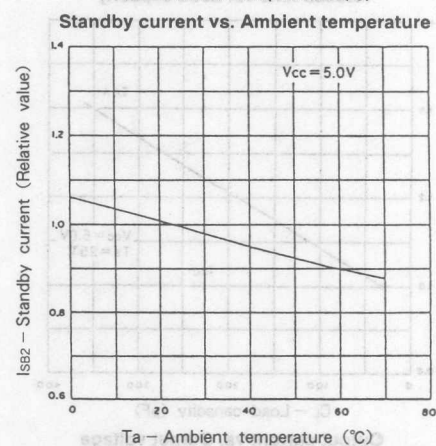
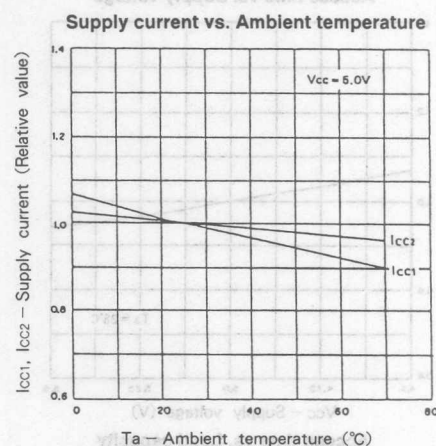
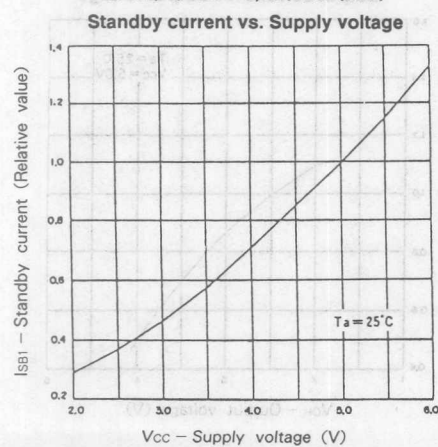
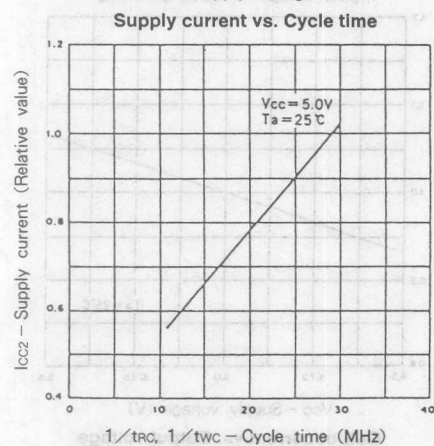
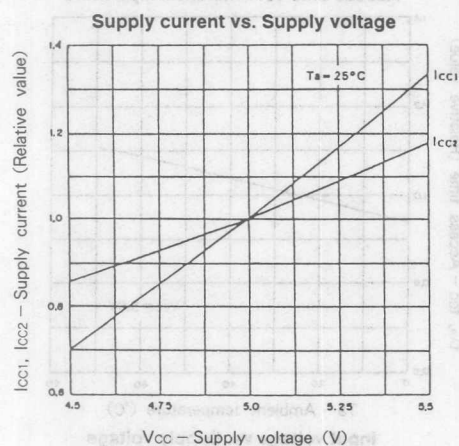
2) Write cycle

• Write cycle 1 : $\overline{WE}$ control• Write cycle 2 : $\overline{CE}$ control

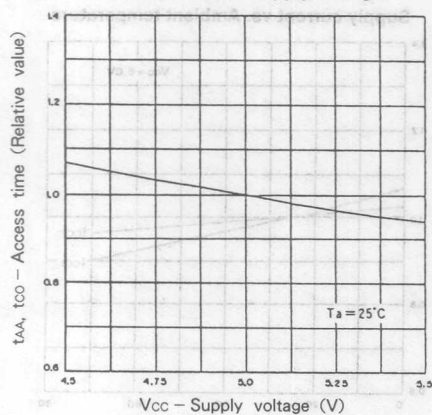
* Note)

1. A write occurs during the low overlap of $\overline{CE}$ and $\overline{WE}$.
2. t_{WR} is measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high to the end of write cycle.

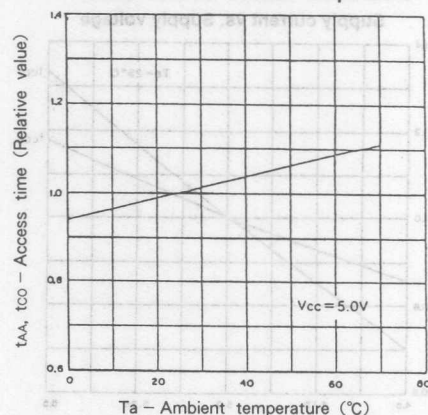
Example of Representative Characteristics



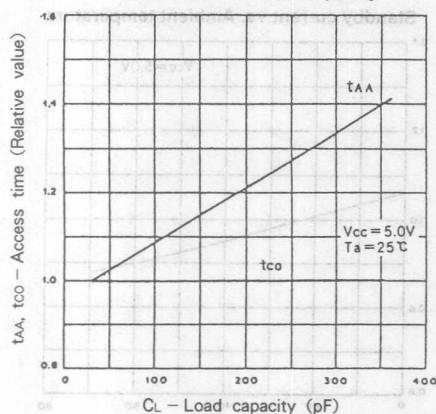
Access time vs. Supply voltage



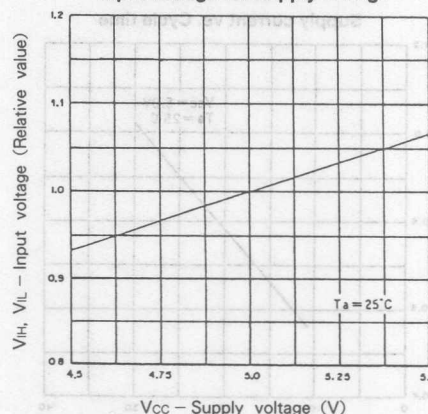
Access time vs. Ambient temperature



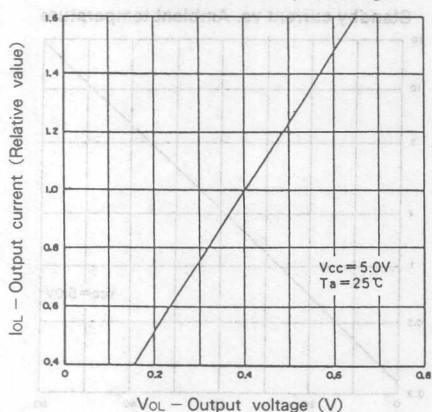
Access time vs. Load capacity



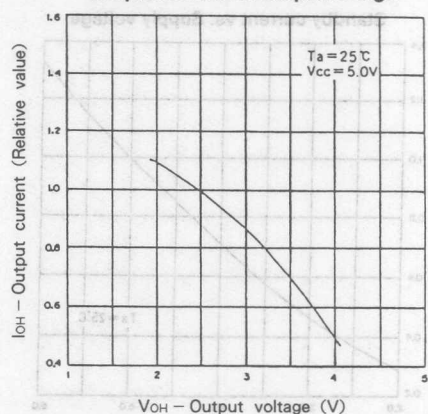
Input voltage vs. Supply voltage



Output current vs. Output voltage



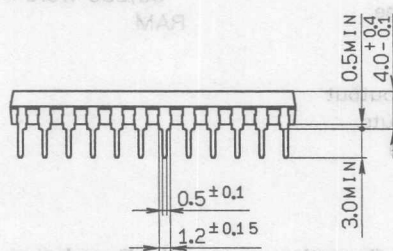
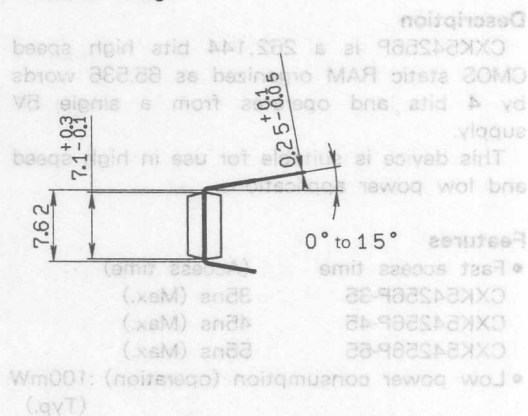
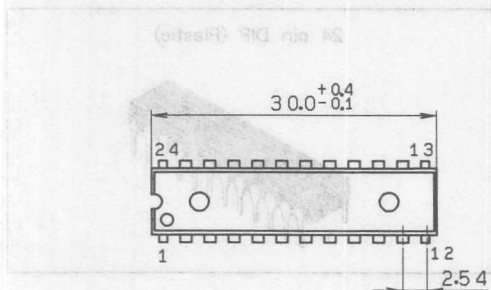
Output current vs. Output voltage



Package Outline

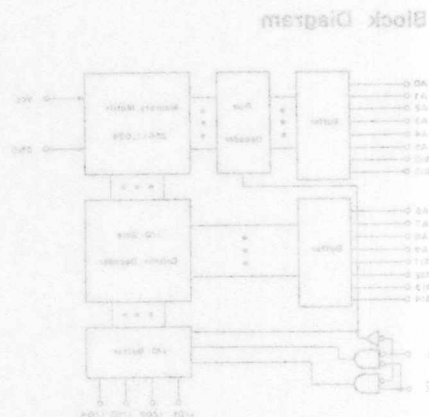
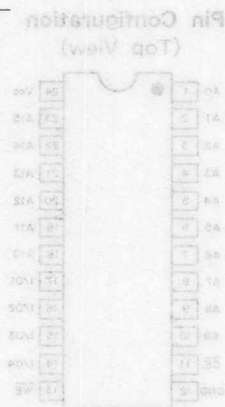
Unit : mm

24 pin DIP (Plastic) 300mil 1.5g



DIP-24P-08

Symbol	Description
A0 to A15	Address input
D0 to D15	Data input/output
OE	Chip enable input
WE	Write enable input
Vcc	+5V power supply
GND	Ground



65,536-word × 4-bit High Speed CMOS Static RAM

Description

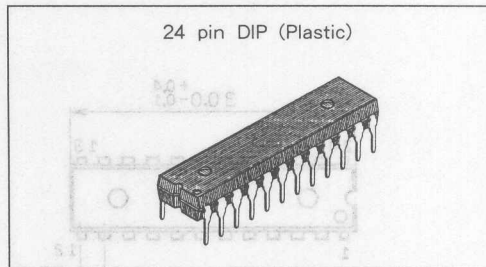
CXK54256P is a 262,144 bits high speed CMOS static RAM organized as 65,536 words by 4 bits and operates from a single 5V supply.

This device is suitable for use in high speed and low power applications.

Features

- Fast access time (Access time)
CXK54256P-35 35ns (Max.)
CXK54256P-45 45ns (Max.)
CXK54256P-55 55ns (Max.)
- Low power consumption (operation) :100mW (Typ.)
- Single + 5V supply : $5V \pm 10\%$
- Fully static memory...No clock or timing strobe required.
- Equal access and cycle time.
- Common data input and output : three-state output
- Directly TTL compatible : All inputs and outputs.
- High density : 300 mil 24 pin plastic package

24 pin DIP (Plastic)



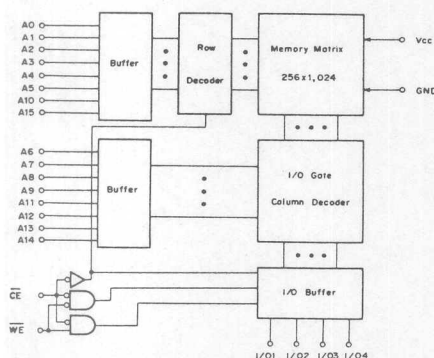
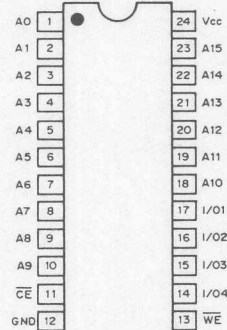
Structure

Silicon gate CMOS IC

Function

65,536-word × 4-bit static RAM

Block Diagram

Pin Configuration
(Top View)

Pin Description

Symbol	Description
A0 to A15	Address input
I/O1 to I/O4	Data input output
CE	Chip enable input
WE	Write enable input
Vcc	+ 5V power supply
GND	Ground

Absolute Maximum Ratings

(Ta = 25 °C, GND = 0V)

Item	Symbol	Rating	Unit
Supply voltage	V _{CC}	- 0.5* to + 7.0	V
Input voltage	V _{IN}	- 0.5* to V _{CC} + 0.5	V
Input and output voltage	V _{I/O}	- 0.5* to V _{CC} + 0.5	V
Allowable power dissipation	P _D	1.0	W
Operating temperature	T _{opr}	0 to + 70	°C
Storage temperature	T _{stg}	- 55 to + 150	°C
Soldering temperature • time	T _{solder}	260 • 10	°C • sec

*Note) V_{CC}, V_{IN}, V_{I/O} = - 3.5V Min. for pulse width less than 20ns.

Truth Table

$\overline{CE}$	$\overline{WE}$	Mode	I/O1 to I/O4	V _{CC} Current
H	X	Not selected	High Z	I _{sa1} , I _{sa2}
L	H	Read	Data out	I _{cc1} , I _{cc2}
L	L	Write	Data in	I _{cc1} , I _{cc2}

X: "H" or "L"

DC Recommended Operating Conditions

(Ta = 0 to + 70 °C, GND = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Input high voltage	V _{IH}	2.2	—	V _{CC} + 0.3	V
Input low voltage	V _{IL}	- 0.3*	—	0.8	V

*Note) V_{IL} = - 3.0V Min. for pulse width less than 20ns.

Electrical Characteristics

•DC and operating characteristics ($V_{CC} = 5V \pm 10\%$, $GND = 0V$, $T_a = 0$ to $+70^\circ C$)

Item	Symbol	Test condition	-35/45/55			Unit
			Min.	Typ.*	Max.	
Input leak current	I_{LI}	$V_{IN} = GND$ to V_{CC} $V_{CC} = 5.5V$	-1	—	1	μA
Output leak current	I_{LO}	$\overline{CE} = V_{IH}$ $V_{I/O} = GND$ to V_{CC}	-1	—	1	μA
Operating power supply current	I_{CC1}	$\overline{CE} = V_{IL}$, $I_{OUT} = 0mA$ $V_{IN} = V_{IH}/V_{IL}$	—	20	45	mA
Average operating current	I_{CC2}	Cycle = Min, Duty = 100 % $I_{OUT} = 0mA$	—	55	85	mA
Standby current	I_{SB1}	$\overline{CE} \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	—	—	2	mA
	I_{SB2}	$\overline{CE} = V_{IH}$	—	15	30	mA
Output high voltage	V_{OH}	$I_{OH} = -4.0mA$	2.4	—	—	V
Output low voltage	V_{OL}	$I_{OL} = 8.0mA$	—	—	0.4	V

* $V_{CC} = 5V$, $T_a = 25^\circ C$

I/O capacitance

($T_a = 25^\circ C$, $f = 1MHz$)

Item	Symbol	Test condition	Min.	Max.	Unit
Input capacitance	C_{IN}	$V_{IN} = 0V$	—	7	pF
Input/Output capacitance	$C_{I/O}$	$V_{I/O} = 0V$	—	7	pF

Note) This parameter is sampled and is not 100% tested.

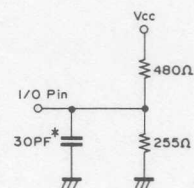
AC characteristics

•AC test conditions

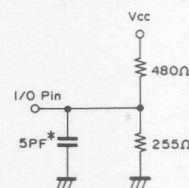
($V_{CC} = 5V \pm 10\%$, $T_a = 0$ to $+70^\circ C$)

Item	Condition
Input pulse high level	$V_{IH} = 3.0V$
Input pulse low level	$V_{IL} = 0V$
Input rise time	$t_r = 5ns$
Input fall time	$t_f = 5ns$
Input and output reference level	1.5V
Output load conditions	Fig. 1

Output Load (1)



Output Load (2)**



* including scope and jig

** for t_{LZ} , t_{HZ} , t_{OW} , t_{WHZ}

Fig. 1

● Read cycle

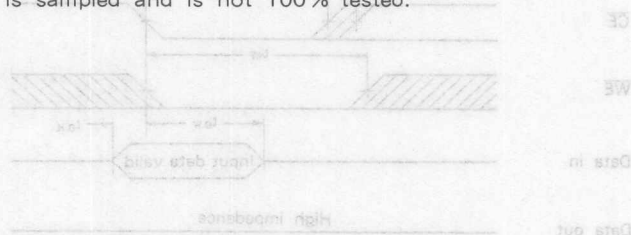
Item	Symbol	- 35		- 45		- 55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t _{RC}	35	—	45	—	55	—	ns
Address access time	t _{AA}	—	35	—	45	—	55	ns
Chip enable access time (CE)	t _{CO}	—	35	—	45	—	55	ns
Output hold from address change	t _{OH}	5	—	5	—	5	—	ns
Chip enable to output in low Z (CE)	t _{LZ} *	5	—	5	—	5	—	ns
Chip disable to output in high Z	t _{HZ} *	0	15	0	15	0	20	ns
Chip enable to power up time	t _{PU}	0	—	0	—	0	—	ns
Chip disable to power down time	t _{PD}	—	30	—	30	—	30	ns

*Note) Transition is measured $\pm 200\text{mV}$ from steady voltage with specified loading in Fig. 1.
This parameter is sampled and is not 100% tested.

● Write cycle

Item	Symbol	- 35		- 45		- 55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t _{WC}	35	—	45	—	55	—	ns
Address valid to end of write	t _{AW}	30	—	35	—	45	—	ns
Chip enable to end of write	t _{CW}	30	—	35	—	45	—	ns
Data to write time overlap	t _{DW}	15	—	20	—	25	—	ns
Data hold from write time	t _{DH}	0	—	0	—	0	—	ns
Write pulse width	t _{WP}	30	—	35	—	45	—	ns
Address set up time	t _{AS}	0	—	0	—	0	—	ns
Write recovery time	t _{WR}	0	—	0	—	0	—	ns
Output active from end of write	t _{OW} *	5	—	5	—	5	—	ns
Write to output in high Z	t _{WHZ} *	0	15	0	15	0	20	ns

*Note) Transition is measured $\pm 200\text{mV}$ from steady voltage with specified loading in Fig. 1.
This parameter is sampled and is not 100% tested.



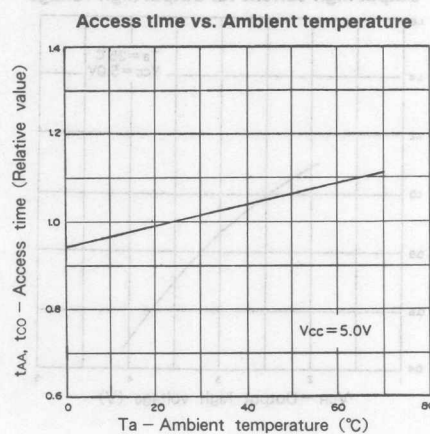
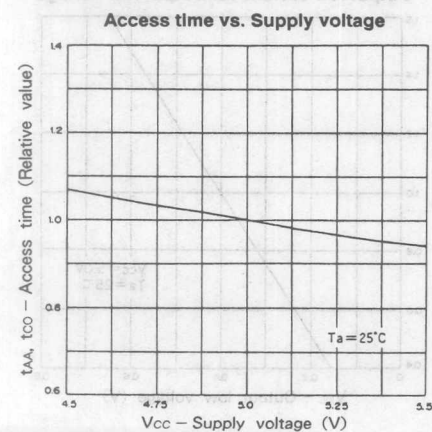
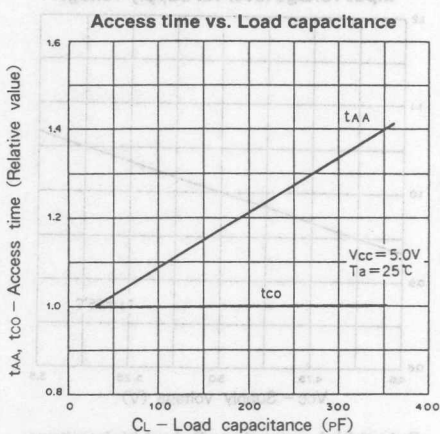
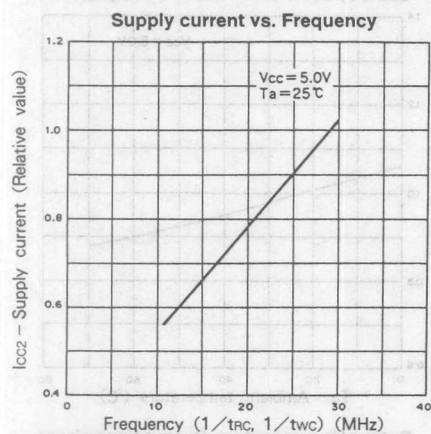
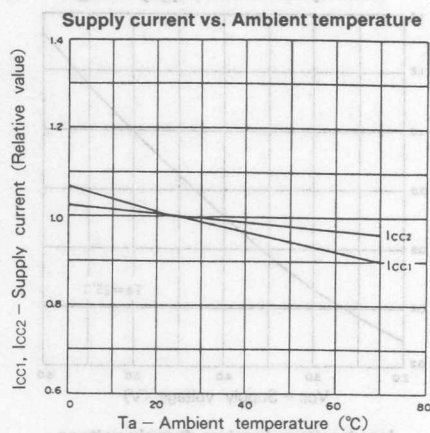
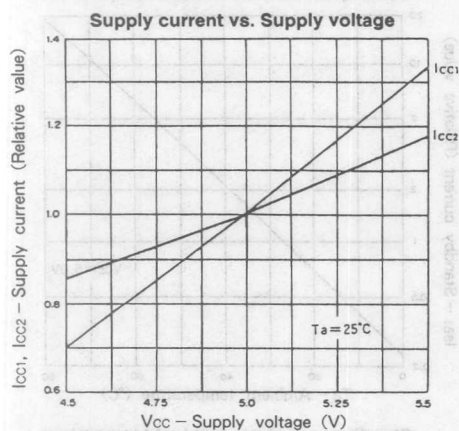
*Note)
1. A write occurs during the low overlap of CE and WE.
2. t_{WR} is measured from the earlier of CE or WE going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the output must not be applied.

-

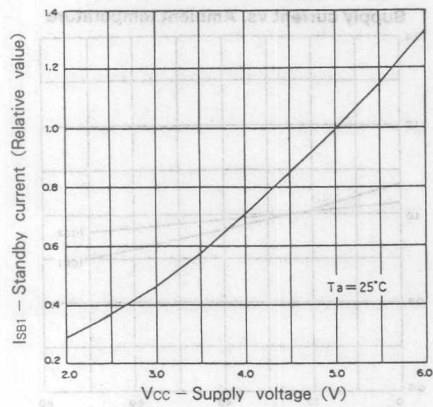
-
- Timing diagram for the 74VHC163 4-bit binary counter. The diagram shows the relationship between Address input, CE (Clock Enable), WE (Write Enable), Data in, and Data out. Key timing parameters are labeled: t_{WC} (Write Cycle time), t_{AS} (Address Setup time), $t_{CW} (*1)$ (Clock-to-Write time), $t_{WR} (*2)$ (Write-to-Rest time), t_{WP} (Write Pulse width), t_{DV} (Data Valid time), t_{DH} (Data Hold time), and t_{DI} (Data Invalid time). The Data in signal is shown as a pulse, and the Data out signal is shown as a high impedance state during the write cycle.

1. A write occurs during the low overlap of $\overline{CE}$ and $\overline{WE}$.
2. t_{WR} is measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the output must not be applied.

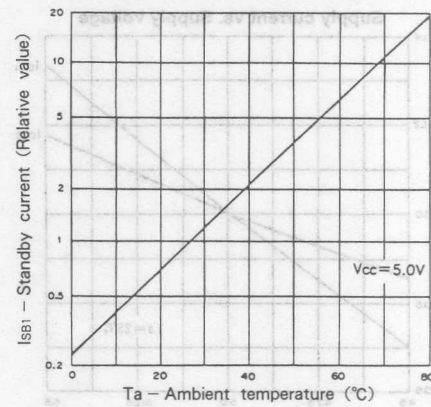
Example of Representative Characteristics



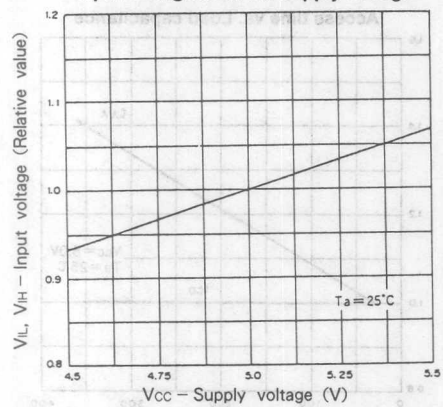
Standby current vs. Supply voltage



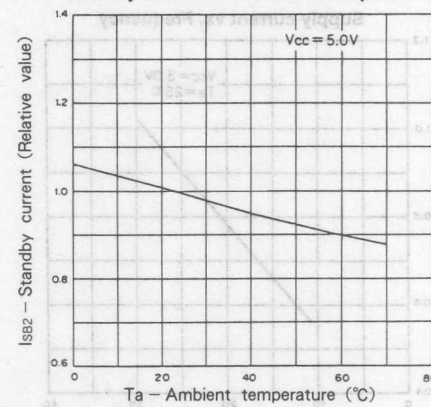
Standby current vs. Ambient temperature



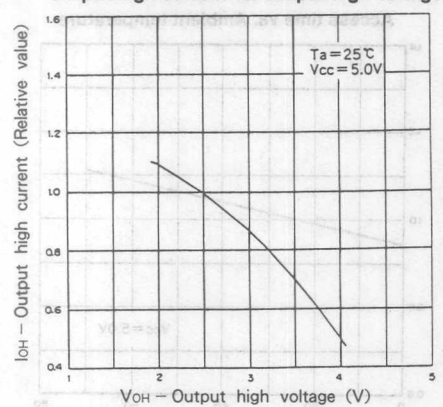
Input voltage level vs. Supply voltage



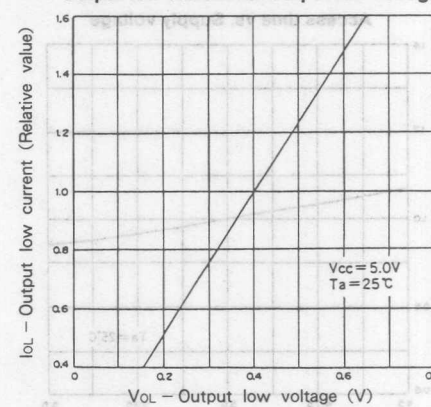
Standby current vs. Ambient temperature



Output high current vs. Output high voltage

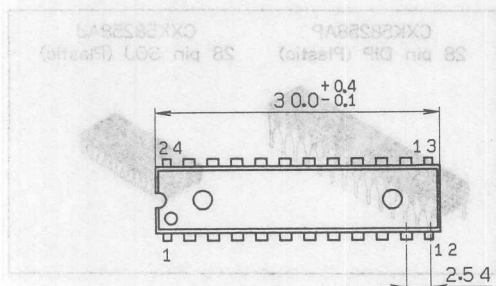
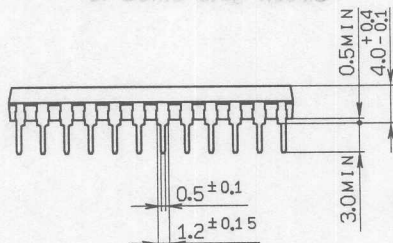


Output low current vs. Output low voltage



Package Outline Unit : mm

CXK54256P 24 pin DIP (Plastic) 300mil 1.5g

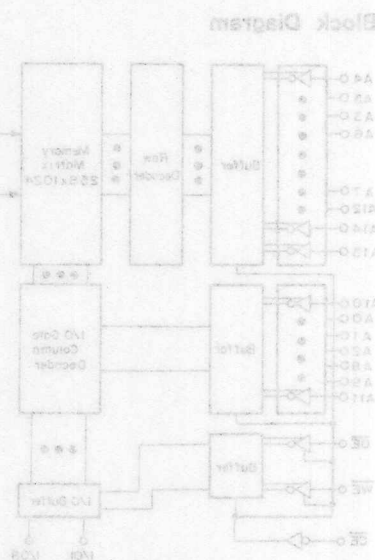
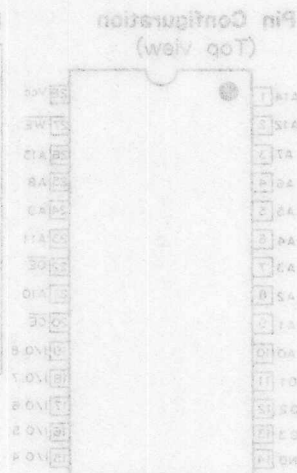
Function
32,768-word x 8-bit static RAMStructure
Silicon gate CMOS IC

Description
The CXK54256P is a high speed CMOS static RAM which consists of 32,768-word x 8-bit. It operates at 20/25ns access time from 5V single supply.

Features
• High speed, low power consumption
• Access time: Power consumption (max) (Typ. Case-Min)
CXK54256P/A1-15 18ns 800mW
CXK54256P/A1-20 20ns 450mW
CXK54256P/A1-25 25ns 375mW

• Single +5V power supply:
-15 5V ± 5%
-20/25 5V ± 10%
• Fully static memory: No clock or timing stops required.
• Equal access and cycle time.
• Directly TTL compatible all inputs and outputs.
• Common data 08
• three state output
• Available in 28 pin 300mil DIP, 300mil SOJ package.

Symbol	Description
A0 to A14	Address input
I/O 0 to I/O 7	Data input/output
CE	Chip enable input
WE	Write enable input
OE	Output enable input
VCC	+5V power supply
GND	Ground



SONY
CXK58258AP/AJ -15/20/25

32,768-word × 8-bit High Speed CMOS Static RAM

Description

The CXK58258AP/AJ is a high speed CMOS static RAM which consists of 32,768-word × 8-bit. It operates at 15/20/25ns access time from 5V single power supply.

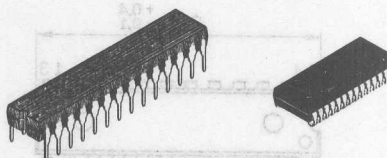
Features

- High speed, low power consumption :

	Access time (Max.)	Power consumption (Typ., Cycle = Min.)
CXK58258AP/AJ-15	15ns	500mW
CXK58258AP/AJ-20	20ns	425mW
CXK58258AP/AJ-25	25ns	375mW

- Single + 5V power supply :
 - 15 5V ± 5%
 - 20/25 5V ± 10%
- Fully static memory...No clock or timing strobe required.
- Equal access and cycle time.
- Directly TTL compatible all inputs and outputs.
- Common data input and output :
 - three state output
- Available in 28 pin 300mil DIP, 300mil SOJ package.

CXK58258AP 28 pin DIP (Plastic) CXK58258AJ 28 pin SOJ (Plastic)



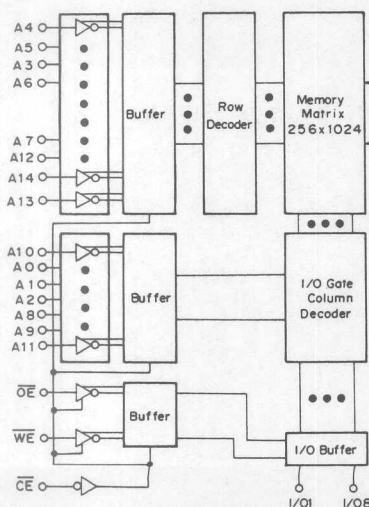
Function

32,768-word × 8-bit static RAM

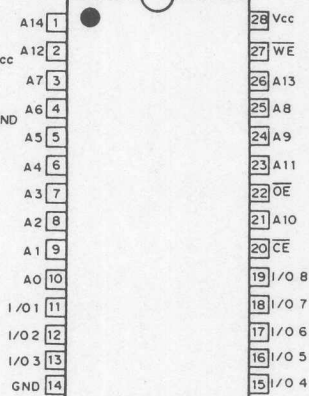
Structure

Silicon gate CMOS IC

Block Diagram



Pin Configuration (Top view)



Pin Description

Symbol	Description
A0 to A14	Address input
I/O1 to I/O8	Data input/output
$\overline{CE}$	Chip enable input
$\overline{WE}$	Write enable input
$\overline{OE}$	Output enable input
Vcc	+ 5V power supply
GND	Ground

Absolute Maximum Ratings

(Ta = 25°C, GND = 0V)

Item	Symbol	Rating	Unit
Supply voltage	V _{CC}	-0.5* to +7.0	V
Input voltage	V _{IN}	-0.5* to V _{CC} + 0.5	V
Input and output voltage	V _{I/O}	-0.5* to V _{CC} + 0.5	V
Allowable power dissipation	P _D	1.0	W
Operating temperature	T _{opr}	0 to +70	°C
Storage temperature	T _{stg}	-55 to +150	°C
Soldering temperature • time	T _{solder}	260 • 10	°C • sec

* V_{CC}, V_{IN}, V_{I/O} = -3.5V Min. for pulse width less than 20ns.

Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O1 to I/O8	V _{CC} Current
H	X	X	Not selected	High Z	I _{SB1} , I _{SB2}
L	H	H	Output disable	High Z	I _{CC1} , I _{CC2}
L	L	H	Read	Data out	I _{CC1} , I _{CC2}
L	X	L	Write	Data in	I _{CC1} , I _{CC2}

X: "H" or "L"

DC Recommended Operating Conditions

(Ta = 0 to +70°C, GND = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V _{CC}	-15	4.75	5.25	V
		-20/25	4.5	5.0	
Input high voltage	V _{IH}	2.2	—	V _{CC} + 0.3	V
Input low voltage	V _{IL}	-0.3*	—	0.8	V

* V_{IL} = -3.0V Min. for pulse width less than 20ns.

Electrical Characteristics

• DC and operating characteristics (Vcc = 5V ± 10%*, GND = 0V, Ta = 0 to +70°C)

Item	Symbol	Test conditions	Min.	Typ.**	Max.	Unit
Input leakage current	ILI	VIN = GND to Vcc	-1	—	1	μA
Output leakage current	ILO	V _{I/O} = GND to Vcc, CE = VIH or OE = VIH or WE = VIL	-1	—	1	μA
Operating power supply current	Icc1	CE = VIL, VIN = VIH or VIL, IOUT = 0mA	—	—	—	mA
Average operating current	Icc2	Cycle = Min, Duty = 100%, IOUT = 0mA, CE = VIL, VIN = VIH or VIL	-15	100	130	mA
			-20	85	120	
			-25	75	120	
Standby current	ISB1	CE ≥ Vcc - 0.2V VIN ≥ Vcc - 0.2V or VIN ≤ 0.2V	—	—	1	mA
	ISB2	Cycle = Min, Duty = 100%, CE = VIH, VIN = VIL or VIH	—	15	25	mA
Output high voltage	VOH	I _{OH} = -4.0mA	2.4	—	—	V
Output low voltage	VOL	I _{OL} = 8.0mA	—	—	0.4	V

* Vcc = 5V ± 5% for CXK58258AP/AJ-15

** Vcc = 5V, Ta = 25°C

I/O capacitance

(Ta = 25°C, f = 1MHz)

Item	Symbol	Test conditions	Min.	Max.	Unit
Input capacitance	CIN	VIN = 0V	—	6	pF
I/O capacitance	C _{I/O}	V _{I/O} = 0V	—	7	pF

(Note) This parameter is sampled and is not 100% tested.

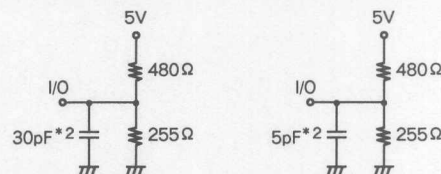
AC characteristics

• AC test conditions

(Vcc = 5V ± 10%*1, Ta = 0 to +70°C)

Item	Conditions
Input pulse high level	VIH = 3.0V
Input pulse low level	VIL = 0V
Input rise time	tr = 3ns
Input fall time	tf = 3ns
Input and output reference level	1.5V
Output load conditions	Fig. 1

Output Load (1) Output Load (2)*3



*1 Vcc = 5V ± 5% for CXK58258AP/AJ-15

*2 including scope and jig capacitance

*3 for tLZ, tHZ, tOHZ, tOLZ, tOW, tWHZ

Fig. 1

• Read cycle

Item	Symbol	- 15		- 20		- 25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t _{RC}	15	—	20	—	25	—	ns
Address access time	t _{AA}	—	15	—	20	—	25	ns
Chip enable access time	t _{CO}	—	15	—	20	—	25	ns
Output enable to output valid	t _{OE}	—	8	—	10	—	12	ns
Output hold from address change	t _{OH}	5	—	5	—	5	—	ns
Chip enable to output in low Z ($\overline{\text{CE}}$)	t _{LZ} *	3	—	3	—	3	—	ns
Output enable to output in low Z ($\overline{\text{OE}}$)	t _{OLZ} *	2	—	2	—	2	—	ns
Chip disable to output in high Z ($\overline{\text{CE}}$)	t _{HZ} *	—	8	—	9	—	10	ns
Chip disable to output in high Z ($\overline{\text{OE}}$)	t _{OHZ} *	—	7	—	8	—	9	ns
Chip enable to power up time	t _{PU}	0	—	0	—	0	—	ns
Chip disable to power down time	t _{PD}	—	15	—	20	—	25	ns

* Transition is measured $\pm 200\text{mV}$ from steady voltage with specified loading in Fig. 1-(2).
This parameter is sampled and is not 100% tested.

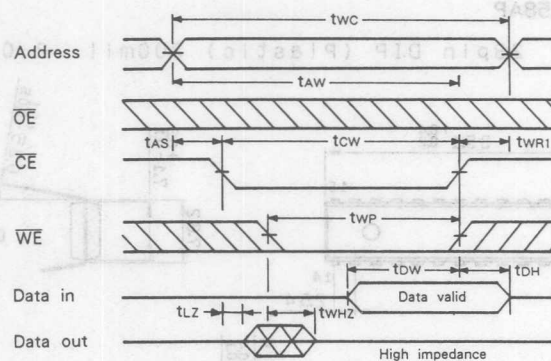
• Write cycle

Item	Symbol	- 15		- 20		- 25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t _{WC}	15	—	20	—	25	—	ns
Address valid to end of write	t _{AW}	10	—	13	—	15	—	ns
Chip enable to end of write	t _{CW}	11	—	14	—	16	—	ns
Data to write time overlap	t _{DW}	8	—	10	—	12	—	ns
Data hold from write time	t _{DH}	0	—	0	—	0	—	ns
Write pulse width	t _{WP}	10	—	13	—	15	—	ns
Address setup time	t _{AS}	0	—	0	—	0	—	ns
Write recovery time ($\overline{\text{WE}}$)	t _{WR}	0	—	0	—	0	—	ns
Write recovery time ($\overline{\text{CE}}$)	t _{WR1}	0	—	0	—	0	—	ns
Output active from end of write	t _{OW} *	3	—	3	—	3	—	ns
Write to output in high Z	t _{WHZ} *	—	8	—	9	—	10	ns

* Transition is measured $\pm 200\text{mV}$ from steady voltage with specified loading in Fig. 1-(2).
This parameter is sampled and is not 100% tested.



• Write cycle (2) : $\overline{CE}$ control



Note)

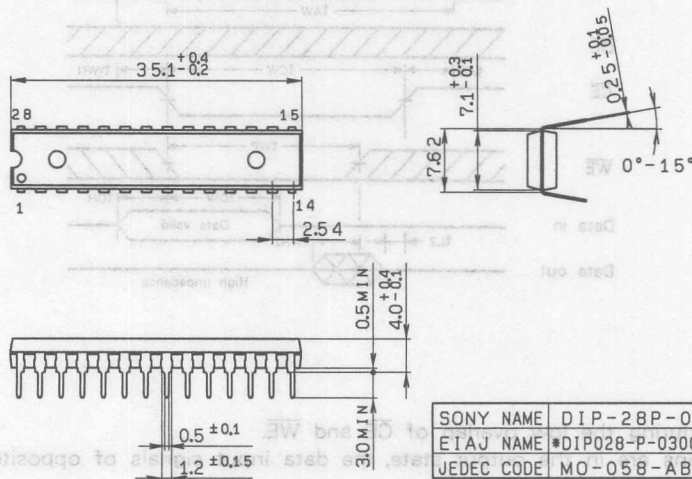
1. Write occurs during the low overlap of $\overline{CE}$ and $\overline{WE}$.
2. During I/O pins are in the output state, the data input signals of opposite phase to the output must not be applied.

Package Outline Unit : mm

White cycle (S) : CE control *

CXK58258AP

28pin DIP (Plastic) 300mil±2.0g

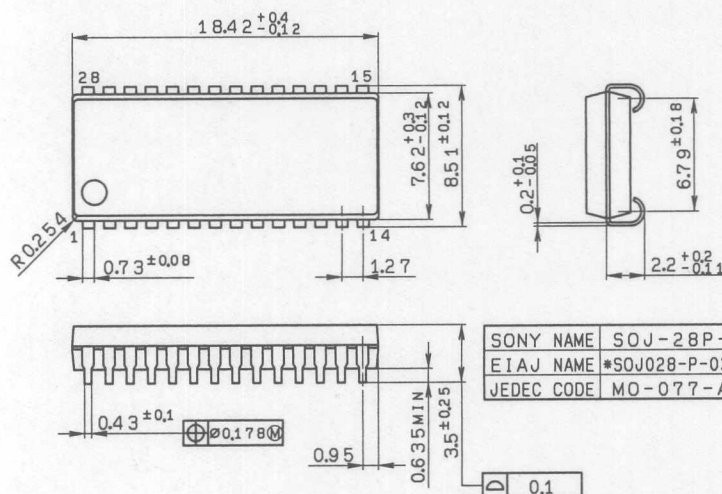


SONY NAME	DIP-28P-06
EIAJ NAME	*DIP028-P-0300-A
JEDEC CODE	MO-058-AB *

* (Similar)

CXK58258AJ

28pin SOJ (Plastic) 300mil 0.8g



SONY NAME	SOJ-28P-01
EIAJ NAME	*SOJ028-P-0300-A
JEDEC CODE	MO-077-AB

SONY CXK58258BP/BJ/BM -20L/25L/35L -20LL/25LL/35LL

32,768-word × 8-bit High Speed CMOS Static RAM

Description

The CXK58258BP/BJ is a high speed CMOS static RAM which consists of 32,768-word × 8-bit. It operates at 20/25/35ns access time from 5V single power supply.

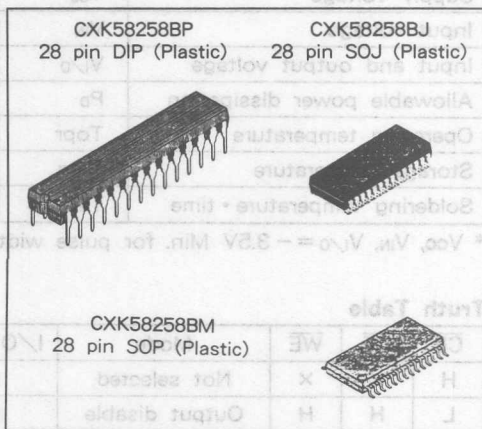
This device is suitable for use in high speed and low power applications in which battery back up for nonvolatility is required.

Features

- Fast access time (Access time)
CXK58258BP/BJ-20L, 20LL 20ns (Max.)
CXK58258BP/BJ-25L, 25LL 25ns (Max.)
CXK58258BP/BJ-35L, 35LL 35ns (Max.)
- Low power operation

	Standby (Max.)	Operation (Typ., Min. Cycle)
CXK58258BP/BJ-20LL	5 μ W	425mW
CXK58258BP/BJ-25LL	5 μ W	375mW
CXK58258BP/BJ-35LL	5 μ W	325mW
CXK58258BP/BJ-20L	10 μ W	425mW
CXK58258BP/BJ-25L	10 μ W	375mW
CXK58258BP/BJ-35L	10 μ W	325mW

- Single +5V power supply : 5V $\pm$ 10 %
- Fully static memory...No clock or timing strobe required.
- Equal access and cycle time.
- Directly TTL compatible all inputs and outputs.
- Common data input and output : three state output
- Available in 28 pin 300mil DIP, 300mil SOJ package.



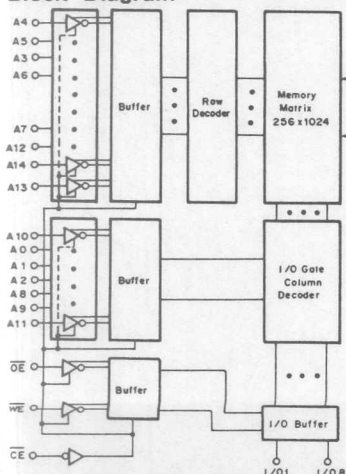
Function

32,768-word × 8-bit static RAM

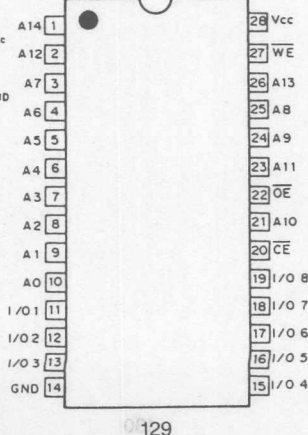
Structure

Silicon gate CMOS IC

Block Diagram



Pin Configuration (Top view)



Pin Description

Symbol	Description
A0 to A14	Address input
I/O1 to I/O8	Data input/output
CE	Chip enable input
WE	Write enable input
OE	Output enable input
Vcc	+5V power supply
GND	Ground

SONY reserves the right to change products and specifications without notice.
This information does not convey any license under patent rights of SONY corporation or others.

PE90268 - ST

Absolute Maximum Ratings (Ta = 25°C, GND = 0V)

Item	Symbol	Rating	Unit
Supply voltage	Vcc	- 0.5* to + 7.0	V
Input voltage	V _{IN}	- 0.5* to Vcc + 0.5	V
Input and output voltage	V _{I/O}	- 0.5* to Vcc + 0.5	V
Allowable power dissipation	Pd	1.0	W
Operating temperature	Topr	0 to + 70	°C
Storage temperature	Tstg	- 55 to + 150	°C
Soldering temperature • time	Tsolder	260 • 10	°C • sec

* Vcc, V_{IN}, V_{I/O} = - 3.5V Min. for pulse width less than 20ns.

Truth Table

CE	OE	WE	Mode	I/O1 to I/O8	Vcc Current
H	X	X	Not selected	High Z	I _{sB1} , I _{sB2}
L	H	H	Output disable	High Z	I _{cc1} , I _{cc2}
L	L	H	Read	Data out	I _{cc1} , I _{cc2}
L	X	L	Write	Data in	I _{cc1} , I _{cc2}

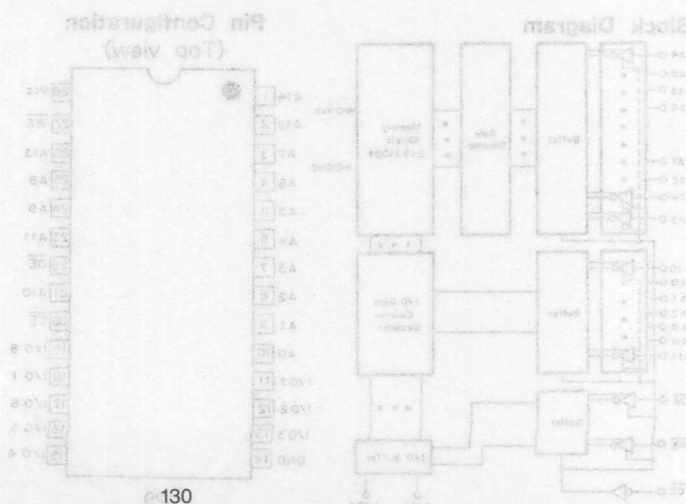
X : "H" or "L"

DC Recommended Operating Conditions (Ta = 0 to + 70°C, GND = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Vcc	4.5	5.0	5.5	V
Input high voltage	V _{IH}	2.2	—	Vcc + 0.3	V
Input low voltage	V _{IL}	- 0.3*	—	0.8	V

* V_{IL} = - 3.0V Min. for pulse width less than 20ns.

Symbol	Description
A0 to A14	Address input
I/O1 to I/O8	Data input/output
OE	Chip enable input
WE	Write enable input
OE	Output enable input
Vcc	+ 5V power supply
GND	Ground



Electrical Characteristics

• DC and operating characteristics

(V_{CC} = 5V ± 10 %, GND = 0V, T_a = 0 to +70 °C)

Item	Symbol	Test conditions	-20L/25L/35L			-20LL/25LL/35LL			Unit	
			Min.	Typ.*	Max.	Min.	Typ.*	Max.		
Input leakage current	I _{LI}	V _{IN} = GND to V _{CC}	- 1	—	1	- 1	—	1	μA	
Output leakage current	I _{LO}	V _{I/O} = GND to V _{CC} , CE = V _{IH} or OE = V _{IH}	- 1	—	1	- 1	—	1	μA	
Operating power supply current	I _{CC1}	CE = V _{IL} , V _{IN} = V _{IH} or V _{IL} , I _{OUT} = 0mA	—	—	—	—	—	—	mA	
Average operating current	I _{CC2}	Cycle = Min, Duty = 100 %, I _{OUT} = 0mA, CE = V _{IL} , V _{IN} = V _{IH} or V _{IL}	-20L/20LL	—	85	120	—	85	120	mA
		-25L/25LL	—	75	120	—	75	120		
		-35L/35LL	—	65	100	—	65	100		
Standby current	I _{SB1}	CE ≥ V _{CC} - 0.2V	—	0.002	0.1	—	0.001	0.05	mA	
	I _{SB2}	Cycle = Min, Duty = 100 %, CE = V _{IH}	—	1.5	5	—	1.5	5	mA	
Output high voltage	V _{OH}	I _{OH} = - 4.0mA	2.4	—	—	2.4	—	—	V	
Output low voltage	V _{OL}	I _{OL} = 8.0mA	—	—	0.4	—	—	0.4	V	

* V_{CC} = 5V, T_a = 25 °C

I/O capacitance

(T_a = 25 °C, f = 1MHz)

Item	Symbol	Test conditions	Min.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} = 0V	—	6	pF
I/O capacitance	C _{I/O}	V _{I/O} = 0V	—	7	pF

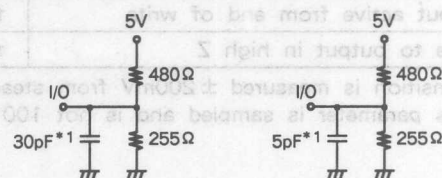
Note) This parameter is sampled and is not 100 % tested.

AC characteristics

• AC test conditions

(V_{CC} = 5V ± 10 %, T_a = 0 to +70 °C)

Item	Conditions
Input pulse high level	V _{IH} = 3.0V
Input pulse low level	V _{IL} = 0V
Input rise time	t _r = 3ns
Input fall time	t _f = 3ns
Input and output reference level	1.5V
Output load conditions	Fig. 1

Output Load (1) Output Load (2)*²

*1 including scope and jig capacitance

*2 for t_{LZ}, t_{HZ}, t_{OHZ}, t_{OLZ}, t_{OW}, t_{WHZ}

Fig. 1

• Read cycle

Item	Symbol	-20L/20LL		-25L/25LL		-35L/35LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t _{RC}	20	—	25	—	35	—	ns
Address access time	t _{AA}	—	20	—	25	—	35	ns
Chip enable access time	t _{CO}	—	20	—	25	—	35	ns
Output enable to output valid	t _{OE}	—	10	—	12	—	15	ns
Output hold from address change	t _{OH}	5	—	5	—	5	—	ns
Chip enable to output in low Z ($\overline{CE}$)	t _{LZ} *	3	—	3	—	3	—	ns
Output enable to output in low Z ($\overline{OE}$)	t _{OLZ} *	2	—	2	—	2	—	ns
Chip disable to output in high Z ($\overline{CE}$)	t _{HZ} *	—	9	—	10	—	15	ns
Chip disable to output in high Z ($\overline{OE}$)	t _{OHZ} *	—	8	—	9	—	12	ns
Chip enable to power up time	t _{PU}	0	—	0	—	0	—	ns
Chip disable to power down time	t _{PD}	—	20	—	25	—	35	ns

* Transition is measured $\pm 200\text{mV}$ from steady voltage with specified loading in Fig. 1-(2).
This parameter is sampled and is not 100% tested.

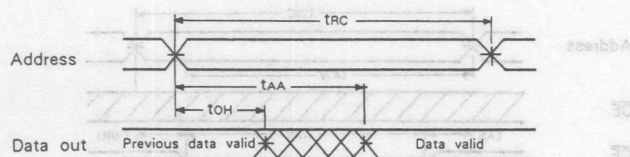
• Write cycle

Item	Symbol	-20L/20LL		-25L/25LL		-35L/35LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t _{WC}	20	—	25	—	35	—	ns
Address valid to end of write	t _{AW}	13	—	15	—	20	—	ns
Chip enable to end of write	t _{CW}	14	—	16	—	20	—	ns
Data to write time overlap	t _{DW}	10	—	12	—	15	—	ns
Data hold from write time	t _{DH}	0	—	0	—	0	—	ns
Write pulse width	t _{WP}	13	—	15	—	20	—	ns
Address setup time	t _{AS}	0	—	0	—	0	—	ns
Write recovery time ($\overline{WE}$)	t _{WR}	0	—	0	—	0	—	ns
Write recovery time ($\overline{CE}$)	t _{WR1}	0	—	0	—	0	—	ns
Output active from end of write	t _{OW} *	3	—	3	—	3	—	ns
Write to output in high Z	t _{WHZ} *	—	9	—	10	—	12	ns

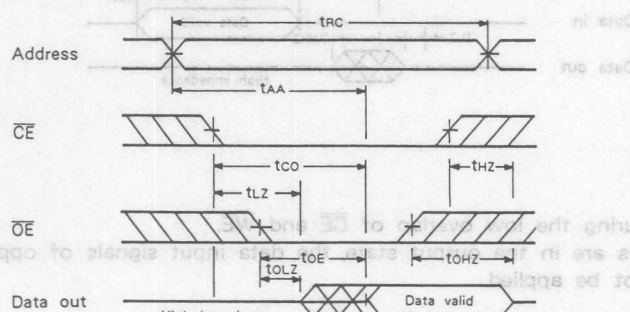
* Transition is measured $\pm 200\text{mV}$ from steady voltage with specified loading in Fig. 1-(2).
This parameter is sampled and is not 100% tested.

Timing Waveform

- Read cycle (1) : $\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$

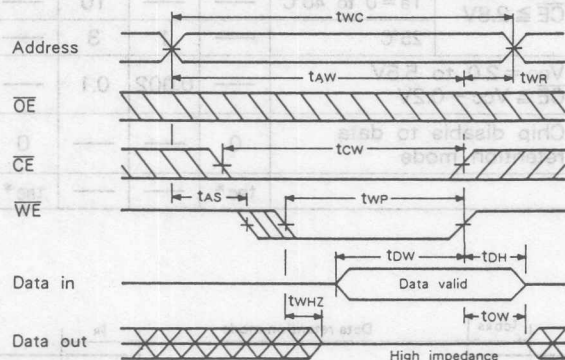


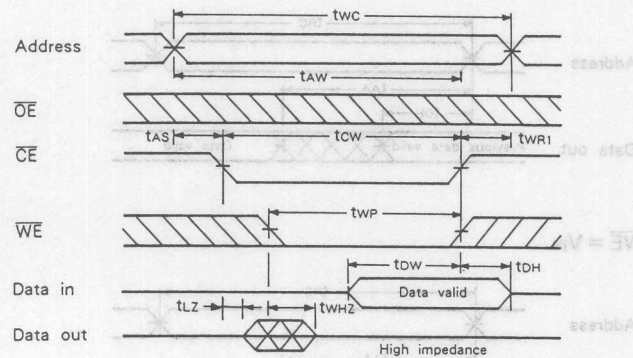
- Read cycle (2) : $\overline{WE} = V_{IH}$



Item	Symbol	Test conditions	Typ.	Max.	Unit
Data retention voltage	V_{DR}	$V_{CC} \leq V_{DR} \leq 0.2V$	2.0	2.5	V
Data retention current	I_{DR}	$V_{CC} = 3.0V$ $V_{DR} = 0.2V$	10	10	μA
Data retention setup time	t_{DS}	$V_{CC} = 3.0V$ $V_{DR} = 0.2V$	0.001	0.05	ms
Recovery time	t_{R}	$V_{CC} = 3.0V$ $V_{DR} = 0.2V$	0	0	ms

- Write cycle (1) : $\overline{WE}$ control





Note)

1. Write occurs during the low overlap of $\overline{CE}$ and $\overline{WE}$.
2. During I/O pins are in the output state, the data input signals of opposite phase to the output must not be applied.

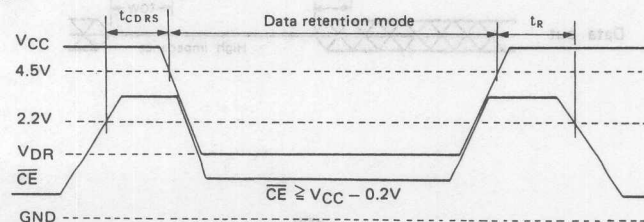
Data Retention Characteristics

($T_a = 0$ to $+70^\circ\text{C}$)

Item	Symbol	Test conditions		-20L/25L/35L			-20LL/25LL/35LL			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
Data retention voltage	V _{DR}	CE ≥ V _{CC} – 0.2V		2.0	—	5.5	2.0	—	5.5	V
Data retention current	I _{CCDR1}	V _{CC} = 3.0V CE ≥ 2.8V	T _a = 0 to 70 °C	—	—	50	—	—	10	μA
			T _a = 0 to 40 °C	—	—	10	—	—	4	
			25 °C	—	1	3	—	0.5	1	
	I _{CCDR2}	V _{CC} = 2.0 to 5.5V CE ≥ V _{CC} – 0.2V	—	0.002	0.1	—	0.001	0.05	mA	
Data retention setup time	t _{CDRS}	Chip disable to data retention mode		0	—	—	0	—	—	ns
Recovery time	t _R			t _{RC} *	—	—	t _{RC} *	—	—	ns

* t_{RC} : Read cycle time

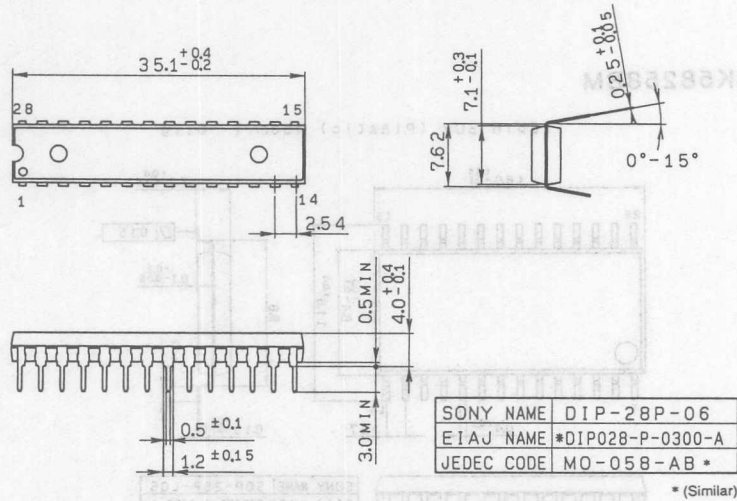
Data retention time



Package Outline Unit : mm

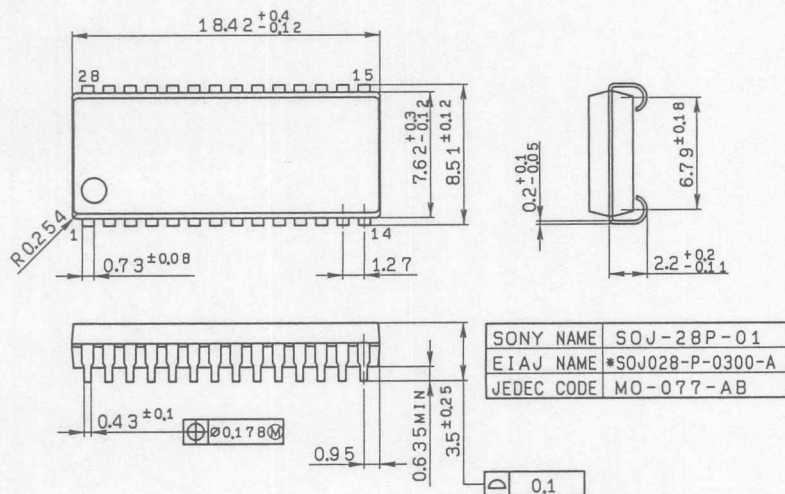
CXK58258BP

28pin DIP (Plastic) 300mil 2.0g



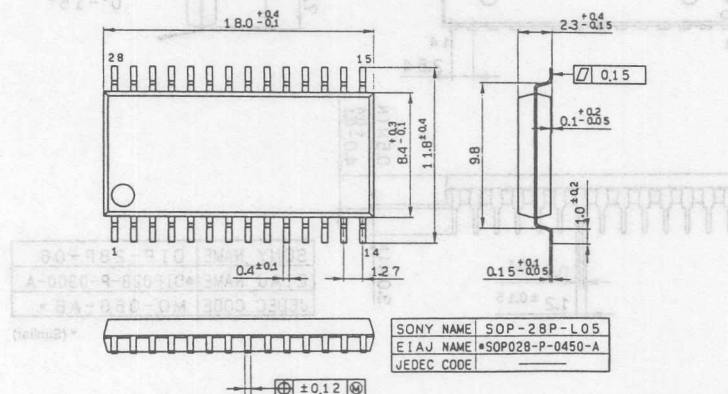
CXK58258BJ

28pin SOJ (Plastic) 300mil 0.8g



Unit : mm

28pin SOP (Plastic) 450mil 0.7g



SONY NAME	SOP-28P-L05
EIAJ NAME	*SOP028-P-0450-A
JDEC CODE	_____

Absolute Maximum Ratings

(Ta = 25°C, GND = 0V)

Item	Symbol	Rating	Unit
Supply voltage	V _{CC}	-0.5* to +7.0	V
Input voltage	V _{IN}	-0.5* to V _{CC} + 0.5	V
Input and output voltage	V _{I/O}	-0.5* to V _{CC} + 0.5	V
Allowable power dissipation	P _D	1.0	W
Operating temperature	T _{opr}	0 to +70	°C
Storage temperature	T _{stg}	-55 to +150	°C
Soldering temperature • time	T _{solder}	260 • 10	°C • sec

* V_{CC}, V_{IN}, V_{I/O} = -3.5V Min. for pulse width less than 20ns.

Truth Table

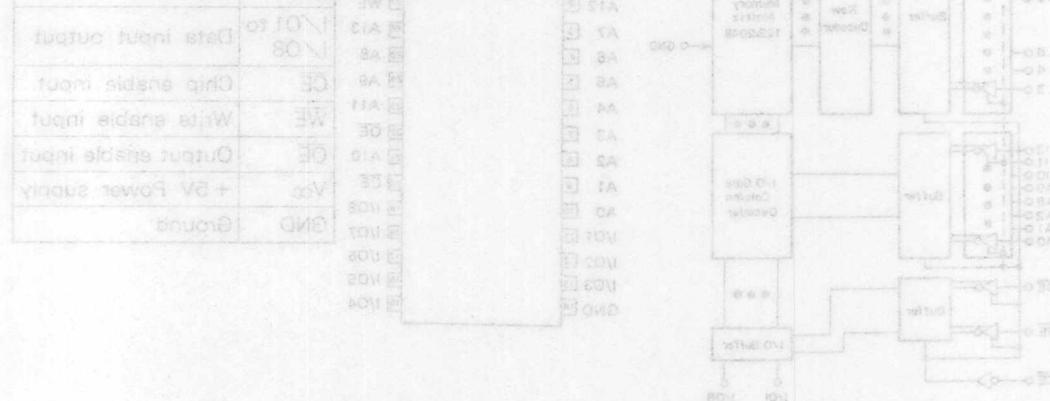
CE	OE	WE	Mode	I/O1 to I/O8	V _{CC} Current
H	X	X	Not selected	High Z	I _{SB1} , I _{SB2}
L	H	H	Output disable	High Z	I _{CC1} , I _{CC2}
L	L	H	Read	Data out	I _{CC1} , I _{CC2}
L	X	L	Write	Data in	I _{CC1} , I _{CC2}

X: "H" or "L"

DC Recommended Operating Conditions

(Ta = 0 to +70°C, GND = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Input high voltage	V _{IH}	2.2	—	V _{CC} + 0.3	V
Input low voltage	V _{IL}	-0.3*	—	0.8	V

* V_{IL} = -3.0V Min. for pulse width less than 20ns.

Electrical Characteristics

● DC and operating characteristics

(V_{CC} = 5V ± 10 %, GND = 0V, T_a = 0 to +70 °C)

Item	Symbol	Test condition	- 35/45/55			Unit
			Min.	Typ.*	Max.	
Input leak current	I _{LI}	V _{IN} = GND to V _{CC}	- 2	—	2	μA
Output leak current	I _{LO}	$\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$ V _{I/O} = GND to V _{CC}	- 2	—	2	μA
Operating supply current	I _{CC1}	$\overline{CE} = V_{IL}$, V _{IN} = V _{IH} or V _{IL} , I _{OUT} = 0mA	—	50	80	mA
Average operating current	I _{CC2}	Min. cycle Duty = 100 %, I _{OUT} = 0mA	—	90	140	mA
Standby current	I _{SB1}	$\overline{CE} \geq V_{CC} - 0.2V$	—	0.01	2	mA
	I _{SB2}	$\overline{CE} = V_{IH}$	—	—	10	
Output high voltage	V _{OH}	I _{OH} = - 4.0mA	2.4	—	—	V
Output low voltage	V _{OL}	I _{OL} = 8.0mA	—	—	0.4	V

* V_{CC} = 5V, T_a = 25 °C

I/O capacitance

(T_a = 25 °C, f = 1MHz)

Item	Symbol	Test condition	Min.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} = 0V	—	5	pF
Input/Output capacitance	C _{I/O}	V _{I/O} = 0V	—	7	pF

Note) This parameter is sampled and is not 100 % tested.

AC characteristics

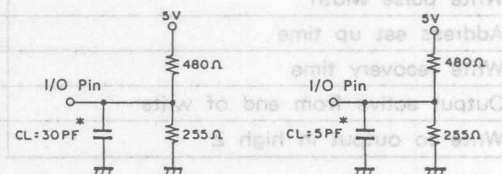
● AC test conditions

(V_{CC} = 5V ± 10 %, T_a = 0 to +70 °C)

Item	Condition
Input pulse high level	V _{IH} = 3.0V
Input pulse low level	V _{IL} = 0V
Input rise time	t _r = 5ns
Input fall time	t _f = 5ns
Input and output reference level	1.5V
Output load conditions	Fig. 1

Output Load (1)

Output Load (2)**



* including scope and jig capacitance

** for t_{LZ}, t_{HZ}, t_{OHZ}, t_{OLZ}, t_{OW}, t_{WHZ}

Fig. 1

• Read cycle

Item	Symbol	- 35		- 45		- 55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t _{RC}	35	—	45	—	55	—	ns
Address access time	t _{AA}	—	35	—	45	—	55	ns
Chip enable access time	t _{CO}	—	35	—	45	—	55	ns
Output enable to output valid	t _{OE}	—	20	—	25	—	30	ns
Output hold from address change	t _{OH}	5	—	5	—	5	—	ns
Chip enable to output in low Z ($\overline{CE}$)	t _{LZ} *	5	—	5	—	5	—	ns
Output enable to output in low Z ($\overline{OE}$)	t _{OLZ} *	0	—	0	—	0	—	ns
Chip disable to output in high Z ($\overline{CE}$)	t _{HZ} *	—	15	—	20	—	25	ns
Output disable to output in high Z ($\overline{OE}$)	t _{OHZ} *	—	15	—	20	—	25	ns
Power up time	t _{PU}	0	—	0	—	0	—	ns
Power down time	t _{PD}	—	35	—	45	—	55	ns

* Transition is measured $\pm 200\text{mV}$ from steady voltage with specified loading in Fig. 1-(2).

This parameter is sampled and is not 100% tested.

• Write cycle

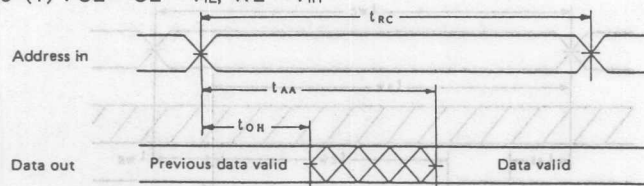
Item	Symbol	- 35		- 45		- 55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t _{WC}	35	—	45	—	55	—	ns
Address valid to end of write	t _{AW}	30	—	40	—	45	—	ns
Chip enable to end of write	t _{CW}	35	—	40	—	45	—	ns
Data to write time overlap	t _{DW}	18	—	20	—	20	—	ns
Data hold from write time	t _{DH}	0	—	0	—	0	—	ns
Write pulse width	t _{WP}	30	—	35	—	35	—	ns
Address set up time	t _{AS}	0	—	0	—	0	—	ns
Write recovery time	t _{WR}	0	—	0	—	0	—	ns
Output active from end of write	t _{OW} *	5	—	5	—	5	—	ns
Write to output in high Z	t _{WHZ} *	—	12	—	15	—	15	ns

* Transition is measured $\pm 200\text{mV}$ from steady voltage with specified loading in Fig. 1-(2).

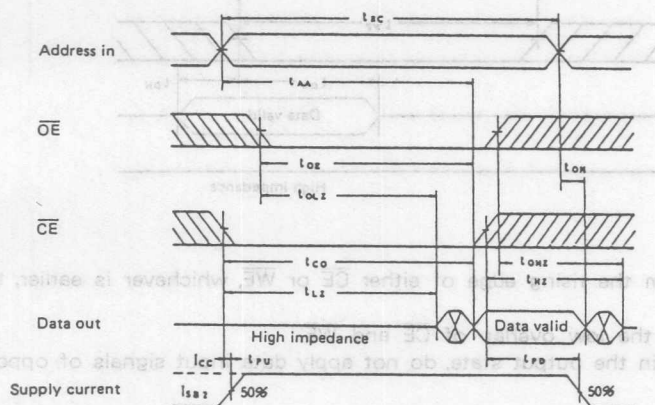
This parameter is sampled and is not 100% tested.

Timing Waveform

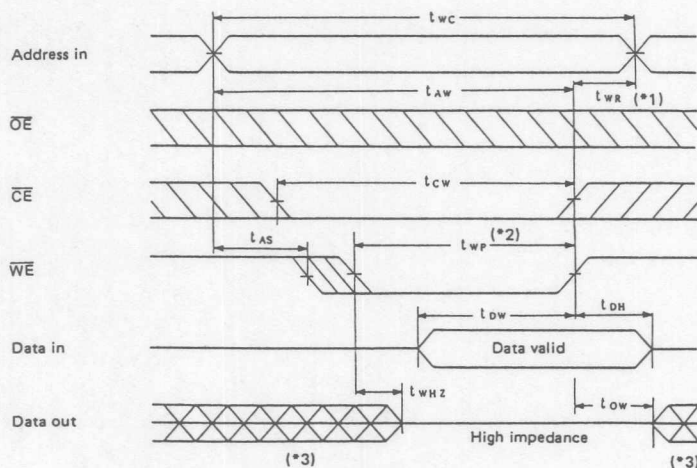
- Read cycle (1) : $\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$

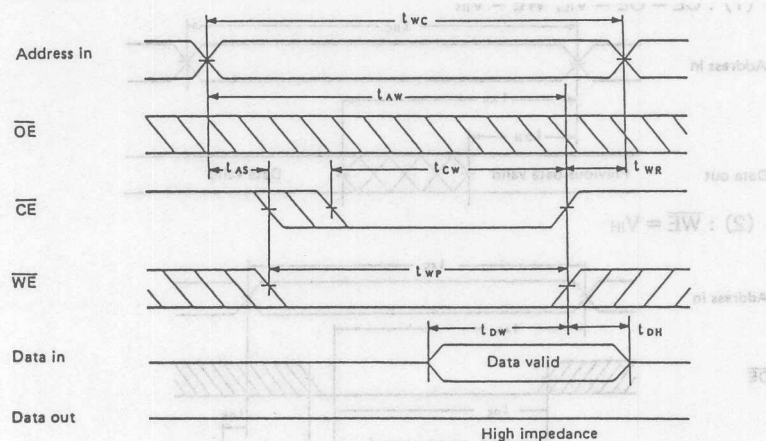


- Read cycle (2) : $\overline{WE} = V_{IH}$

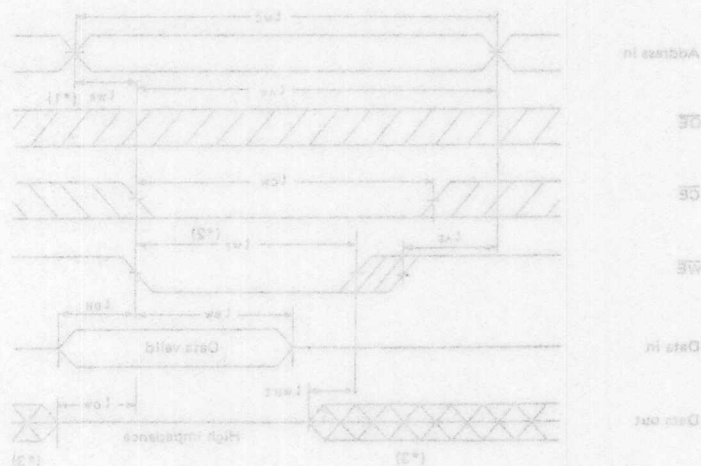


- Write cycle (1) : $\overline{WE}$ control

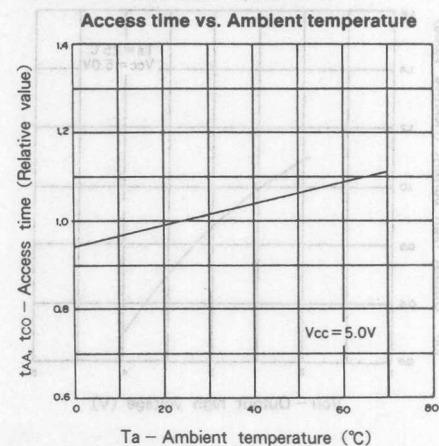
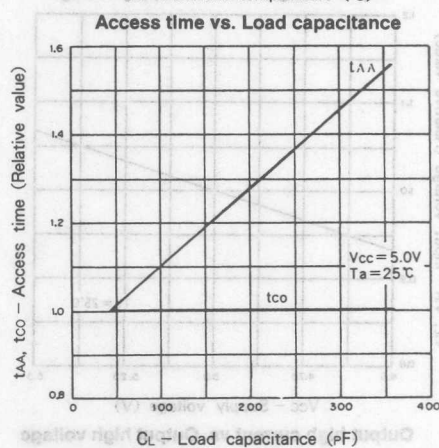
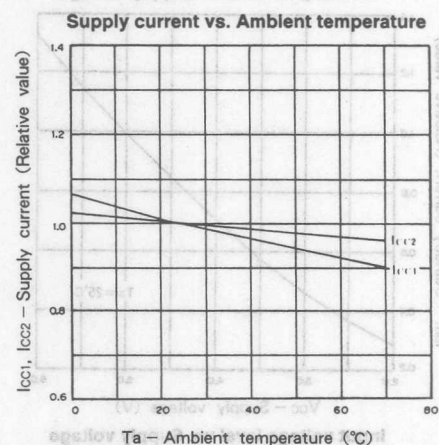
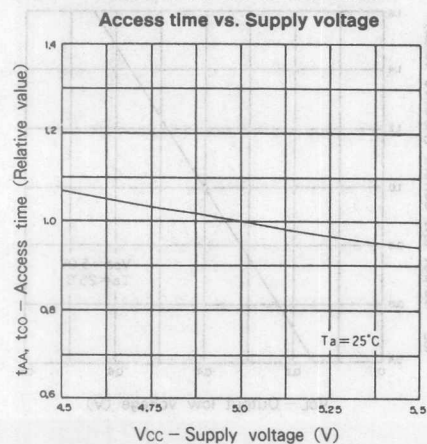
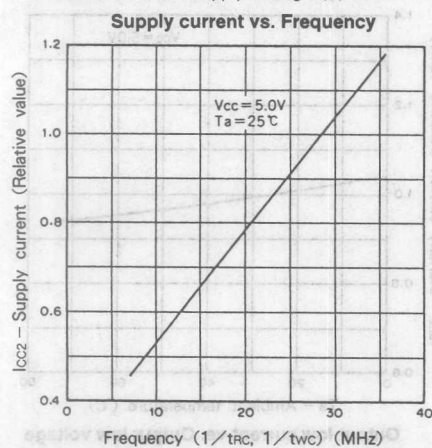
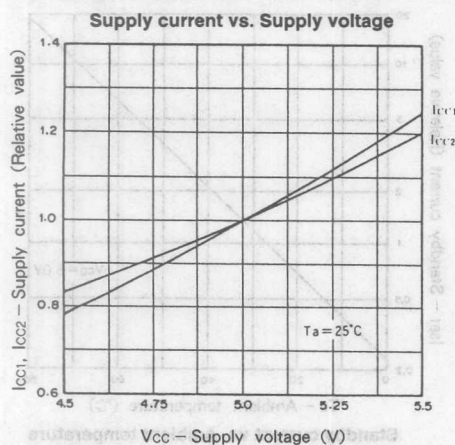




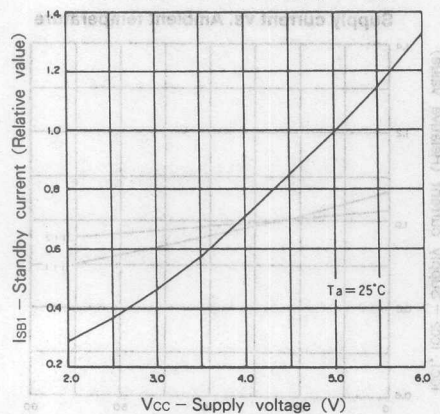
- * 1. t_{WR} is measured from the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever is earlier, to the end of write cycle.
- * 2. Write occurs during the low overlap of $\overline{CE}$ and $\overline{WE}$.
- * 3. While I/O pins are in the output state, do not apply data input signals of opposite phase to the output.



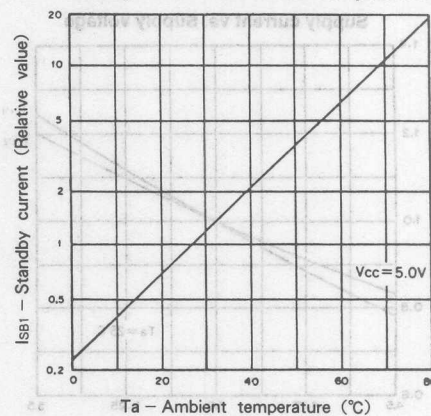
Example of Representative Characteristics



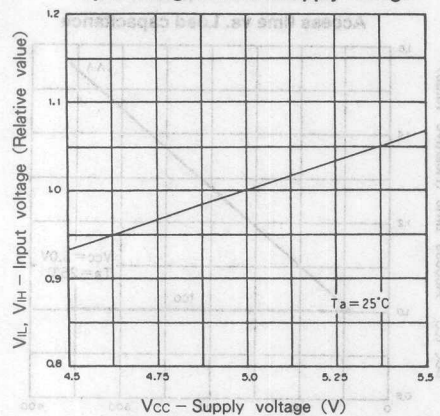
Standby current vs. Supply voltage



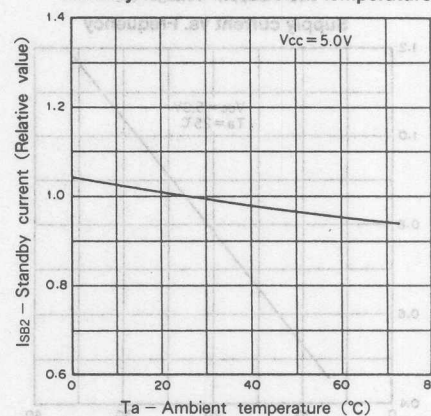
Standby current vs. Ambient temperature



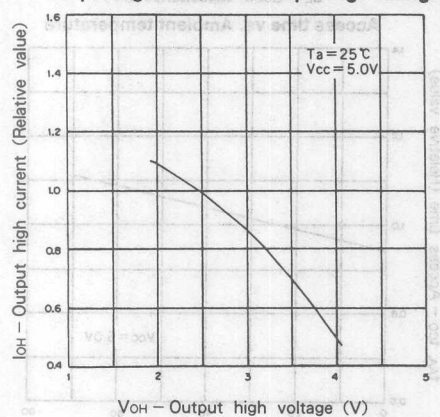
Input voltage level vs. Supply voltage



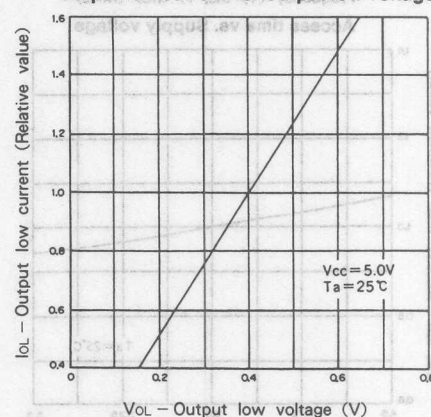
Standby current vs. Ambient temperature



Output high current vs. Output high voltage



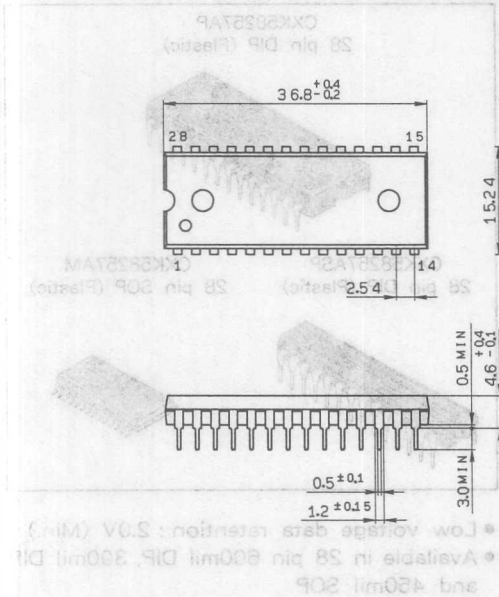
Output low current vs. Output low voltage



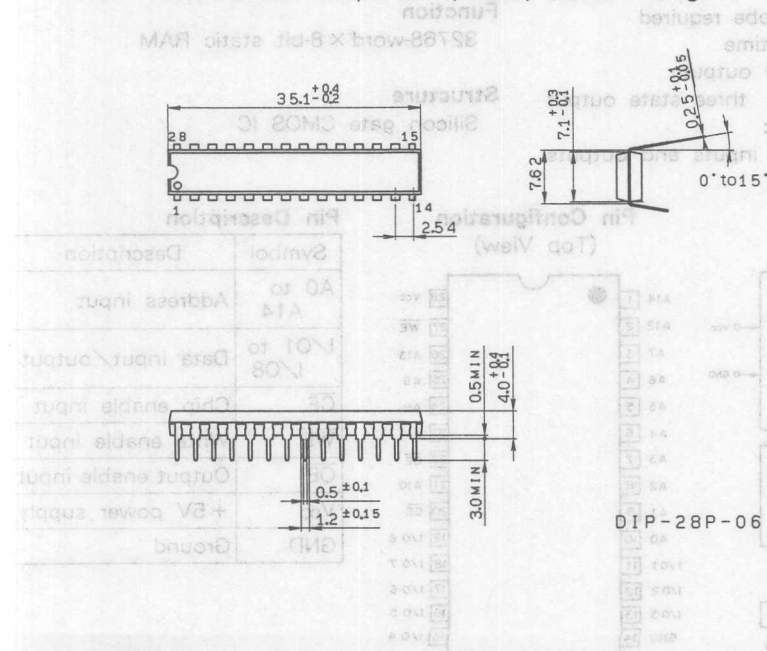
Package Outline

Unit : mm

CXK58258P 28 pin DIP (Plastic) 600mil 4.2g



CXK58258SP 28 pin DIP (Plastic) 300mil 2.0g



Block Diagram

DIP-28P-06



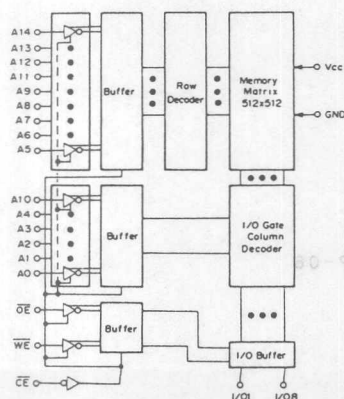
Description

CXK58257AP/ASP/AM is 262,144 bits high speed CMOS static RAM organized as 32,768 words by 8 bits and operates from a single 5V supply. This device is suitable for use in high speed and low power applications in which battery back up for nonvolatility is required.

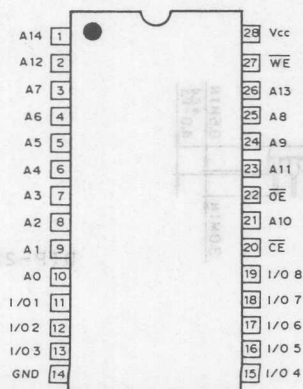
Features

- Fast access time : (Access time)
CXK58257AP/ASP/AM-70L, 70LL 70ns(Max.)
CXK58257AP/ASP/AM-85L, 85LL 85ns(Max.)
CXK58257AP/ASP/AM-10L, 10LL 100ns(Max.)
CXK58257AP/ASP/AM-12L, 12LL 120ns(Max.)
- Low power operation :
CXK58257AP/ASP/AM-70LL, 85LL, 10LL, 12LL ;
Standby : 1 μ W (Typ.)
Operation : 15mW (Typ.)
CXK58257AP/ASP/AM-70L, 85L, 10L, 12L ;
Standby : 2.5 μ W (Typ.)
Operation : 15mW (Typ.)
- Single +5V supply : +5V $\pm$ 10 %
- Fully static memory...No clock or timing strobe required
- Equal access and cycle time
- Common data input and output :
three state output
- Directly TTL compatible :
All inputs and outputs

Block Diagram

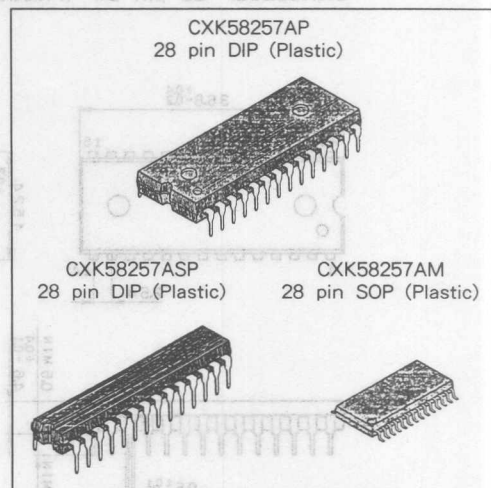


Pin Configuration (Top View)



Pin Description

Symbol	Description
A0 to A14	Address input
I/O1 to I/O8	Data input/output
CE	Chip enable input
WE	Write enable input
OE	Output enable input
Vcc	+5V power supply
GND	Ground



- Low voltage data retention : 2.0V (Min.)
- Available in 28 pin 600mil DIP, 300mil DIP and 450mil SOP

Function

32768-word $\times$ 8-bit static RAM

Structure

Silicon gate CMOS IC

Absolute Maximum Ratings

(Ta = 25°C, GND = 0V)

Item	Symbol	Rating	Unit
Supply voltage	V _{CC}	- 0.5 to + 7.0	V
Input voltage	V _{IN}	- 0.5* to V _{CC} + 0.5	V
Input and output voltage	V _{I/O}	- 0.5* to V _{CC} + 0.5	V
Allowable power dissipation	P _D	CXK58257AP/ASP	1.0
		CXK58257AM	0.7
			W
Operating temperature	T _{opr}	0 to + 70	°C
Storage temperature	T _{stg}	- 55 to + 150	°C
Soldering temperature	T _{solder}	260 ± 10	°C • sec

* V_{IN}, V_{I/O} = - 3.0V Min. for pulse width less than 50ns.

Truth Table

CE	OE	WE	Mode	I/O1 to I/O8	V _{CC} Current
H	X	X	Not selected	High Z	I _{SB1} , I _{SB2}
L	H	H	Not selected	High Z	I _{CC1} , I _{CC2}
L	L	H	Read	Data out	I _{CC1} , I _{CC2}
L	X	L	Write	Data in	I _{CC1} , I _{CC2}

X : "H" or "L"

DC Recommended Operating Conditions (Ta = 0 to + 70°C, GND = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Input high voltage	V _{IH}	2.2	—	V _{CC} + 0.3	V
Input low voltage	V _{IL}	- 0.3*	—	0.8	V

* V_{IL} = - 3.0V Min. for pulse width less than 50ns.

Electrical Characteristics

• DC and operating characteristics

(V_{CC} = 5V ± 10%, GND = 0V, T_a = 0 to +70°C)

Item	Symbol	Test conditions	-70L/85L/10L/12L			-70LL/85LL/10LL/12LL			Unit
			Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Input leakage current	I _{LI}	V _{IN} = GND to V _{CC}	-0.5	—	0.5	-0.5	—	0.5	μA
Output leakage current	I _{LO}	$\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$ V _{I/O} = GND to V _{CC}	-0.5	—	0.5	-0.5	—	0.5	μA
Operating power supply current	I _{CC1}	$\overline{CE} = V_{IL}$, V _{IN} = V _{IH} or V _{IL} , I _{OUT} = 0mA	—	3	10	—	3	10	mA
		$\overline{CE} \leq 0.2V$ V _{IN} $\leq 0.2V$ or $\geq V_{CC} - 0.2V$	—	1	5	—	1	5	
Average operating current	I _{CC2}	Cycle = Min, Duty = 100%, I _{OUT} = 0mA	70L/70LL	—	30	50	—	30	mA
			85L/85LL	—	25	50	—	25	
			10L/10LL	—	23	50	—	23	
			12L/12LL	—	20	50	—	20	
Standby current	I _{SB1}	$\overline{CE} \geq V_{CC} - 0.2V$	0 to 70°C	—	—	25	—	—	μA
			0 to 40°C	—	—	5	—	—	
			25°C	—	0.5	2	—	0.2	
	I _{SB2}	$\overline{CE} = V_{IH}$	—	0.4	2	—	0.4	2	mA
Output high voltage	V _{OH}	I _{OH} = -1.0mA	2.4	—	—	2.4	—	—	V
Output low voltage	V _{OL}	I _{OL} = 2.1mA	—	—	0.4	—	—	0.4	V

* V_{CC} = 5V, T_a = 25°C

I/O capacitance

(T_a = 25°C, f = 1MHz)

Item	Symbol	Test conditions	Min.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} = 0V	—	6	pF
I/O capacitance	C _{I/O}	V _{I/O} = 0V	—	8	pF

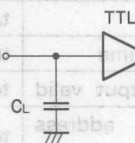
Note) This parameter is sampled and is not 100% tested.

AC characteristics

● AC test conditions

(V_{CC} = 5V ± 10%, T_a = 0 to +70°C)

Item	Conditions
Input pulse high level	V _{IH} = 2.2V
Input pulse low level	V _{IL} = 0.8V
Input rise time	t _r = 5ns
Input fall time	t _f = 5ns
Input and output reference level	1.5V
Output load conditions	85L/85LL/10L/10LL/12L/12LL C _L * = 100pF, 1TTL
	70L/70LL C _L * = 30pF, 1TTL

* C_L includes scope and jig capacitances.

Item	Symbol	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
Write to output in high Σ	t _{WH} *	0	25	0	25	0	25	0	25
Output active from end of write	t _{OW}	10	—	10	—	10	—	10	—
Write recovery time (CE)	t _{WR}	0	—	0	—	0	—	0	—
Write recovery time (WE)	t _{WR}	0	—	0	—	0	—	0	—
Address setup time	t _{AS}	0	—	0	—	0	—	0	—
Write pulse width	t _{WP}	80	—	80	—	80	—	70	—
Data hold from write time	t _{DH}	0	—	0	—	0	—	0	—
Data to write time overlap	t _{DW}	30	—	30	—	30	—	40	—
Chip enable to end of write	t _{CEW}	65	—	75	—	80	—	100	—
Address valid to end of write	t _{AW}	85	—	75	—	80	—	100	—
Write cycle time	t _{WC}	70	—	85	—	100	—	120	—

* t_{WH} is defined as the time required for outputs to turn to high impedance state and is referred to as output voltage level.

Item	Symbol	-70L/70LL		-85L/85LL		-10L/10LL		-12L/12LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t _{RC}	70	—	85	—	100	—	120	—	ns
Address access time	t _{AA}	—	70	—	85	—	100	—	120	ns
Chip enable access time	t _{CO}	—	70	—	85	—	100	—	120	ns
Output enable to output valid	t _{OE}	—	35	—	45	—	50	—	60	ns
Output hold from address change	t _{OH}	20	—	20	—	20	—	20	—	ns
Chip enable to output in low Z (CE)	t _{LZ}	10	—	10	—	10	—	10	—	ns
Output enable to output in low Z (OE)	t _{OLZ}	5	—	5	—	5	—	5	—	ns
Chip disable to output in high Z (CE)	t _{HZ} *	0	30	0	30	0	30	0	30	ns
Chip disable to output in high Z (OE)	t _{OHZ} *	0	30	0	30	0	30	0	30	ns

* t_{HZ} and t_{OHZ} are defined as the time required for outputs to turn to high impedance state and are not referred to as output voltage levels.

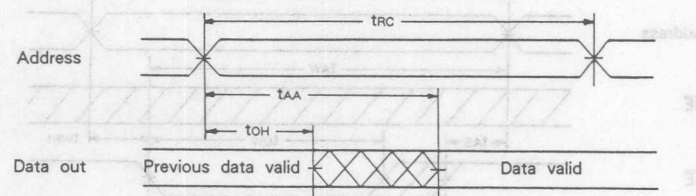
• Write cycle

Item	Symbol	-70L/70LL		-85L/85LL		-10L/10LL		-12L/12LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t _{WC}	70	—	85	—	100	—	120	—	ns
Address valid to end of write	t _{AW}	65	—	75	—	80	—	100	—	ns
Chip enable to end of write	t _{CW}	65	—	75	—	80	—	100	—	ns
Data to write time overlap	t _{DW}	30	—	30	—	35	—	40	—	ns
Data hold from write time	t _{DH}	0	—	0	—	0	—	0	—	ns
Write pulse width	t _{WP}	50	—	50	—	60	—	70	—	ns
Address setup time	t _{AS}	0	—	0	—	0	—	0	—	ns
Write recovery time (WE)	t _{WR}	0	—	0	—	0	—	0	—	ns
Write recovery time (CE)	t _{WR1}	0	—	0	—	0	—	0	—	ns
Output active from end of write	t _{OW}	10	—	10	—	10	—	10	—	ns
Write to output in high Z	t _{WHZ} *	0	25	0	25	0	25	0	25	ns

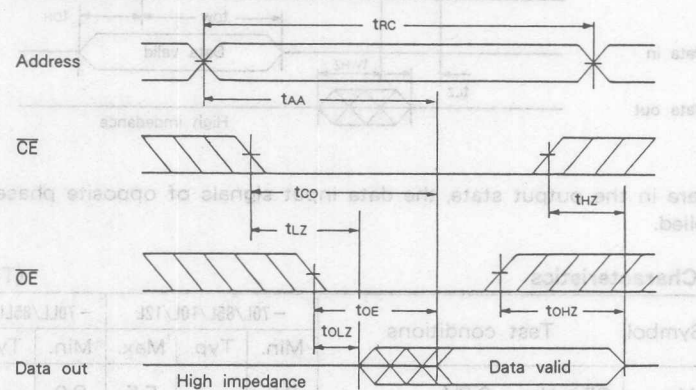
* t_{WHZ} is defined as the time required for outputs to turn to high impedance state and is not referred to as output voltage level.

Timing Waveform

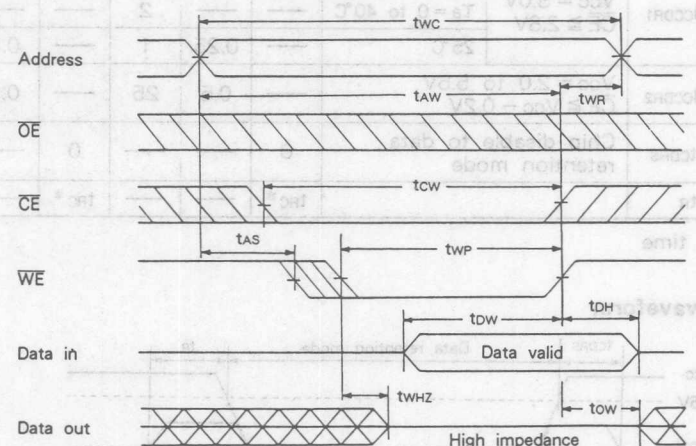
- Read cycle (1) : $\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$



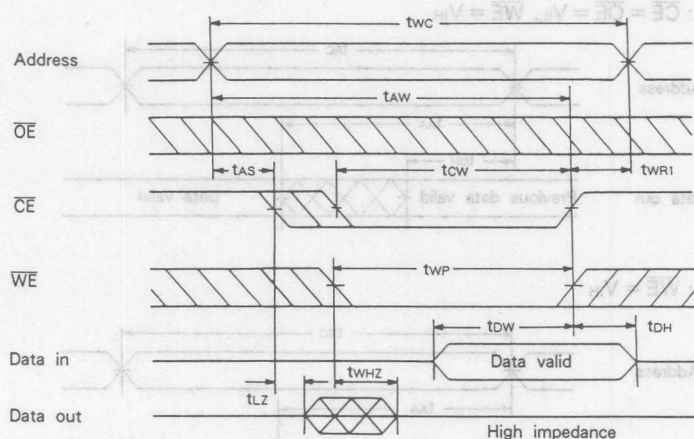
- Read cycle (2) : $\overline{WE} = V_{IH}$



- Write cycle (1) : $\overline{WE}$ control



• Write cycle (2) : $\overline{CE}$ control



During I/O pins are in the output state, the data input signals of opposite phase to the output must not be applied.

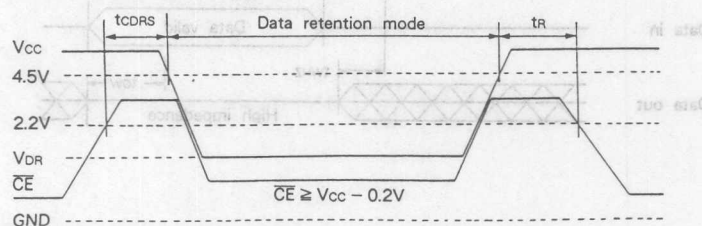
Data Retention Characteristics

($T_a = 0$ to 70°C)

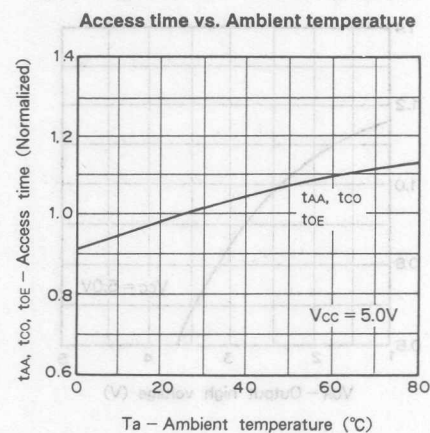
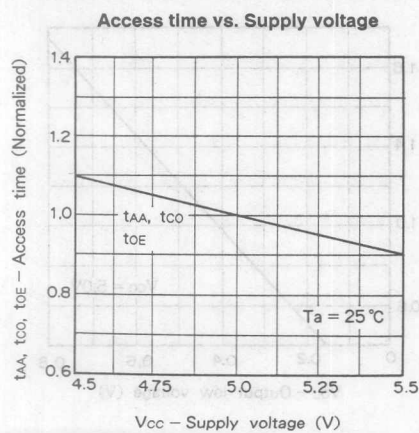
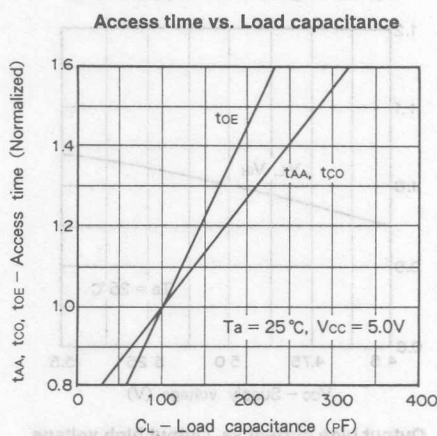
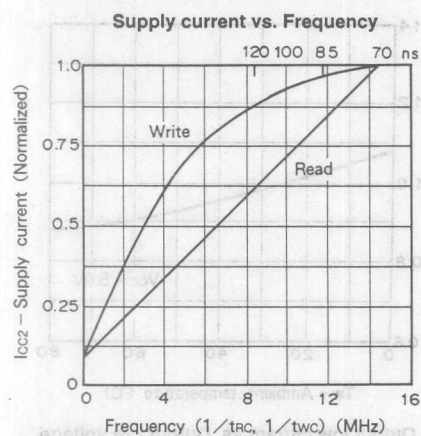
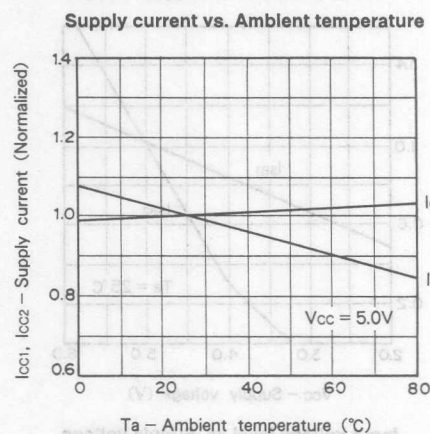
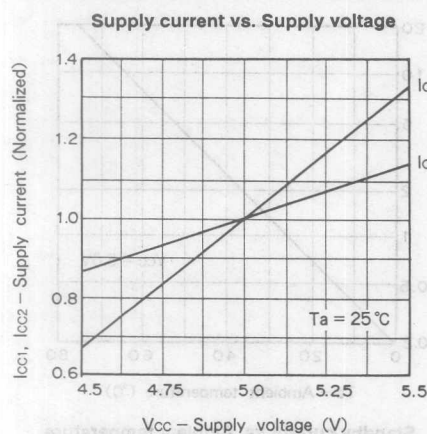
Item	Symbol	Test conditions	- 70L/85L/10L/12L			- 70LL/85LL/10LL/12LL			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Data retention voltage	V_{DR}	$\overline{CE} \geq V_{CC} - 0.2V$	2.0	—	5.5	2.0	—	5.5	V
Data retention current	I_{CCDR1}	$V_{CC} = 3.0V$ $\overline{CE} \geq 2.8V$	$T_a = 0$ to 70°C			$T_a = 0$ to 70°C			μA
			—	—	10	—	—	3	
		$T_a = 0$ to 40°C	—	—	2	—	—	0.6	
		25°C	—	0.25	1	—	0.1	0.3	
	I_{CCDR2}	$V_{CC} = 2.0$ to $5.5V$ $\overline{CE} \geq V_{CC} - 0.2V$	—	0.5	25	—	0.2	5	μA
Data retention setup time	t_{CDRS}	Chip disable to data retention mode	0	—	—	0	—	—	ns
Recovery time	t_R		t_{RC}^*	—	—	t_{RC}^*	—	—	ns

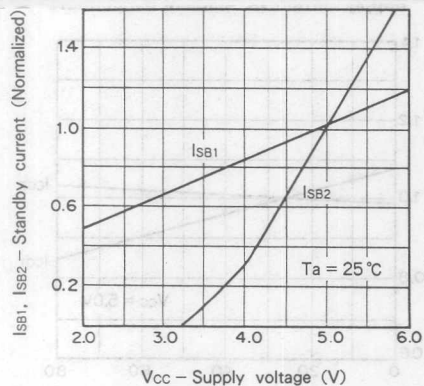
* t_{RC} : Read cycle time

Data retention waveform

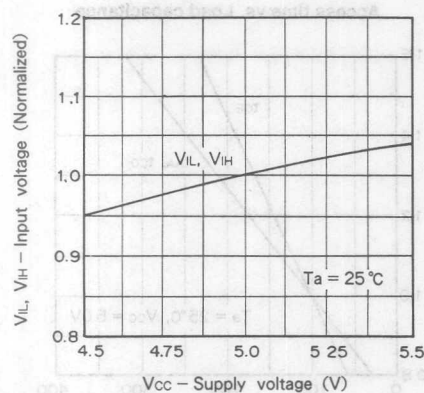


Example of Representative Characteristics

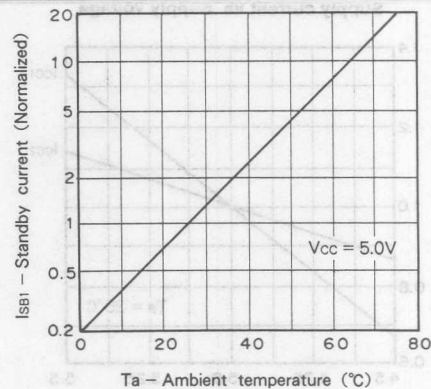
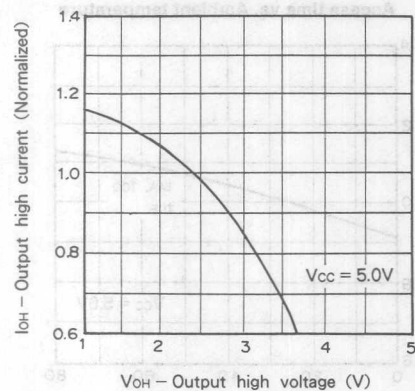




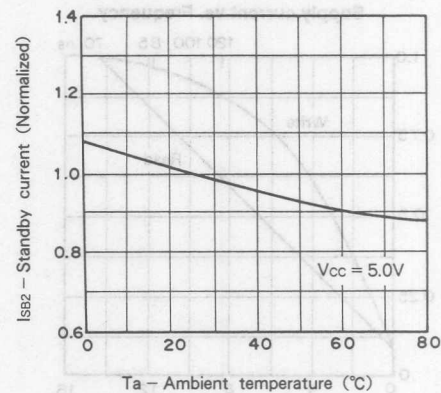
Input voltage level vs. Supply voltage



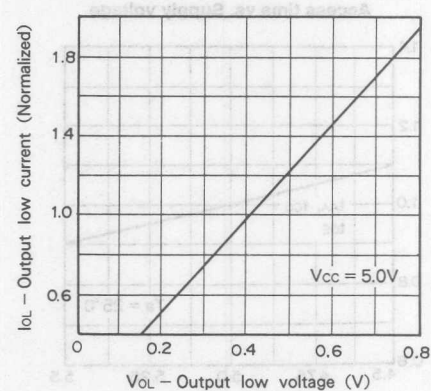
Output high current vs. Output high voltage



Standby current vs. Ambient temperature



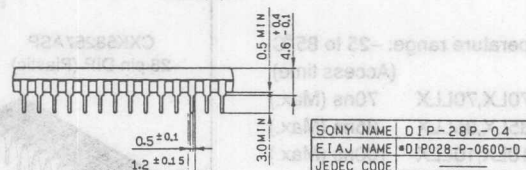
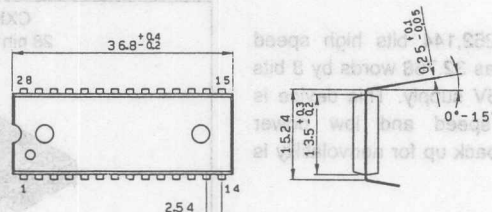
Output low current vs. Output low voltage



Package Outline Unit : mm

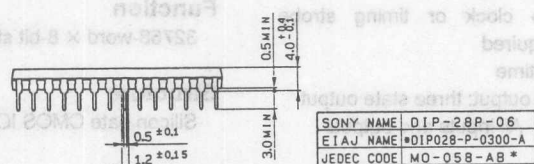
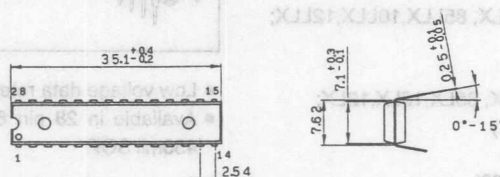
CXK58257AP

28pin DIP (Plastic) 600mil 4.2g



CXK58257ASP

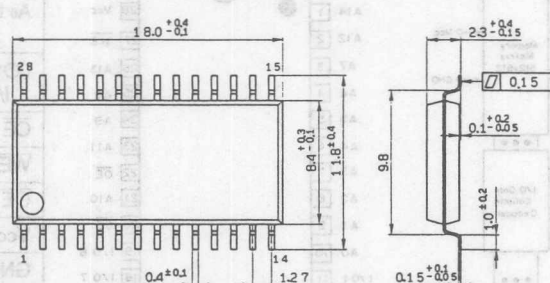
28pin DIP (Plastic) 300mil 2.0g



* (Similar)

CXK58257AM

28pin SOP (Plastic) 450mil 0.7g



SONY NAME	SOP-28P-L05
EIAJ NAME	*SOP028-P-0450-A
JEDEC CODE	

SONY CXK58257AP/ASP/AM

-70LX/85LX/10LX/12LX
-70LLX/85LLX/10LLX/12LLX

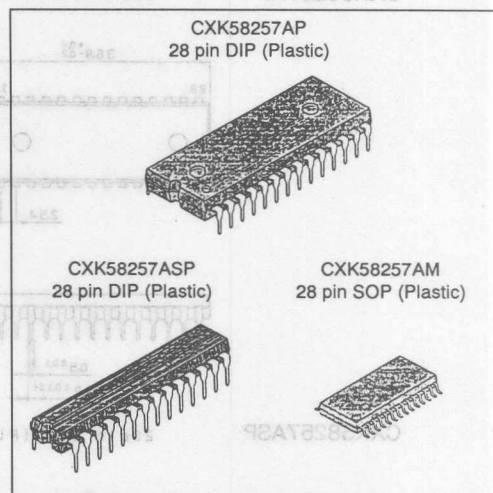
32768-word × 8-bit High Speed CMOS Static RAM

Description

CXK58257AP/ASP/AM is 262,144 bits high speed CMOS static RAM organized as 32,768 words by 8 bits and operates from a single 5V supply. This device is suitable for use in high speed and low power applications in which battery back up for nonvolatility is required.

Features

- Extended operating temperature range: -25 to 85 °C
- Fast access time: (Access time)
 - CXK58257AP/ASP/AM-70LX,70LLX 70ns (Max.)
 - CXK58257AP/ASP/AM-85LX,85LLX 85ns (Max.)
 - CXK58257AP/ASP/AM-10LX,10LLX 100ns (Max.)
 - CXK58257AP/ASP/AM-12LX,12LLX 120ns (Max.)
- Low power operation:
 - CXK58257AP/ASP/AM-70LLX, 85LLX,10LLX,12LLX;
 - Standby : 1 μW (Typ.)
 - Operation : 15mW (Typ.)
 - CXK58257AP/ASP/AM-70LX, 85LX,10LX,12LX;
 - Standby : 2.5 μW (Typ.)
 - Operation : 15mW (Typ.)
- Single +5V supply: +5V ± 10%
- Fully static memory...No clock or timing strobe required
- Equal access and cycle time
- Common data input and output: three state output
- Directly TTL compatible: All inputs and outputs



- Low voltage data retention: 2.0V (Min.)
- Available in 28 pin 600mil DIP, 300mil DIP and 450mil SOP

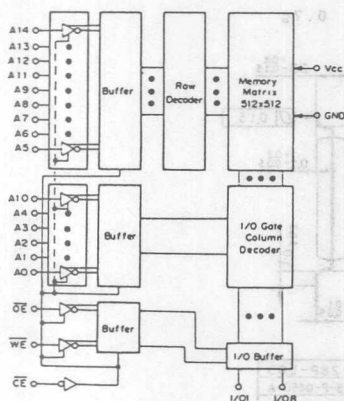
Function

32768-word × 8-bit static RAM

Structure

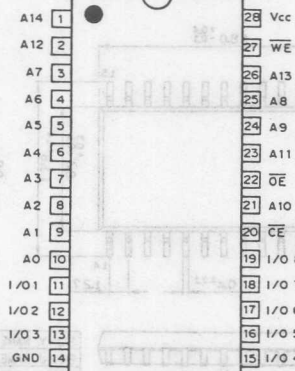
Silicon gate CMOS IC

Block diagram



Pin Configuration

(Top View)



Pin Description

Symbol	Description
A ₀ to A ₁₄	Address input
I/O ₁ to I/O ₈	Data input/output
CE	Chip enable input
WE	Write enable input
OE	Output enable input
V _{cc}	+5V power supply
GND	Ground

Sony reserves the right to change products and specifications without prior notice. This information does not convey any license by any implication or otherwise under any patents or other right. Application circuits shown, if any, are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits.

Absolute Maximum Ratings

(Ta=25°C, GND=0V)

Item	Symbol	Rating	Unit
Supply voltage	V _{CC}	− 0.5 to +7.0	V
Input voltage	V _{IN}	− 0.5 * to V _{CC} +0.5	V
Input and output voltage	V _{IO}	− 0.5 * to V _{CC} +0.5	V
Allowable power dissipation	P _D	CXK58257AP/ASP	1.0
		CXK58257AM	0.7
			W
Operating temperature	T _{opr}	− 25 to +85	°C
Storage temperature	T _{stg}	− 55 to +150	°C
Soldering temperature • time	T _{solder}	260 • 10	°C • sec

* V_{IN}, V_{IO} = − 3.0V Min. for pulse width less than 50ns.

Truth Table

CE	OE	WE	Mode	I/O1 to I/O8	V _{CC} Current
H	x	x	Not selected	High Z	I _{SB1} , I _{SB2}
L	H	H	Not selected	High Z	I _{CC1} , I _{CC2}
L	L	H	Read	Data out	I _{CC1} , I _{CC2}
L	x	L	Write	Data in	I _{CC1} , I _{CC2}

x : "H" or "L"

DC Recommended Operating Conditions (Ta = − 25 to +85°C, GND=0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Input high voltage	V _{IH}	2.2	—	V _{CC} +0.3	V
Input low voltage	V _{IL}	− 0.3 *	—	0.8	V

* V_{IL} = − 3.0V Min. for pulse width less than 50ns.

Item	Symbol	Test conditions	-70LX/85LX/10LX/12LX			-70LLX/85LLX/10LLX/12LLX			Unit
			Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Input leakage current	I _{II}	V _{IN} =GND to V _{CC}	-0.5	—	0.5	-0.5	—	0.5	μA
Output leakage current	I _{LO}	$\overline{CE}=V_{IH}$ or $\overline{OE}=V_{IH}$ V _{I/O} =GND to V _{CC}	-0.5	—	0.5	-0.5	—	0.5	μA
Operating power supply current	I _{CC1}	$\overline{CE}=V_{IL}$, V _{IN} =V _{IH} or V _{IL} , I _{OUT} =0mA	—	3	10	—	3	10	mA
		$\overline{CE} \leq 0.2V$ V _{IN} $\leq 0.2V$ or $\geq V_{CC}-0.2V$	—	1	5	—	1	5	
Average operating current	I _{CC2}	Cycle=Min, Duty=100% I _{OUT} =0mA	70LX/70LLX	—	30	60	—	30	mA
			85LX/85LLX	—	25	60	—	25	
			10LX/10LLX	—	23	60	—	23	
			12LX/12LLX	—	20	60	—	20	
Standby current	I _{SB1}	$\overline{CE} \geq V_{CC}-0.2V$	-25 to 85 °C	—	—	50	—	—	μA
			-25 to 70 °C	—	—	25	—	—	
			-25 to 40 °C	—	—	5	—	—	
			25 °C	—	0.5	2	—	0.2	
	I _{SB2}	$\overline{CE}=V_{IH}$	—	0.4	2	—	0.4	2	mA
Output high voltage	V _{OH}	I _{OH} =-1.0mA	2.4	—	—	2.4	—	—	V
Output low voltage	V _{OL}	I _{OL} =2.1mA	—	—	0.4	—	—	0.4	V

* V_{CC}=5V, T_a=25 °C

I/O capacitance

(T_a=25 °C, f=1MHz)

Item	Symbol	Test conditions	Min.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} =0V	—	6	pF
I/O capacitance	C _{I/O}	V _{I/O} =0V	—	8	pF

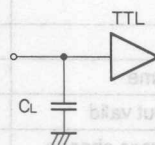
Note) This parameter is sampled and is not 100% tested.

AC characteristics

● AC test conditions

(V_{CC}=5V ± 10%, T_a=-25 to +85°C)

Item	Conditions
Input pulse high level	V _{IH} =2.4V
Input pulse low level	V _{IL} =0.6V
Input rise time	t _r =5ns
Input fall time	t _f =5ns
Input and output reference level	1.5V
Output load conditions	85LX/85LLX/10LX/ 10LLX/12LX/12LLX/
	70LX/70LLX
	C _L * =100pF, 1TTL
	C _L * =30pF, 1TTL

* C_L includes scope and jig capacitances.

* t_{tr} and t_{off} are defined as the time required for outputs to turn to high impedance state and are not related to as output voltage levels.

Item	Symbol	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Write cycle time	t _{WC}	70	—	85	—	—	—	100	—	120	—	ns
Address valid to end of write	t _{AV}	65	—	75	—	80	—	100	—	100	—	ns
Chip enable to end of write	t _{CE}	65	—	75	—	80	—	100	—	100	—	ns
Data to write time overlap	t _{DO}	30	—	30	—	35	—	40	—	40	—	ns
Data hold from write time	t _{DH}	0	—	0	—	0	—	0	—	0	—	ns
Write pulse width	t _{WP}	30	—	50	—	80	—	70	—	70	—	ns
Address setup time	t _{AS}	0	—	0	—	0	—	0	—	0	—	ns
Write recovery time (WE)	t _{WR}	5	—	5	—	5	—	5	—	5	—	ns
Write recovery time (CE)	t _{WR}	0	—	0	—	0	—	0	—	0	—	ns
Output active from end of write	t _{OW}	10	—	10	—	10	—	10	—	10	—	ns
Write to output in high Z	t _{WHS} *	0	25	0	25	0	25	0	25	0	25	ns

* t_{WHS} is defined as the time required for outputs to turn to high impedance state and is not related to as output voltage level.

• Read cycle

Item	Symbol	-70LX/70LLX		-85LX/85LLX		-10LX/10LLX		-12LX/12LLX		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t _{RC}	70	—	85	—	100	—	120	—	ns
Address access time	t _{AA}	—	70	—	85	—	100	—	120	ns
Chip enable access time	t _{CO}	—	70	—	85	—	100	—	120	ns
Output enable to output valid	t _{OE}	—	35	—	45	—	50	—	60	ns
Output hold from address change	t _{OH}	5	—	10	—	10	—	10	—	ns
Chip enable to output in low Z ($\overline{CE}$)	t _{LZ}	10	—	10	—	10	—	10	—	ns
Output enable to output in low Z ($\overline{OE}$)	t _{OLZ}	5	—	5	—	5	—	5	—	ns
Chip disable to output in high Z ($\overline{CE}$)	t _{HZ} *	0	30	0	30	0	30	0	30	ns
Chip disable to output in high Z ($\overline{OE}$)	t _{OHZ} *	0	30	0	30	0	30	0	30	ns

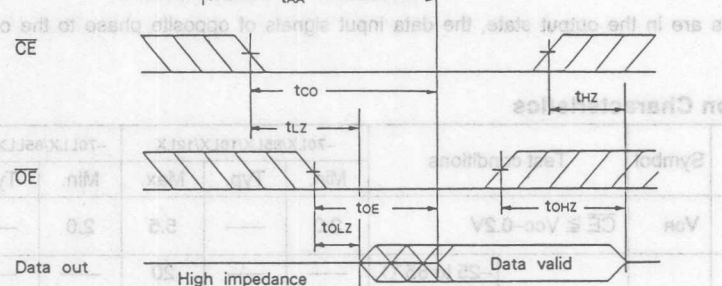
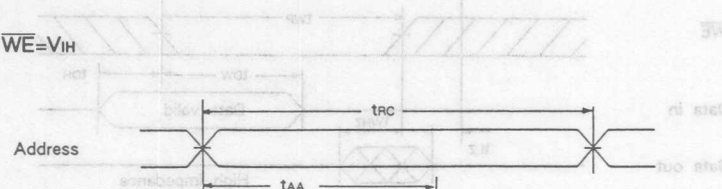
* t_{HZ} and t_{OHZ} are defined as the time required for outputs to turn to high impedance state and are not referred to as output voltage levels.

• Write cycle

Item	Symbol	-70LX/70LLX		-85LX/85LLX		-10LX/10LLX		-12LX/12LLX		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t _{WC}	70	—	85	—	100	—	120	—	ns
Address valid to end of write	t _{AW}	65	—	75	—	80	—	100	—	ns
Chip enable to end of write	t _{CW}	65	—	75	—	80	—	100	—	ns
Data to write time overlap	t _{DW}	30	—	30	—	35	—	40	—	ns
Data hold from write time	t _{DH}	0	—	0	—	0	—	0	—	ns
Write pulse width	t _{WP}	50	—	50	—	60	—	70	—	ns
Address setup time	t _{AS}	0	—	0	—	0	—	0	—	ns
Write recovery time ($\overline{WE}$)	t _{WR}	5	—	5	—	5	—	5	—	ns
Write recovery time ($\overline{CE}$)	t _{WR1}	0	—	0	—	0	—	0	—	ns
Output active from end of write	t _{OW}	10	—	10	—	10	—	10	—	ns
Write to output in high Z	t _{WHZ} *	0	25	0	25	0	25	0	25	ns

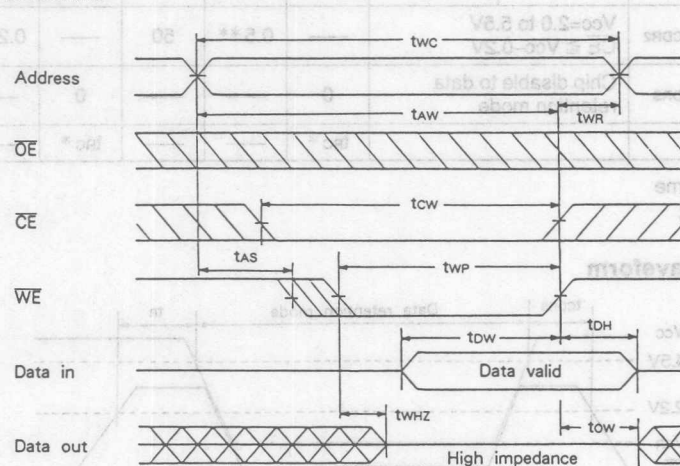
* t_{WHZ} is defined as the time required for outputs to turn to high impedance state and is not referred to as output voltage level.

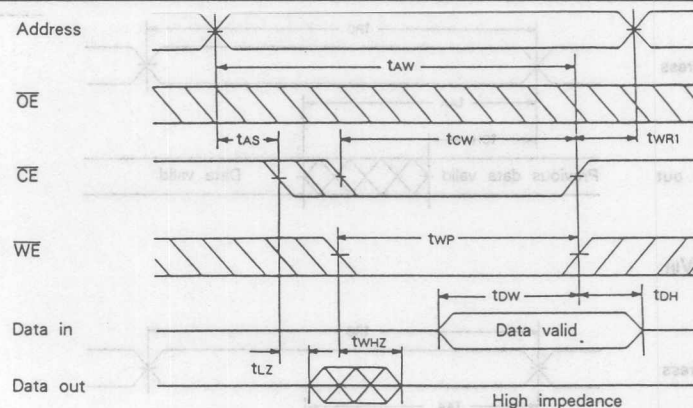
- Read cycle (2) : $\overline{WE}=V_{IH}$



Timing diagram for Write cycle (1) showing WE control, Address, and Data out signals. The diagram includes timing parameters: t_{LZ} (load to Z), t_{OE} (output enable), t_{OHZ} (output high Z), t_{OLZ} (output low Z), and t_{OW} (output write).

- Write cycle (1) : $\overline{WE}$ control





During I/O pins are in the output state, the data input signals of opposite phase to the output must not be applied.

Data Retention Characteristics

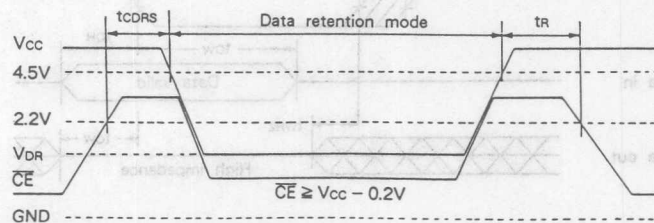
(Ta=-25 to 85 °C)

Item	Symbol	Test conditions	-70LX/85LX/10LX/12LX			-70LLX/85LLX/10LLX/12LLX			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Data retention voltage	V _{DR}	$\overline{CE} \geq V_{CC}-0.2V$	2.0	—	5.5	2.0	—	5.5	V
Data retention current	I _{CCDR1}	V _{CC} =3.0V $\overline{CE} \geq 2.8V$	-25 to 85 °C	—	20	—	—	6	μA
			-25 to 70 °C	—	10	—	—	3	
			-25 to 40 °C	—	2	—	—	0.6	
			25 °C	—	0.25	—	0.1	0.3	
	I _{CCDR2}	V _{CC} =2.0 to 5.5V $\overline{CE} \geq V_{CC}-0.2V$	—	0.5**	50	—	0.2**	10	μA
Data retention setup time	t _{CDRS}	Chip disable to data retention mode	0	—	—	0	—	—	ns
Recovery time	t _R		t _{RC} *	—	—	t _{RC} *	—	—	ns

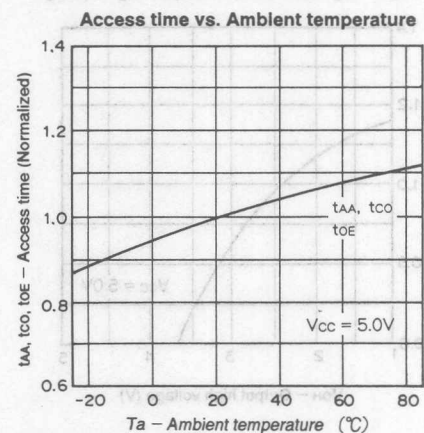
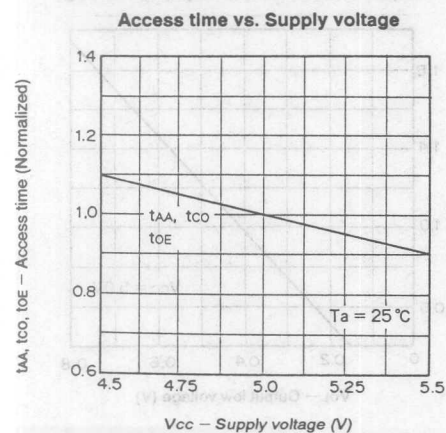
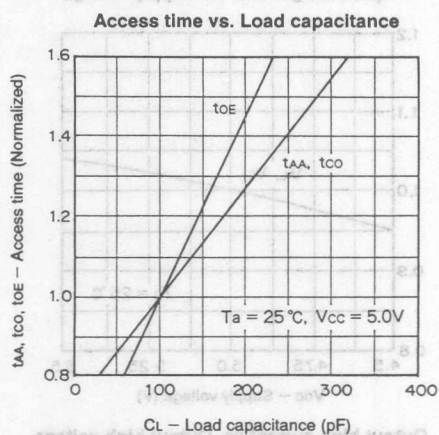
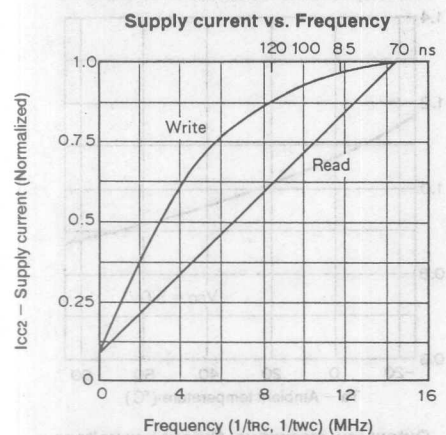
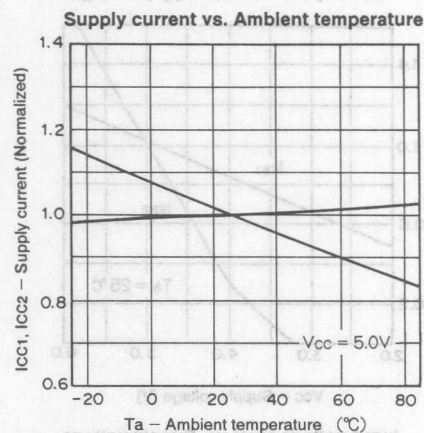
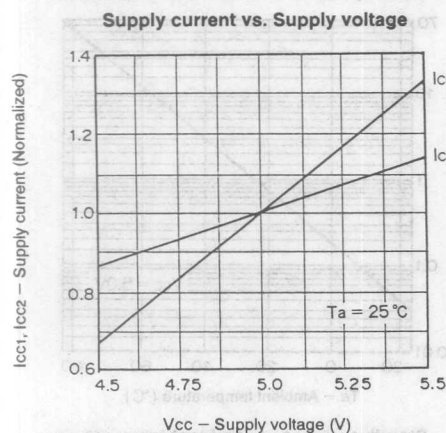
* t_{RC} : Read cycle time

** V_{CC}=5V, Ta=25 °C

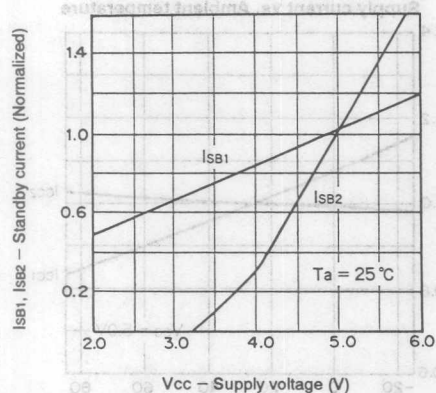
Data retention waveform



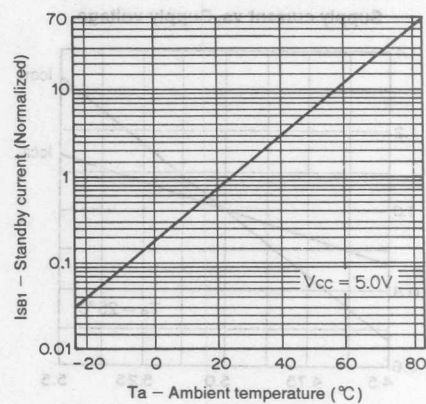
Example of Representative Characteristics



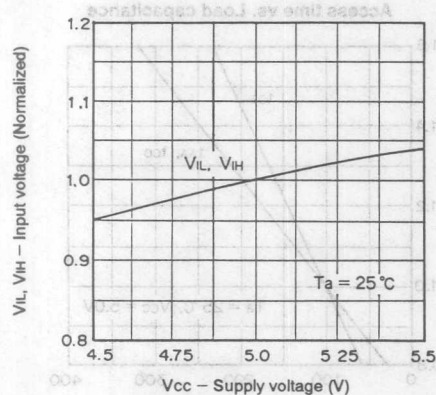
Standby current vs. Supply voltage



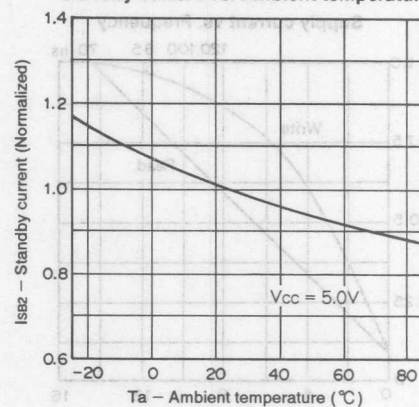
Standby current vs. Ambient temperature



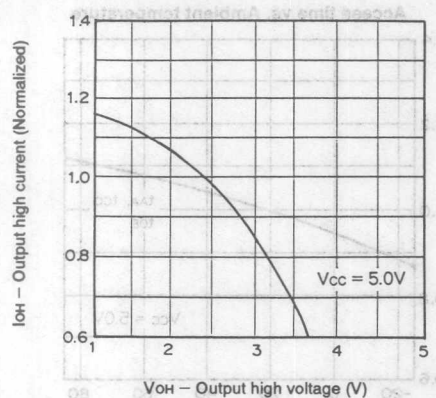
Input voltage level vs. Supply voltage



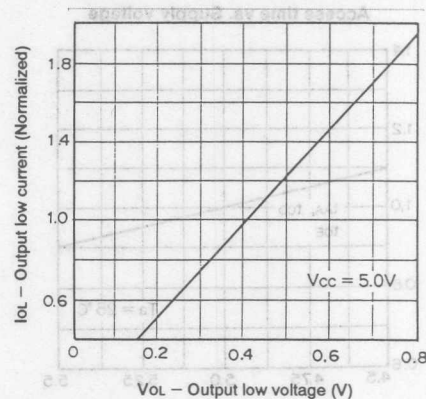
Standby current vs. Ambient temperature



Output high current vs. Output high voltage



Output low current vs. Output low voltage

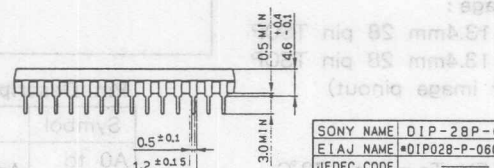
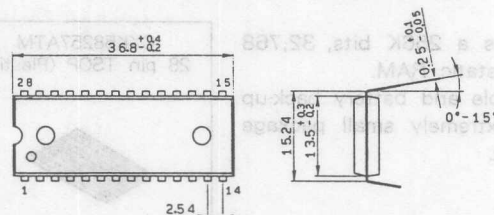


Package Outline

Unit : mm

CXK58257AP

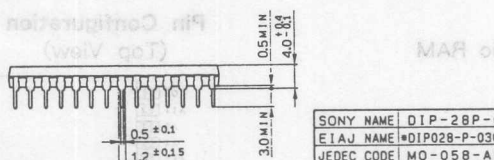
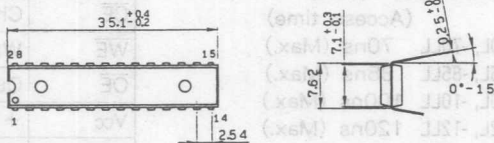
28pin DIP (Plastic) 600mil 4.2g



SONY NAME	DIP-28P-04
EIAJ NAME	*DIP028-P-0600-0
JEDEC CODE	

CXK58257ASP

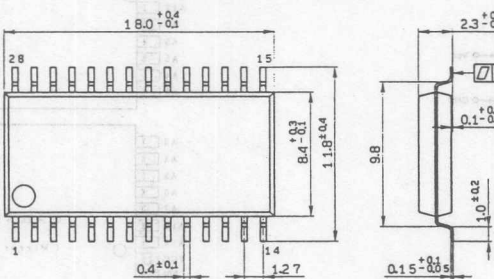
28pin DIP (Plastic) 300mil 2.0g



SONY NAME	DIP-28P-06
EIAJ NAME	*DIP028-P-0300-A
JEDEC CODE	MO-05-05-05-05-05-05-05-05

CXK58257AM

28pin SOP (Plastic) 450mil 0.7g



SONY NAME	SOP-28P-L05
EIAJ NAME	*SOP028-P-0450-A
JEDEC CODE	

165

Description

CXK58257ATM/AYM is a 256K bits, 32,768 words by 8 bits, CMOS static RAM.

It is suitable for portable and battery back-up systems which require extremely small package and low stand-by current.

Features

- Thin Small-outline package :
CXK58257ATM : 8mm×13.4mm 28 pin TSOP
CXK58257AYM : 8mm×13.4mm 28 pin TSOP
(Mirror image pinout)
- Low stand-by current :
L-Version :
25 μ A (Max.) @ Vcc = 5.5V, Ta = 0 to 70°C
LL-Version :
5 μ A (Max.) @ Vcc = 5.5V, Ta = 0 to 70°C
- Low voltage data retention : 2.0V (Min.)
- Fast access time : (Access time)
CXK58257ATM/AYM-70L, -70LL 70ns (Max.)
CXK58257ATM/AYM-85L, -85LL 85ns (Max.)
CXK58257ATM/AYM-10L, -10LL 100ns (Max.)
CXK58257ATM/AYM-12L, -12LL 120ns (Max.)
- Single +5V Supply : 5V $\pm$ 10%

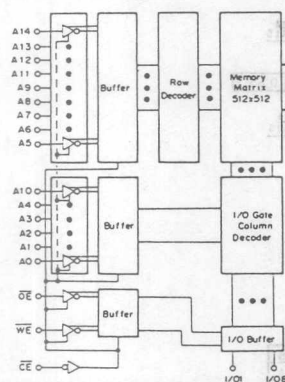
Function

32768-word $\times$ 8-bit static RAM

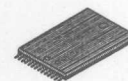
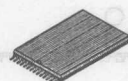
Structure

Silicon gate CMOS IC

Block Diagram



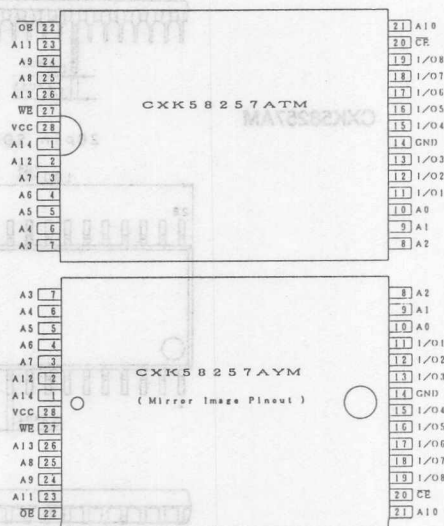
CXK58257ATM 28 pin TSOP (Plastic) CXK58257AYM 28 pin TSOP (Plastic)



Pin Description

Symbol	Description
A0 to A14	Address input
I/O0 to I/O8	Data input/output
CE	Chip enable input
WE	Write enable input
OE	Output enable input
Vcc	+5V power supply
GND	Ground

Pin Configuration (Top View)



Absolute Maximum Ratings

(Ta = 25 °C, GND = 0V)

Item	Symbol	Rating	Unit
Supply voltage	V _{CC}	- 0.5 to + 7.0	V
Input voltage	V _{IN}	- 0.5* to V _{CC} + 0.5	V
Input and output voltage	V _{I/O}	- 0.5* to V _{CC} + 0.5	V
Allowable power dissipation	P _D	0.7	W
Operating temperature	T _{opr}	0 to + 70	°C
Storage temperature	T _{stg}	- 55 to + 150	°C
Soldering temperature	T _{solder}	235 ± 10	°C • sec

* V_{IN}, V_{I/O} = - 3.0V Min. for pulse width less than 50ns.

Truth Table

CE	OE	WE	Mode	I/O1 to I/O8	V _{CC} Current
H	x	x	Not selected	High Z	I _{SB1} , I _{SB2}
L	H	H	Not selected	High Z	I _{CC1} , I _{CC2}
L	L	H	Read	Data out	I _{CC1} , I _{CC2}
L	x	L	Write	Data in	I _{CC1} , I _{CC2}

x : "H" or "L"

DC Recommended Operating Conditions (Ta = 0 to + 70 °C, GND = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Input high voltage	V _{IH}	2.2	—	V _{CC} + 0.3	V
Input low voltage	V _{IL}	- 0.3*	—	0.8	V

* V_{IL} = - 3.0V Min. for pulse width less than 50ns.

Item	Symbol	Test conditions	Min.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} = 0V	—	8	pF
I/O capacitance	C _{I/O}	V _{I/O} = 0V	—	8	pF

(Note) This parameter is sampled and is not 100% tested.

Electrical Characteristics

• DC and operating characteristics

(V_{CC} = 5V ± 10%, GND = 0V, T_a = 0 to +70 °C)

Item	Symbol	Test conditions	- 70L/85L/10L/12L			- 70LL/85LL/10LL/12LL			Unit	
			Min.	Typ.*	Max.	Min.	Typ.*	Max.		
Input leakage current	I _{LI}	V _{IN} = GND to V _{CC}	- 0.5	—	0.5	- 0.5	—	0.5	μA	
Output leakage current	I _{LO}	$\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$ V _{I/O} = GND to V _{CC}	- 0.5	—	0.5	- 0.5	—	0.5	μA	
Operating power supply current	I _{CC1}	$\overline{CE} = V_{IL}$, V _{IN} = V _{IH} or V _{IL} , I _{OUT} = 0mA	—	3	10	—	3	10	mA	
		$\overline{CE} \leq 0.2V$ V _{IN} $\leq 0.2V$ or $\geq V_{CC} - 0.2V$	—	1	5	—	1	5		
Average operating current	I _{CC2}	Cycle = Min, Duty = 100 %, I _{OUT} = 0mA	70L/70LL	—	30	50	—	30	50	mA
			85L/85LL	—	25	50	—	25	50	
			10L/10LL	—	23	50	—	23	50	
			12L/12LL	—	20	50	—	20	50	
Standby current	I _{SB1}	$\overline{CE} \geq V_{CC} - 0.2V$	0 to 70°C	—	—	25	—	—	5	μA
			0 to 40°C	—	—	5	—	—	1	
			25°C	—	0.5	2	—	0.2	0.5	
	I _{SB2}	$\overline{CE} = V_{IH}$	—	0.4	2	—	0.4	2	mA	
Output high voltage	V _{OH}	I _{OH} = - 1.0mA	2.4	—	—	2.4	—	—	V	
Output low voltage	V _{OL}	I _{OL} = 2.1mA	—	—	0.4	—	—	0.4	V	

* V_{CC} = 5V, T_a = 25 °C

I/O capacitance

(T_a = 25 °C, f = 1MHz)

Item	Symbol	Test conditions	Min.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} = 0V	—	6	pF
I/O capacitance	C _{I/O}	V _{I/O} = 0V	—	8	pF

Note) This parameter is sampled and is not 100% tested.

AC characteristics

● AC test conditions

(V_{CC} = 5V ± 10%, T_a = 0 to +70°C)

Item	Conditions
Input pulse high level	V _{IH} = 2.2V
Input pulse low level	V _{IL} = 0.8V
Input rise time	t _r = 5ns
Input fall time	t _f = 5ns
Input and output reference level	1.5V
Output load conditions	85L/85LL/10L/10LL/12L/12LL
	70L/70LL
	C _L * = 100pF, 1TTL
	C _L * = 30pF, 1TTL

Item	Symbol	Min.	Max.	Unit
Read cycle time	t _{RC}	70	—	ns
Address access time	t _{AA}	70	—	ns
Chip enable access time	t _{CE}	70	—	ns
Output enable to output valid	t _{OE}	35	—	ns
Output hold from address change	t _{OH}	30	—	ns
Chip enable to output in low	t _{LE}	10	—	ns
Output enable to output in high	t _{HE}	—	—	ns
Chip disable to output in high	t _{HD} *	0	30	ns
Chip disable to output in high	t _{OD} *	0	30	ns

* C_L includes scope and jig capacitances.

* t_{OH} and t_{OD} are defined as the time required for outputs to turn to high impedance state and are not referred to as output voltage levels.

Item	Symbol	Min.	Max.	Unit
Write cycle time	t _{WC}	70	—	ns
Address valid to end of write	t _{AW}	65	—	ns
Chip enable to end of write	t _{CEW}	65	—	ns
Data to write time overlap	t _{OW}	30	—	ns
Data hold from write time	t _{OH}	0	—	ns
Write pulse width	t _{WP}	50	—	ns
Address setup time	t _{AS}	0	—	ns
Write recovery time (WE)	t _{WR}	0	—	ns
Write recovery time (OE)	t _{WRH}	0	—	ns
Output active from end of write	t _{OW}	10	—	ns
Write to output in high Z	t _{WHS} *	0	25	ns

* t_{WHS} is defined as the time required for outputs to turn to high impedance state and is not referred to as output voltage level.

		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Read cycle time	t _{RC}	70	—	85	—	100	—	120	—	ns
Address access time	t _{AA}	—	70	—	85	—	100	—	120	ns
Chip enable access time	t _{CO}	—	70	—	85	—	100	—	120	ns
Output enable to output valid	t _{OE}	—	35	—	45	—	50	—	60	ns
Output hold from address change	t _{OH}	20	—	20	—	20	—	20	—	ns
Chip enable to output in low Z ($\overline{CE}$)	t _{LZ}	10	—	10	—	10	—	10	—	ns
Output enable to output in low Z ($\overline{OE}$)	t _{OLZ}	5	—	5	—	5	—	5	—	ns
Chip disable to output in high Z ($\overline{CE}$)	t _{HZ} *	0	30	0	30	0	30	0	30	ns
Chip disable to output in high Z ($\overline{OE}$)	t _{OHZ} *	0	30	0	30	0	35	0	40	ns

* t_{HZ} and t_{OHZ} are defined as the time required for outputs to turn to high impedance state and are not referred to as output voltage levels.

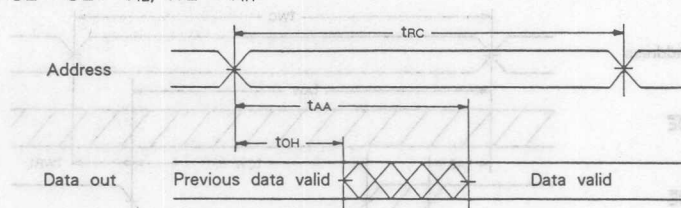
• Write cycle

Item	Symbol	-70L/70LL		-85L/85LL		-10L/10LL		-12L/12LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t _{WC}	70	—	85	—	100	—	120	—	ns
Address valid to end of write	t _{AW}	65	—	75	—	80	—	100	—	ns
Chip enable to end of write	t _{CW}	65	—	75	—	80	—	100	—	ns
Data to write time overlap	t _{DW}	30	—	30	—	35	—	40	—	ns
Data hold from write time	t _{DH}	0	—	0	—	0	—	0	—	ns
Write pulse width	t _{WP}	50	—	50	—	60	—	70	—	ns
Address setup time	t _{AS}	0	—	0	—	0	—	0	—	ns
Write recovery time ($\overline{WE}$)	t _{WR}	0	—	0	—	0	—	0	—	ns
Write recovery time ($\overline{CE}$)	t _{WR1}	0	—	0	—	0	—	0	—	ns
Output active from end of write	t _{OW}	10	—	10	—	10	—	10	—	ns
Write to output in high Z	t _{WHZ} *	0	25	0	25	0	25	0	25	ns

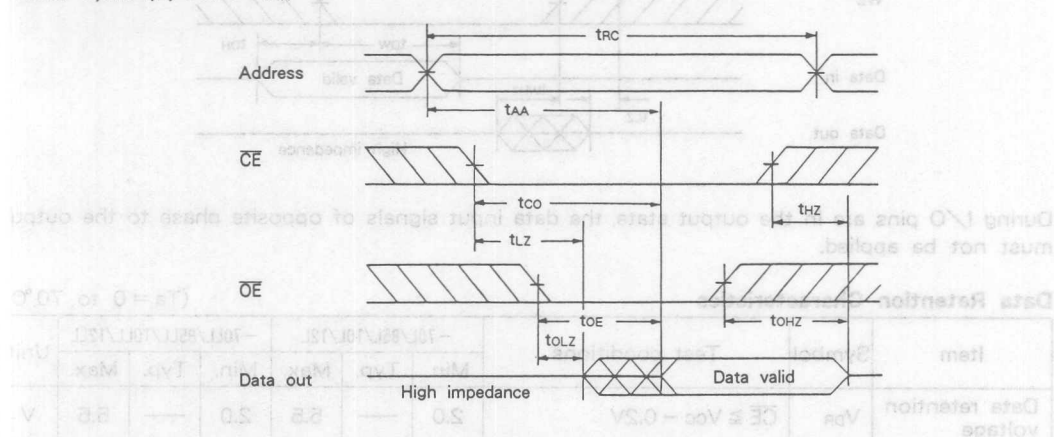
* t_{WHZ} is defined as the time required for outputs to turn to high impedance state and is not referred to as output voltage level.

Timing Waveform

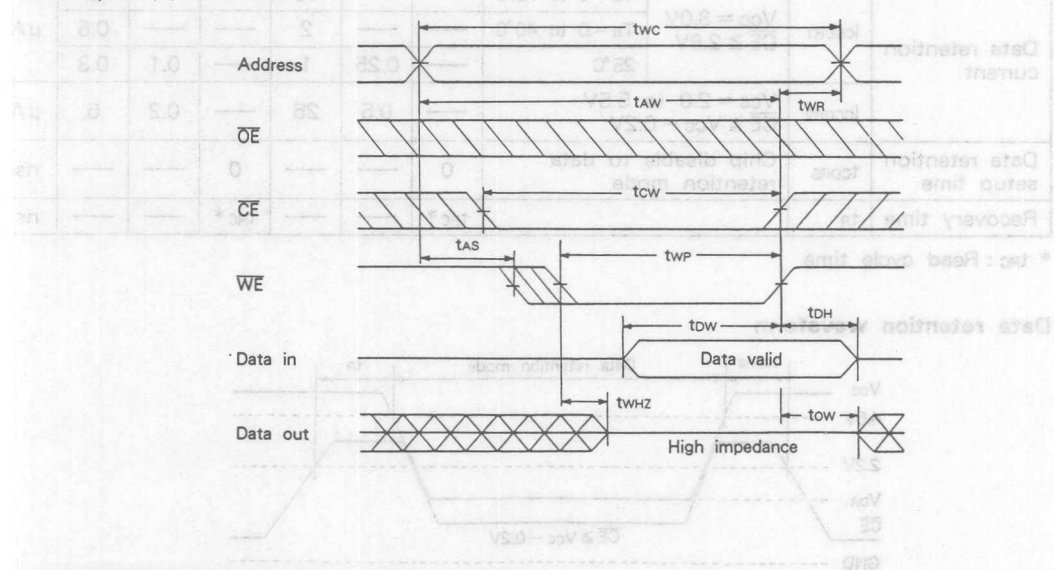
- Read cycle (1) : $\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$



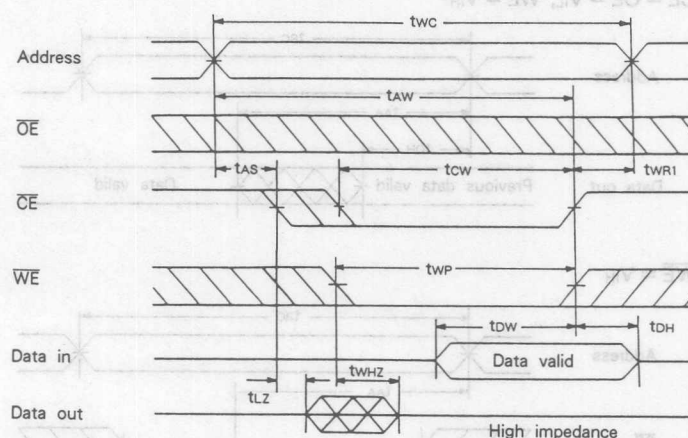
- Read cycle (2) : $\overline{WE} = V_{IH}$



- Write cycle (1) : $\overline{WE}$ control



• Write cycle (2) : $\overline{CE}$ control



During I/O pins are in the output state, the data input signals of opposite phase to the output must not be applied.

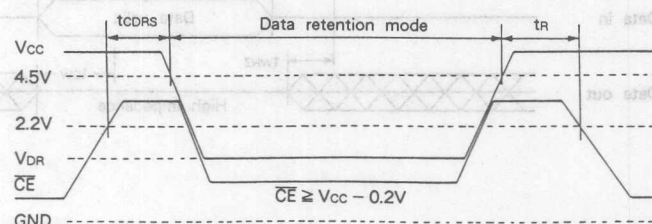
Data Retention Characteristics

($T_a = 0$ to 70°C)

Item	Symbol	Test conditions	-70L/85L/10L/12L			-70LL/85LL/10LL/12LL			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Data retention voltage	V_{DR}	$\overline{CE} \geq V_{CC} - 0.2V$	2.0	—	5.5	2.0	—	5.5	V
Data retention current	I_{CCDR1}	$V_{CC} = 3.0V$ $\overline{CE} \geq 2.8V$ $T_a = 0$ to 70°C	—	—	10	—	—	3	μA
		$T_a = 0$ to 40°C	—	—	2	—	—	0.6	
		25°C	—	0.25	1	—	0.1	0.3	
	I_{CCDR2}	$V_{CC} = 2.0$ to $5.5V$ $\overline{CE} \geq V_{CC} - 0.2V$	—	0.5	25	—	0.2	5	μA
Data retention setup time	t_{CDRS}	Chip disable to data retention mode	0	—	—	0	—	—	ns
Recovery time	t_R		t_{RC}^*	—	—	t_{RC}^*	—	—	ns

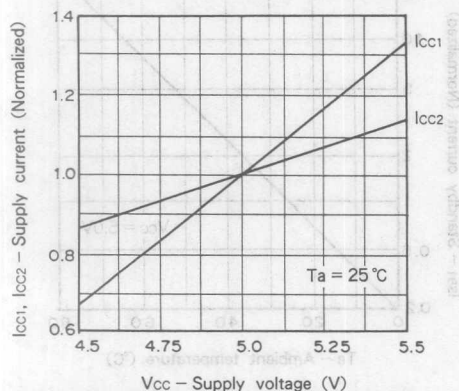
* t_{RC} : Read cycle time

Data retention waveform

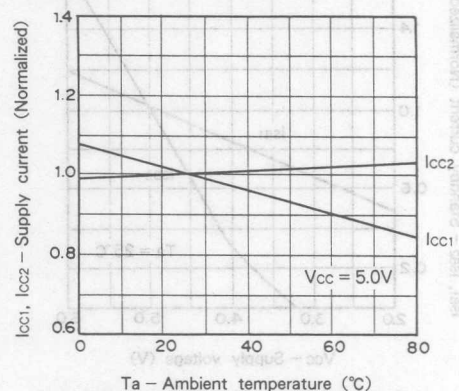


Example of Representative Characteristics

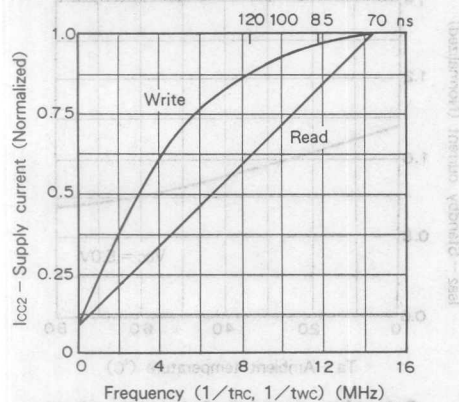
Supply current vs. Supply voltage



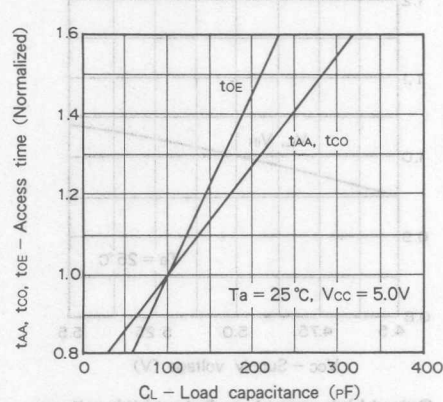
Supply current vs. Ambient temperature



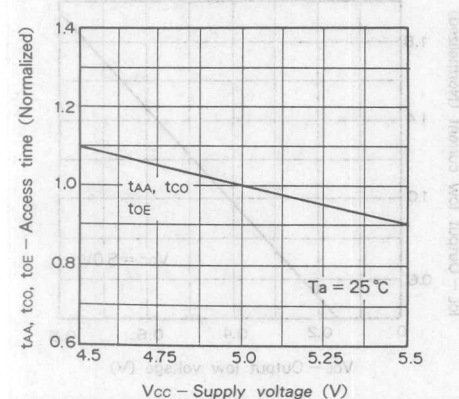
Supply current vs. Frequency



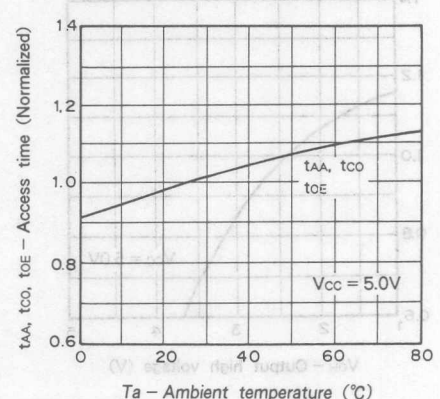
Access time vs. Load capacitance



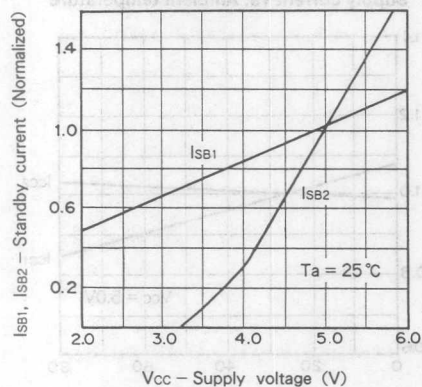
Access time vs. Supply voltage



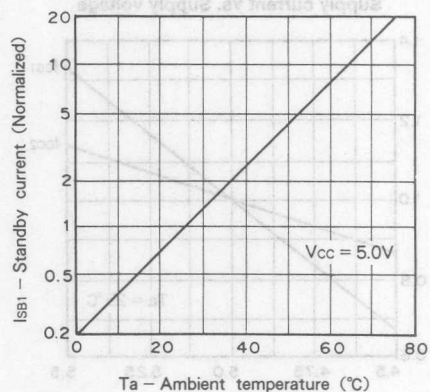
Access time vs. Ambient temperature



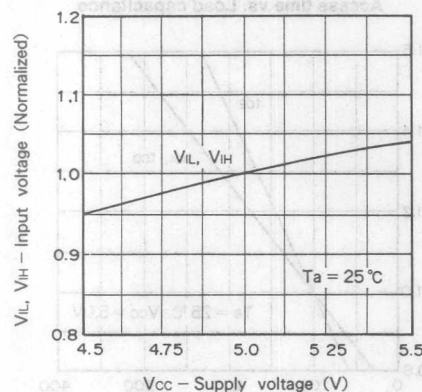
Standby current vs. Supply voltage



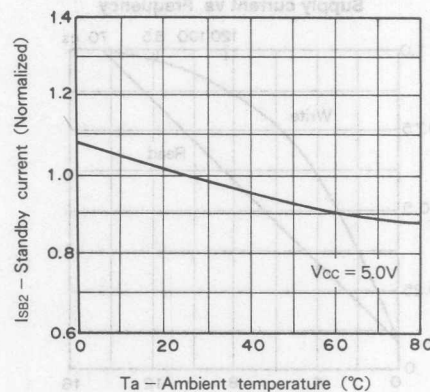
Standby current vs. Ambient temperature



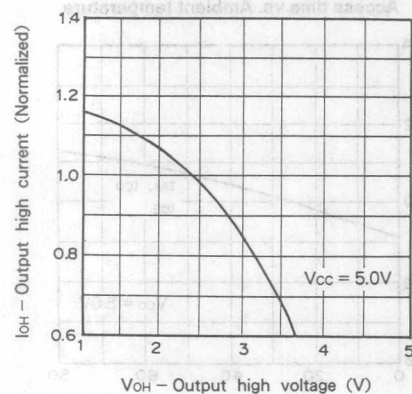
Input voltage level vs. Supply voltage



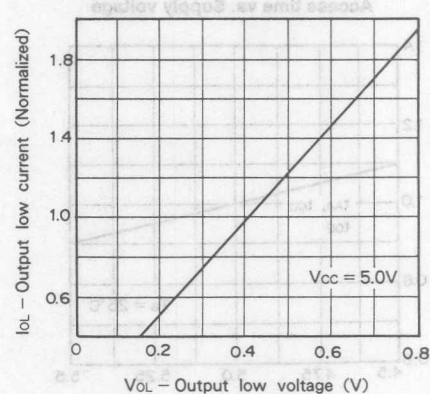
Standby current vs. Ambient temperature



Output high current vs. Output high voltage



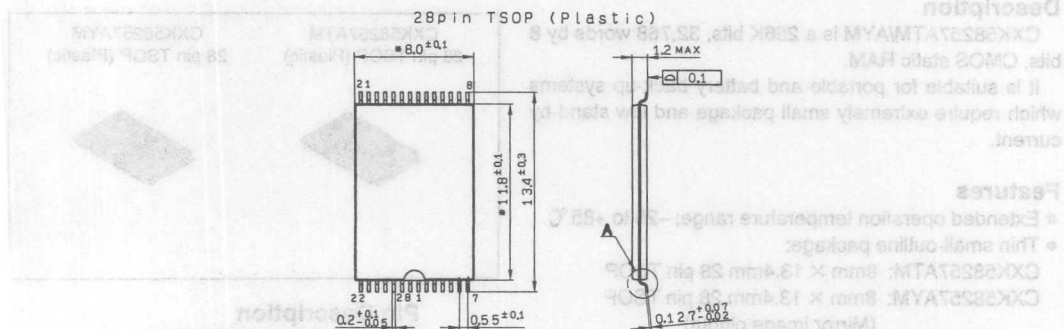
Output low current vs. Output low voltage



Package Outline Unit: mm

CXK58257ATM

28pin TSOP (Plastic)

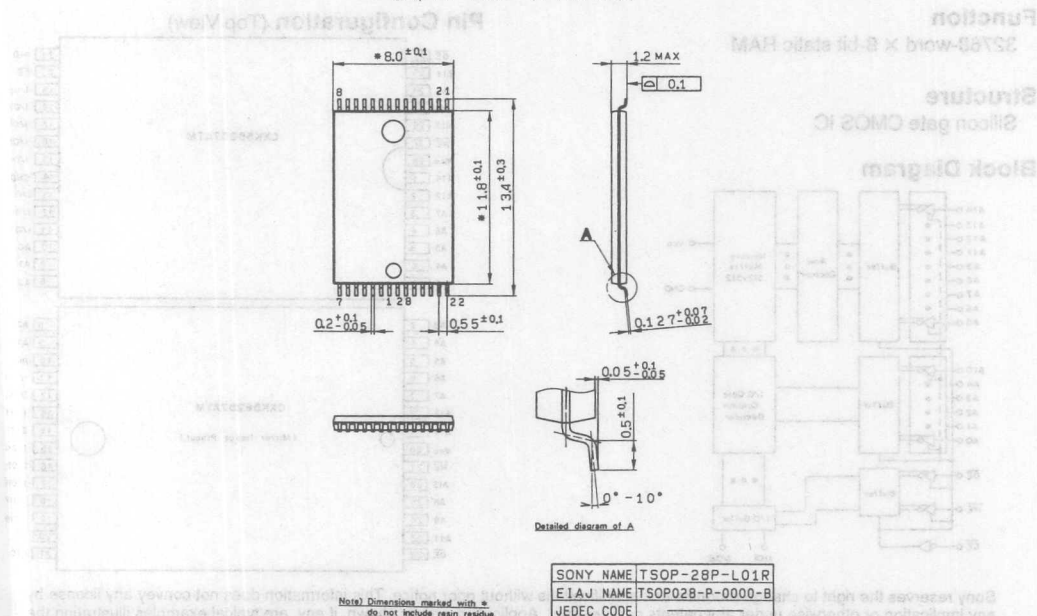


Description	Symbol
Address input	A0 to A7
Data input/output	D0 to D7
Chip enable input	CE
Write enable input	WE
Output enable input	OE
+5V power supply	VCC
GND	GND

Note: Dimensions marked with * do not include resin residue.

CXK58257AYM

28pin TSOP (Plastic)



SONY NAME	TSOP-28P-L01R
EIAJ NAME	TSOP28-P-0000-B
JEDEC CODE	

Note: Dimensions marked with * do not include resin residue.

-70LX/85LX/10LX/12LX
-70LLX/85LLX/10LLX/12LLX

32,768 words by 8

y back-up systems
e and low stand-by

- | Symbol | Description |
|-----------------|---------------------|
| A0 to A14 | Address input |
| I/O1 to I/O8 | Data input/output |
| $\overline{CE}$ | Chip enable input |
| $\overline{WE}$ | Write enable input |
| $\overline{OE}$ | Output enable input |
| Vcc | +5V power supply |
| GND | Ground |

Pin Configuration (Top View)

The image displays two pin diagrams for the CXK58257ATM and CXK58257AYM integrated circuits. The top diagram shows the CXK58257ATM with pins 1-14 on the left and 15-28 on the right. The bottom diagram shows the CXK58257AYM with pins 1-14 on the left and 15-28 on the right, with a note '(Mirror Image Pinout)' between the two diagrams.

Pin	Signal	Pin	Signal
22	OE	21	A10
23	A11	20	CE
24	A9	19	I/OB
25	A8	18	I/O7
26	A13	17	I/O6
27	WE	16	I/O5
28	Vcc	15	I/O4
1	A14	14	GND
2	A12	13	I/O3
3	A7	12	I/O2
4	A6	11	I/O1
5	A5	10	A0
6	A4	9	A1
7	A3	8	A2

CXK58257ATM

CXK58257AYM

(Mirror Image Pinout)

Pin	Signal	Pin	Signal
7	A3	8	A2
6	A4	9	A1
5	A5	10	A0
4	A6	11	I/O1
3	A7	12	I/O2
2	A12	13	I/O3
1	A14	14	GND
28	Vcc	15	I/O4
27	WE	16	I/O5
26	A13	17	I/O6
25	A8	18	I/O7
24	A9	19	I/OB
23	A11	20	CE
22	OE	21	A10

Silicon gate CMOS IC

The diagram illustrates the internal structure of a 256K16 DRAM. It features a central memory array of 512 rows by 512 columns. A Row Decoder (512x512) is connected to the array's rows, receiving address lines A14 through A5. A Column Decoder (512x512) is connected to the array's columns, receiving address lines A10 through A0. The array's output is connected to an I/O Gate Column Decoder, which then feeds into an I/O Buffer. The I/O Buffer has two outputs, I/O1 and I/O0. Control signals include OE (Output Enable), WE (Write Enable), and CE (Chip Enable), each passing through a buffer before reaching the memory array. Power supply connections for Vcc and GND are also indicated.

176

Absolute Maximum Ratings

(Ta=25°C, GND=0V)

Item	Symbol	Rating	Unit
Supply voltage	V _{CC}	-0.5 to +7.0	V
Input voltage	V _{IN}	-0.5 * to V _{CC} +0.5	V
Input and output voltage	V _{I/O}	-0.5 * to V _{CC} +0.5	V
Allowable power dissipation	P _D	0.7	W
Operating temperature	T _{opr}	-25 to +85	°C
Storage temperature	T _{stg}	-55 to +150	°C
Soldering temperature * time	T _{solder}	235 * 10	°C * sec

* V_{IN}, V_{I/O}=-3.0V Min. for pulse width less than 50ns.

Truth Table

CE	OE	WE	Mode	I/O1 to I/O8	V _{CC} Current
H	X	X	Not selected	High Z	I _{SB1} , I _{SB2}
L	H	H	Not selected	High Z	I _{CC1} , I _{CC2}
L	L	H	Read	Data out	I _{CC1} , I _{CC2}
L	X	L	Write	Data in	I _{CC1} , I _{CC2}

X : "H" or "L"

DC Recommended Operating Conditions (Ta=-25 to +85°C, GND=0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Input high voltage	V _{IH}	2.2	—	V _{CC} +0.3	V
Input low voltage	V _{IL}	-0.3 *	—	0.8	V

* V_{IL}=-3.0V Min. for pulse width less than 50ns.

Item	Symbol	Test conditions	Min.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} =0V	—	6	pF
I/O capacitance	C _{IO}	V _{IO} =0V	—	8	pF

(Note) This parameter is sampled and is not 100% tested.

Electrical Characteristics

• DC and operating characteristics

(V_{CC}=5V ± 10%, GND=0V, T_a=-25 to +85 °C)

Item	Symbol	Test conditions	-70LX/85LX/10LX/12LX			-70LLX/85LLX/10LLX/12LLX			Unit	
			Min.	Typ. *	Max.	Min.	Typ. *	Max.		
Input leakage current	I _{LI}	V _{IN} =GND to V _{CC}	-0.5	—	0.5	-0.5	—	0.5	μA	
Output leakage current	I _{LO}	$\overline{CE}=V_{IH}$ or $\overline{OE}=V_{IH}$ V _{I/O} =GND to V _{CC}	-0.5	—	0.5	-0.5	—	0.5	μA	
Operating power supply current	I _{CC1}	$\overline{CE}=V_{IL}$, V _{IN} =V _{IH} or V _{IL} , I _{OUT} =0mA	—	3	10	—	3	10	mA	
		$\overline{CE} \leq 0.2V$ V _{IN} ≤ 0.2V or ≥ V _{CC} -0.2V	—	1	5	—	1	5		
Average operating current	I _{CC2}	Cycle=Min, Duty=100% I _{OUT} =0mA	70LX/70LLX	—	30	60	—	30	60	mA
			85LX/85LLX	—	25	60	—	25	60	
			10LX/10LLX	—	23	60	—	23	60	
			12LX/12LLX	—	20	60	—	20	60	
Standby current	I _{SB1}	$\overline{CE} \geq V_{CC}-0.2V$	-25 to +85 °C	—	—	50	—	—	10	μA
			-25 to +70 °C	—	—	25	—	—	5	
			-25 to +40 °C	—	—	5	—	—	1	
			+25 °C	—	0.5	2	—	0.2	0.5	
	I _{SB2}	$\overline{CE}=V_{IH}$	—	0.4	2	—	0.4	2	mA	
Output high voltage	V _{OH}	I _{OH} =-1.0mA	2.4	—	—	2.4	—	—	V	
Output low voltage	V _{OL}	I _{OL} =2.1mA	—	—	0.4	—	—	0.4	V	

* V_{CC}=5V, T_a=25 °C

I/O Capacitance

(T_a=25 °C, f=1MHz)

Item	Symbol	Test conditions	Min.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} =0V	—	6	pF
I/O capacitance	C _{I/O}	V _{I/O} =0V	—	8	pF

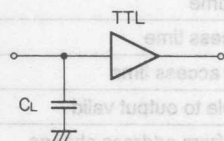
Note) This parameter is sampled and is not 100% tested.

AC Characteristics

● AC test conditions

(V_{CC}=5V ± 10%, T_a=-25 to +85°C)

Item	Conditions
Input pulse high level	V _{IH} =2.4V
Input pulse low level	V _{IL} =0.6V
Input rise time	t _r =5ns
Input fall time	t _f =5ns
Input and output reference level	1.5V
Output load conditions	85LX/85LLX/10LX/ 10LLX/12LX/12LLX
	70LX/70LLX
	C _L * =100pF, 1TTL
	C _L * =30pF, 1TTL

* C_L includes scope and jig capacitances.

Item	Symbol	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
Write cycle time	t _{WC}	70	—	85	—	100	—	120	—	150	—
Address valid to end of write	t _{AV}	65	—	75	—	80	—	100	—	—	—
Chip enable to end of write	t _{CE}	65	—	75	—	80	—	100	—	—	—
Data to write time overlap	t _{DW}	30	—	30	—	35	—	40	—	—	—
Data hold from write time	t _{DH}	0	—	0	—	0	—	0	—	—	—
Write pulse width	t _{WP}	20	—	20	—	20	—	20	—	—	—
Address setup time	t _{AS}	0	—	0	—	0	—	0	—	—	—
Write recovery time (W _R)	t _{WR}	5	—	5	—	5	—	5	—	—	—
Write recovery time (C _R)	t _{WR}	0	—	0	—	0	—	0	—	—	—
Output active from end of write	t _{OW}	10	—	10	—	10	—	10	—	—	—
Write to output in high Z	t _{WZ} *	0	25	0	25	0	25	0	25	—	—

* t_{WZ} is defined as the time required for outputs to turn to high impedance state and is not related to output voltage level.

• Read cycle

Item	Symbol	-70LX/70LLX		-85LX/85LLX		-10LX/10LLX		-12LX/12LLX		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t _{RC}	70	—	85	—	100	—	120	—	ns
Address access time	t _{AA}	—	70	—	85	—	100	—	120	ns
Chip enable access time	t _{CO}	—	70	—	85	—	100	—	120	ns
Output enable to output valid	t _{OE}	—	35	—	45	—	50	—	60	ns
Output hold from address change	t _{OH}	5	—	10	—	10	—	10	—	ns
Chip enable to output in low Z ($\overline{CE}$)	t _{LZ}	10	—	10	—	10	—	10	—	ns
Output enable to output in low Z ($\overline{OE}$)	t _{OLZ}	5	—	5	—	5	—	5	—	ns
Chip disable to output in high Z ($\overline{CE}$)	t _{HZ} *	0	30	0	30	0	30	0	30	ns
Chip disable to output in high Z ($\overline{OE}$)	t _{OHZ} *	0	30	0	30	0	30	0	30	ns

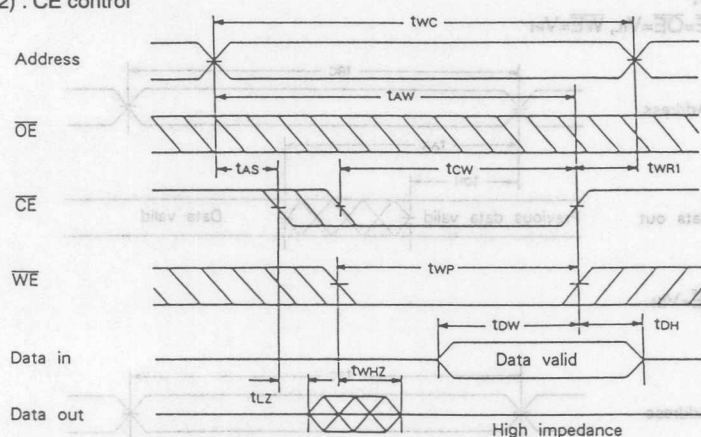
* t_{HZ} and t_{OHZ} are defined as the time required for outputs to turn to high impedance state and are not referred to as output voltage levels.

• Write cycle

Item	Symbol	-70LX/70LLX		-85LX/85LLX		-10LX/10LLX		-12LX/12LLX		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t _{WC}	70	—	85	—	100	—	120	—	ns
Address valid to end of write	t _{AW}	65	—	75	—	80	—	100	—	ns
Chip enable to end of write	t _{CW}	65	—	75	—	80	—	100	—	ns
Data to write time overlap	t _{DW}	30	—	30	—	35	—	40	—	ns
Data hold from write time	t _{DH}	0	—	0	—	0	—	0	—	ns
Write pulse width	t _{WP}	50	—	50	—	60	—	70	—	ns
Address setup time	t _{AS}	0	—	0	—	0	—	0	—	ns
Write recovery time ($\overline{WE}$)	t _{WR}	5	—	5	—	5	—	5	—	ns
Write recovery time ($\overline{CE}$)	t _{WR1}	0	—	0	—	0	—	0	—	ns
Output active from end of write	t _{OW}	10	—	10	—	10	—	10	—	ns
Write to output in high Z	t _{WHZ} *	0	25	0	25	0	25	0	25	ns

* t_{WHZ} is defined as the time required for outputs to turn to high impedance state and is not referred to as output voltage level.

• Write cycle (2) : $\overline{\text{CE}}$ control



During I/O pins are in the output state, the data input signals of opposite phase to the output must not be applied.

Data Retention Characteristics

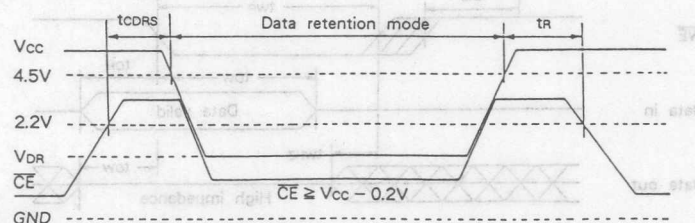
($T_a = -25$ to $+85^\circ\text{C}$)

Item	Symbol	Test conditions	-70LX/85LX/10LX/12LX			-70LLX/85LLX/10LLX/12LLX			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Data retention voltage	V_{DR}	$\overline{\text{CE}} \geq V_{CC} - 0.2\text{V}$	2.0	—	5.5	2.0	—	5.5	V
Data retention current	I_{CCDR1}	$V_{CC} = 3.0\text{V}$ $\overline{\text{CE}} \geq 2.8\text{V}$ -25 to $+85^\circ\text{C}$	—	—	20	—	—	6	μA
		-25 to $+70^\circ\text{C}$	—	—	10	—	—	3	
		-25 to $+40^\circ\text{C}$	—	—	2	—	—	0.6	
		$+25^\circ\text{C}$	—	0.25	1	—	0.1	0.3	
	I_{CCDR2}	$V_{CC} = 2.0$ to 5.5V $\overline{\text{CE}} \geq V_{CC} - 0.2\text{V}$	—	0.5**	50	—	0.2**	10	μA
Data retention setup time	t_{CDRS}	Chip disable to data retention mode	0	—	—	0	—	—	ns
Recovery time	t_R		t_{RC}^*	—	—	t_{RC}^*	—	—	ns

* t_{RC} : Read cycle time

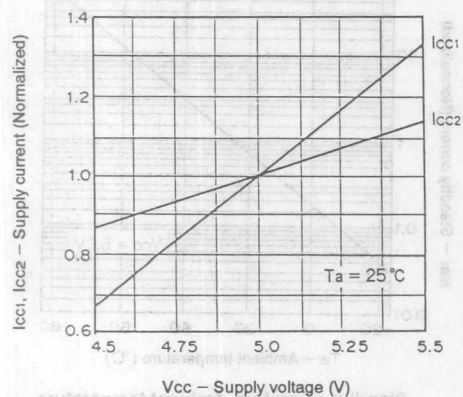
** $V_{CC} = 5\text{V}$, $T_a = 25^\circ\text{C}$

Data Retention Waveform

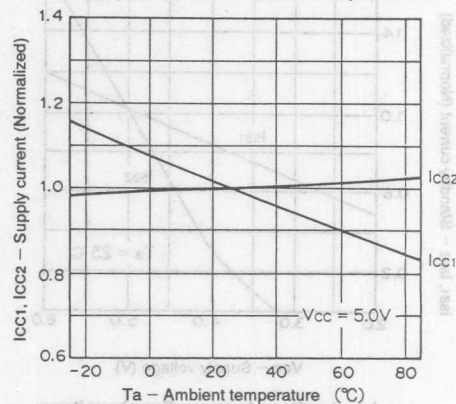


Example of Representative Characteristics

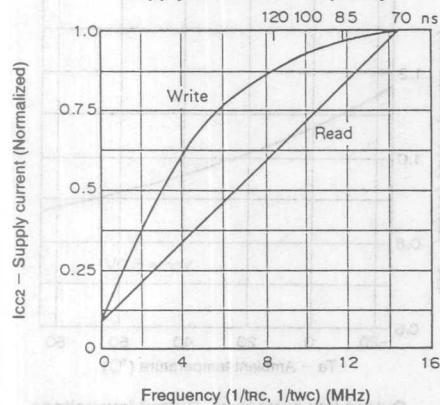
Supply current vs. Supply voltage



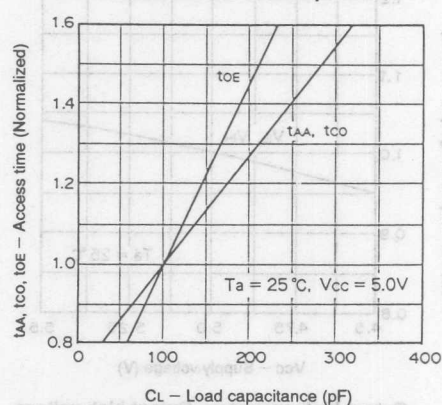
Supply current vs. Ambient temperature



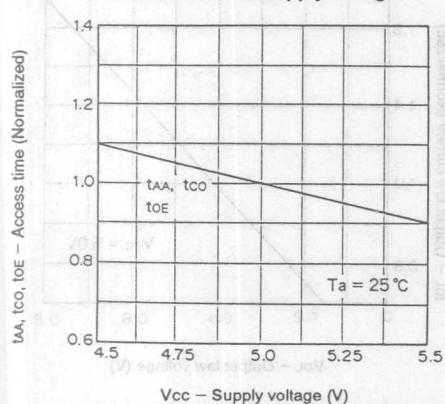
Supply current vs. Frequency



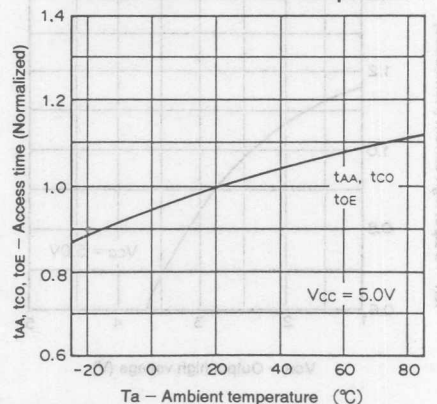
Access time vs. Load capacitance



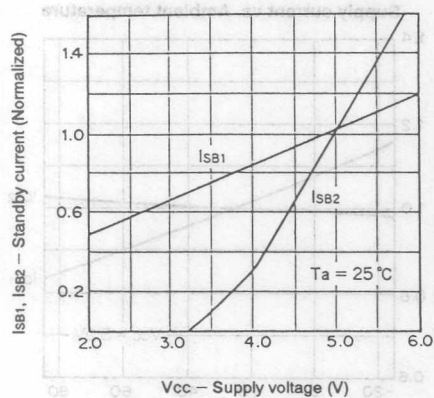
Access time vs. Supply voltage



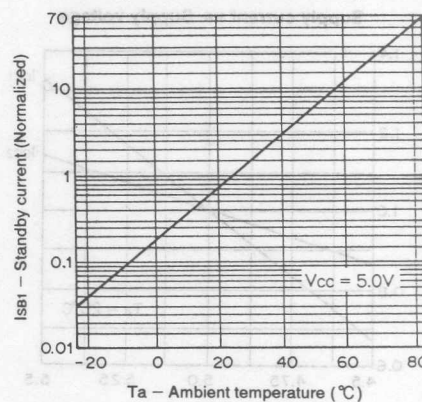
Access time vs. Ambient temperature



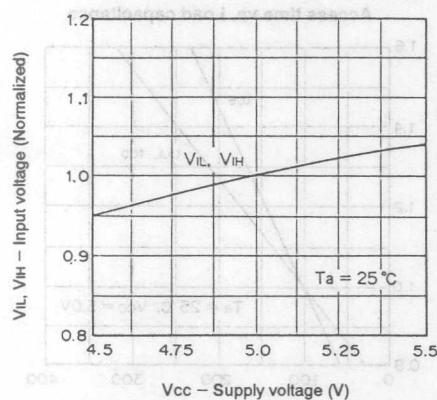
Standby current vs. Supply voltage



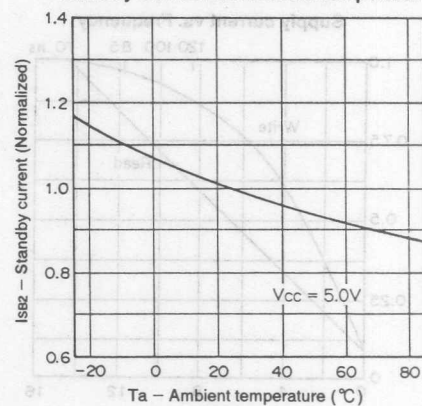
Standby current vs. Ambient temperature



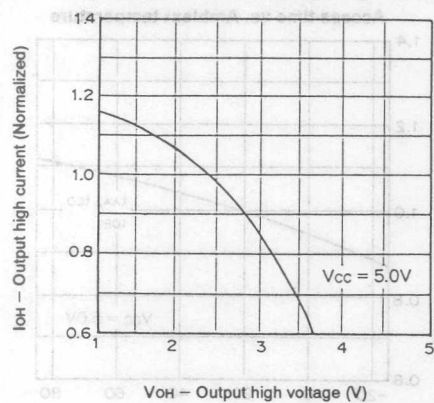
Input voltage level vs. Supply voltage



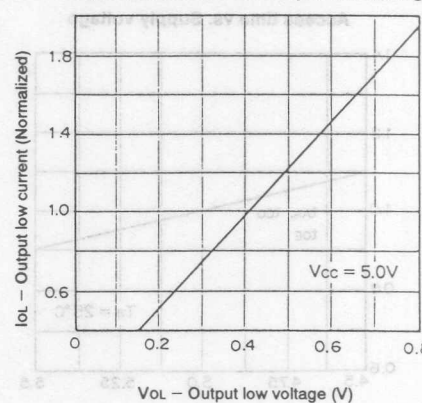
Standby current vs. Ambient temperature



Output high current vs. Output high voltage



Output low current vs. Output low voltage

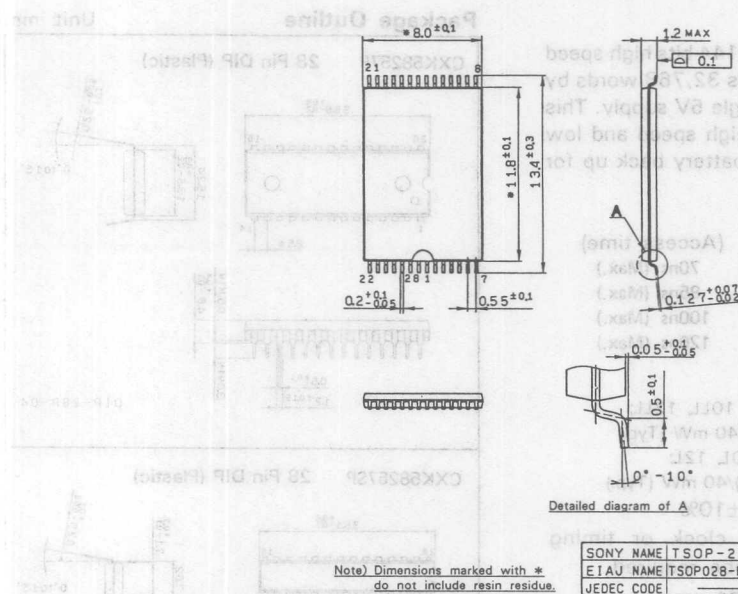


Package Outline

Unit: mm

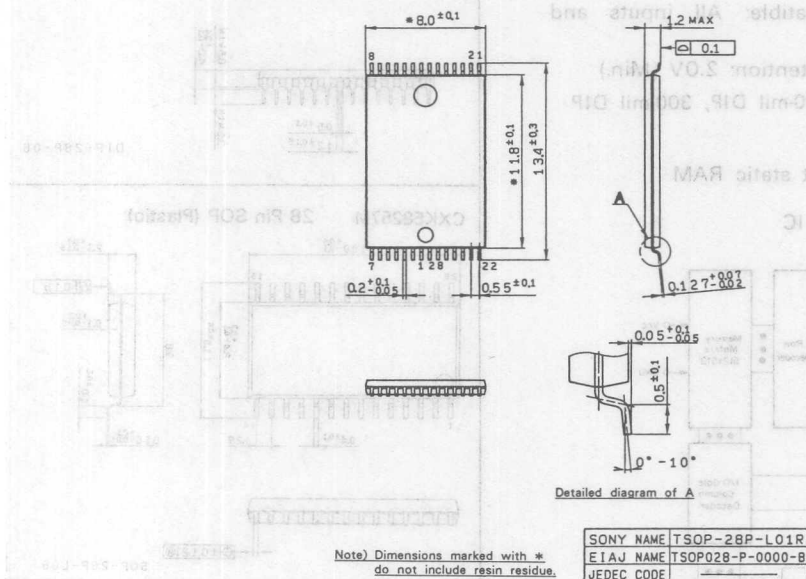
CXK58257ATM

28pin TSOP (Plastic)



CXK58257AYM

28pin TSOP (Plastic)



32768-word $\times$ 8 bit High Speed CMOS Static RAM

Description

CXK5825/P/SP/M is a 262,144 bits high speed CMOS static RAM organized as 32,768 words by 8 bits and operates from a single 5V supply. This device is suitable for use in high speed and low power applications in which battery back up for nonvolatility is required.

Features

- Fast access time: (Access time)
CXK58257P/SP/M-70L, 70LL 70ns (Max.)
CXK58257P/SP/M-85L, 85LL 85ns (Max.)
CXK58257P/SP/M-10L, 10LL 100ns (Max.)
CXK58257P/SP/M-12L, 12LL 120ns (Max.)
- Low power operation:
CXK58257P/SP/M-70LL, 85LL, 10LL, 12LL;
Standby/Operation: 5 μ W (Typ.)/40 mW (Typ.)
CXK58257P/SP/M-70L, 85L, 10L, 12L;
Standby/Operation: 10 μ W (Typ.)/40 mW (Typ.)
- Single +5V supply: +5V $\pm$ 10%
- Fully static memory ... No clock or timing
strobe required
- Equal access and cycle time
- Common data input and output: three state
output
- Directly TTL compatible: All inputs and
outputs
- Low voltage data retention: 2.0V (Min.)
- Available in 28pin 600-mil DIP, 300-mil DIP
and 450-mil SOP

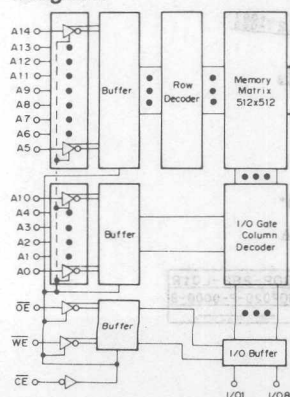
Function

32768-word $\times$ 8 bit static RAM

Structure

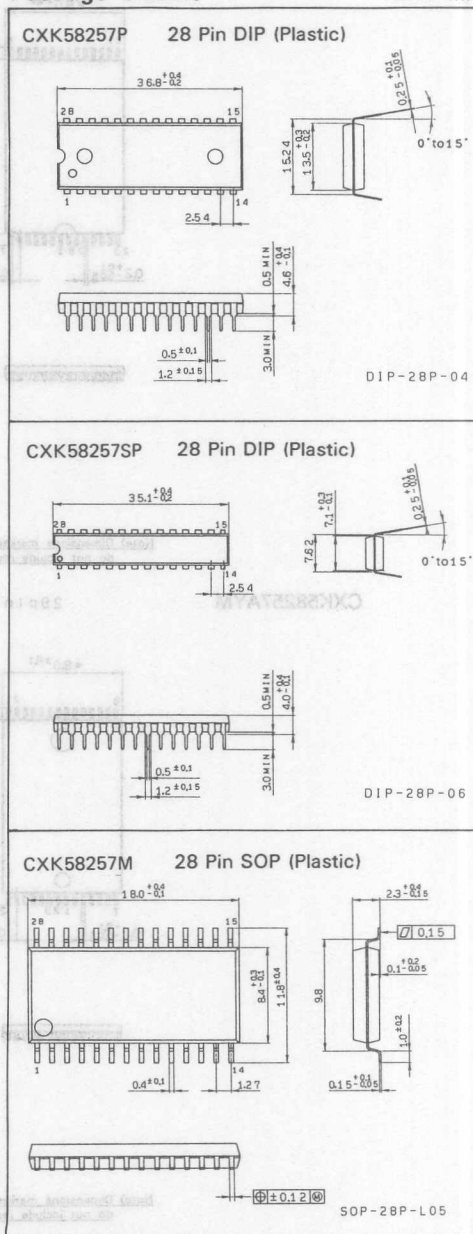
Silicon gate CMOS IC

Block Diagram

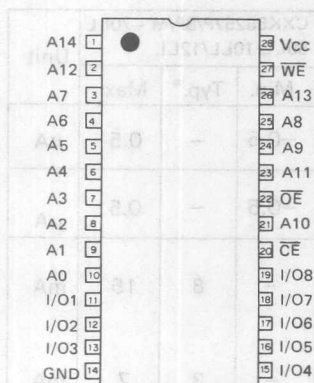


Package Outline

Unit: mm



Pin Configuration (Top View)



Pin Description

Symbol	Description
A0 to A14	Address input
I/O1 to I/O8	Data input output
$\overline{\text{CE}}$	Chip enable input
$\overline{\text{WE}}$	Write enable input
$\overline{\text{OE}}$	Output enable input
Vcc	Power supply
GND	Ground

Absolute Maximum Ratings

(Ta=25°C, GND=0V)

Item	Symbol	Rating	Unit
Supply voltage	Vcc	-0.5 to +7.0	V
Input voltage	V _{IN}	-0.5* to Vcc+0.5	V
Input and output voltage	V _{I/O}	-0.5* to Vcc+0.5	V
Allowable power dissipation P _D	CXK58257P/SP	1.0	W
	CXK58257M	0.7	
Operating temperature	T _{opr}	0 to +70	°C
Storage temperature	T _{stg}	-55 to +150	°C
Soldering temperature	T _{solder}	260 ± 10	°C · sec

*Note) V_{IN}, V_{I/O} = -3.0V Min. for pulse width less than 50 ns.

Truth Table

CE	OE	WE	Mode	I/O1 to I/O8	Vcc Current
H	X	X	Not Selected	High Z	I _{SB1} , I _{SB2}
L	H	H	Output Disable	High Z	I _{CC1} , I _{CC2}
L	L	H	Read	Data out	I _{CC1} , I _{CC2}
L	X	L	Write	Data in	I _{CC1} , I _{CC2}

Note) X: "H" or "L"

DC Recommended Operating Conditions (Ta=0 to +70°C, GND=0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Vcc	4.5	5.0	5.5	V
Input high voltage	V _{IH}	2.2	—	Vcc+0.3	V
Input low voltage	V _{IL}	-0.3*	—	0.8	V

*Note) V_{IL} = -3.0V Min. for pulse width less than 50 ns.

Electrical Characteristics

DC and operating characteristics

(V_{CC}=5V±10%, GND=0V, T_a=0 to +70°C)

Item	Symbol	Test condition	CXK58257P/SP/M -70L/85L/10L/12L			CXK58257P/SP/M -70LL 85LL/10LL/12LL			Unit	
			Min.	Typ.*	Max.	Min.	Typ.*	Max.		
Input leakage current	I _{LI}	V _{IN} =GND to V _{CC}	-0.5	-	0.5	-0.5	-	0.5	μA	
Output leakage current	I _{LO}	$\overline{CE}=V_{IH}$ or $\overline{OE}=V_{IH}$ V _{I/O} =GND to V _{CC}	-0.5	-	0.5	-0.5	-	0.5	μA	
Operating power supply current	I _{CC1}	$\overline{CE}=V_{IL}$, V _{IN} =V _{IH} or V _{IL} , I _{OUT} =0mA	-	8	15	-	8	15	mA	
		$\overline{CE} \leq 0.2V$ V _{IN} ≤ 0.2V or ≥ V _{CC} -0.2V	-	3	7	-	3	7	mA	
Average operating current	I _{CC2}	Min. cycle Duty=100% I _{OUT} =0mA	70L/70LL	-	45	70	-	45	70	mA
			85L/85LL	-	40	70	-	40	70	mA
			10L/10LL	-	35	70	-	35	70	mA
			12L/12LL	-	30	70	-	30	70	mA
Standby current	I _{SB1}	$\overline{CE} \geq V_{CC}-0.2V$	-	0.002	0.1	-	0.001	0.05	mA	
	I _{SB2}	$\overline{CE}=V_{IH}$	-	0.2	2	-	0.2	2	mA	
Output high voltage	V _{OH}	I _{OH} =-1.0mA	2.4	-	-	2.4	-	-	V	
Output low voltage	V _{OL}	I _{OL} =2.1mA	-	-	0.4	-	-	0.4	V	

*Note) V_{CC}=5V, T_a=25°C

Capacitance

(T_a=25°C, f=1 MHz)

Item	Symbol	Test Condition	Min.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} =0V	—	6	pF
Input/output capacitance	C _{I/O}	V _{I/O} =0V	—	8	pF

Note) This parameter is sampled and is not 100% tested.

AC Characteristics

• AC test conditions (V_{CC}=5V±10%, T_a=0 to +70°C)

Item		Condition
Input pulse high level		$V_{IH}=2.2V$
Input pulse low level		$V_{IL}=0.8V$
Input rise time		$t_r=5ns$
Input fall time		$t_f=5ns$
Input and output reference level		1.5V
Output load	85L/85LL/10L/10LL 12L/12LL	$C_L^* = 100pF, 1TTL$
	70L/70LL	$C_L^* = 30pF, 1TTL$

* C_L includes scope and jig capacitances.

• Read cycle

Item	Symbol	CXK58257 P/SP/M -70L/70LL		CXK58257 P/SP/M -85L/85LL		CXK58257 P/SP/M -10L/10LL		CXK58257 P/SP/M -12L/12LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	trc	70	—	85	—	100	—	120	—	ns
Address access time	tAA	—	70	—	85	—	100	—	120	ns
Chip enable access time	tco	—	70	—	85	—	100	—	120	ns
Output enable to output valid	toE	—	35	—	45	—	50	—	60	ns
Output hold from address change	toH	5	—	5	—	10	—	10	—	ns
Chip enable to output in low Z ($\overline{\text{CE}}$)	tlZ	10	—	10	—	10	—	10	—	ns
Output enable to output in low Z ($\overline{\text{OE}}$)	tolZ	5	—	5	—	5	—	5	—	ns
Chip disable to output in high Z ($\overline{\text{CE}}$)	thZ*	0	30	0	30	0	35	0	40	ns
Output disable to output in high Z ($\overline{\text{OE}}$)	toHZ*	0	30	0	30	0	35	0	40	ns

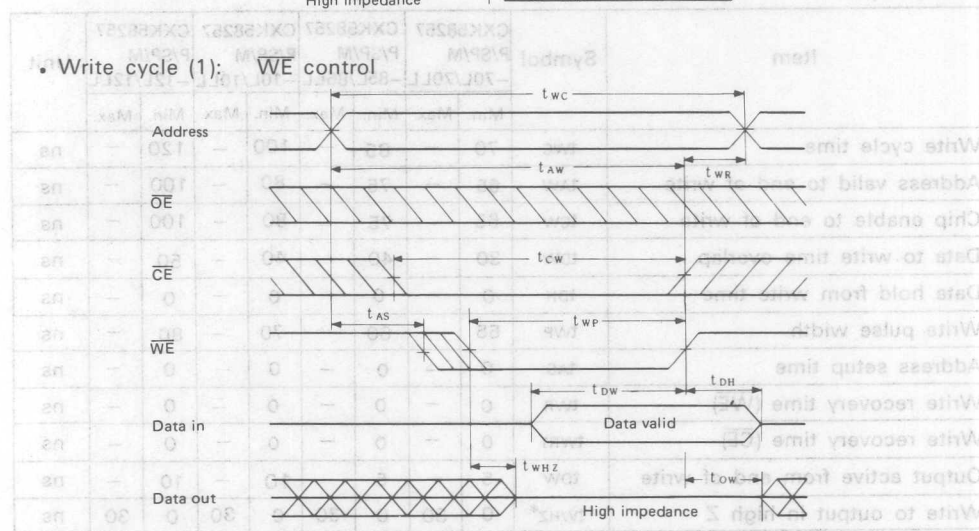
***Note)** thZ and toHZ are defined as the time at which the outputs become the high impedance state and are not referred to output voltage levels.

• Write cycle

Item	Symbol	CXK58257 P/SP/M -70L/70LL		CXK58257 P/SP/M -85L/85LL		CXK58257 P/SP/M -10L/10LL		CXK58257 P/SP/M -12L/12LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	tWC	70	—	85	—	100	—	120	—	ns
Address valid to end of write	tAW	65	—	75	—	80	—	100	—	ns
Chip enable to end of write	tcw	65	—	75	—	80	—	100	—	ns
Data to write time overlap	tdW	30	—	40	—	40	—	50	—	ns
Data hold from write time	tdH	0	—	0	—	0	—	0	—	ns
Write pulse width	tWP	55	—	60	—	70	—	80	—	ns
Address setup time	tAS	0	—	0	—	0	—	0	—	ns
Write recovery time ($\overline{\text{WE}}$)	tWR	0	—	0	—	0	—	0	—	ns
Write recovery time ($\overline{\text{CE}}$)	tWR1	0	—	0	—	0	—	0	—	ns
Output active from end of write	tOW	5	—	5	—	10	—	10	—	ns
Write to output in high Z	tWHZ*	0	30	0	30	0	30	0	30	ns

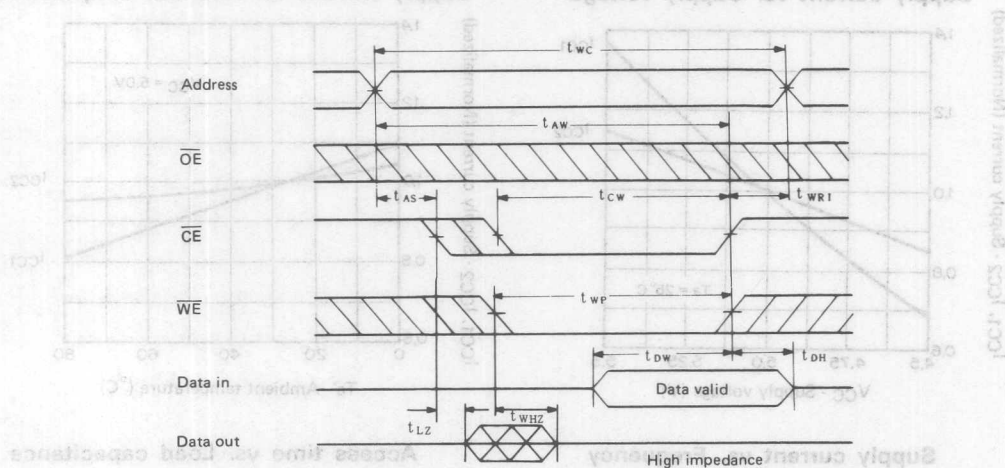
***Note)** tWHZ is defined as the time at which the outputs become the high impedance state and are not referred to output voltage levels.

- Read cycle (2): $\overline{WE} = V_{IH}$



190

- Write cycle (2): $\overline{\text{CE}}$ control



During I/O pins are in the output state, the data input signals of opposite phase to the output must not be applied.

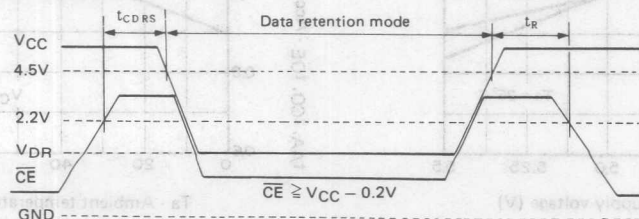
Data Retention Characteristics

($T_a = 0$ to 70°C)

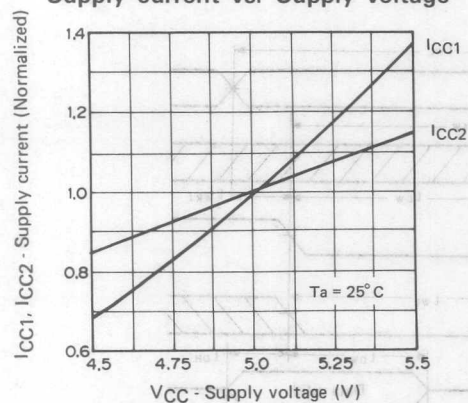
Item	Symbol	Test condition	CXK58257P/SP/M -70L/85L/10L/12L			CXK58257P/SP/M -70LL 85LL/10LL/12LL			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Data retention voltage	V_{DR}	$\overline{\text{CE}} \geq V_{\text{CC}} - 0.2\text{V}$	2.0	—	5.5	2.0	—	5.5	V
Data retention current	I_{CCDR1}	$V_{\text{CC}} = 3.0\text{V}$ $\overline{\text{CE}} \geq 2.8\text{V}$ $T_a = 0^\circ\text{C to } 70^\circ\text{C}$	—	1	50	—	0.4	10	μA
		$T_a = 0^\circ\text{C to } 50^\circ\text{C}$	—	—	—	—	0.4	5	
	I_{CCDR2}	$V_{\text{CC}} = 2.0 \text{ to } 5.5\text{V}$ $\overline{\text{CE}} \geq V_{\text{CC}} - 0.2\text{V}$ 25°C	—	—	—	—	0.4	1	μA
Data retention setup time	t_{CDRS}	Chip disable to data retention mode	0	—	—	0	—	—	ns
Recovery time	t_{R}		t_{RC}^*	—	—	t_{RC}^*	—	—	ns

* t_{RC} : Read cycle time

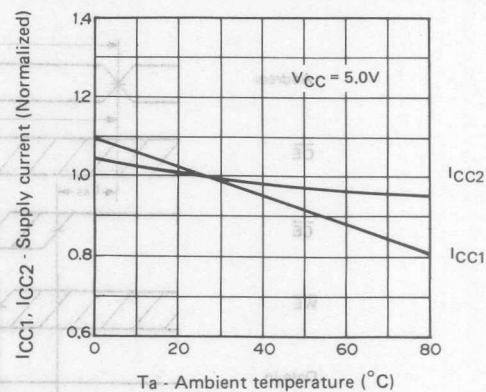
- Data retention waveform



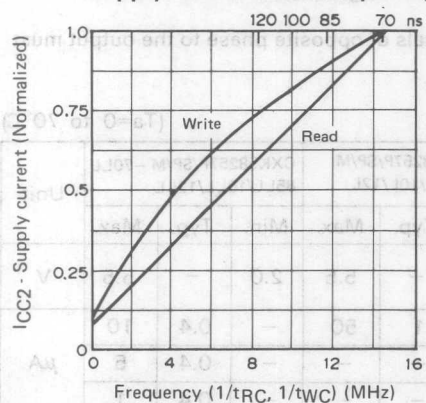
Supply current vs. Supply voltage



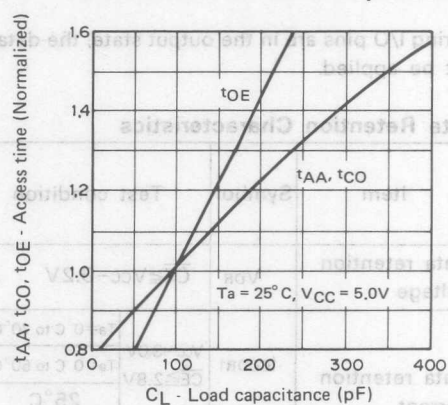
Supply current vs. Ambient temperature



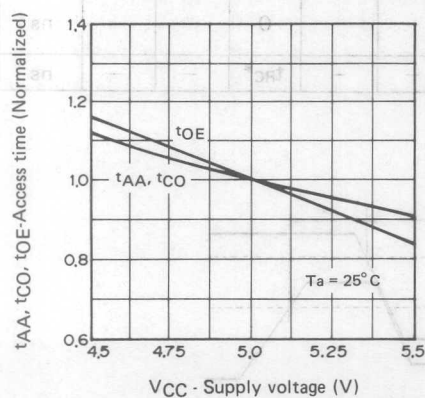
Supply current vs. Frequency



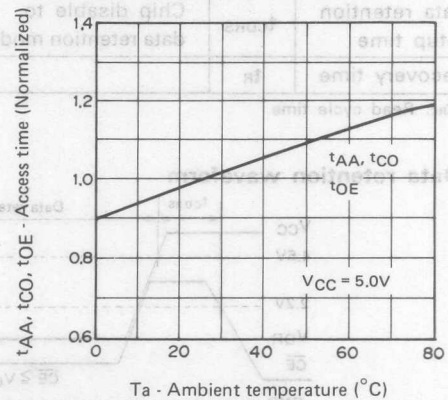
Access time vs. Load capacitance



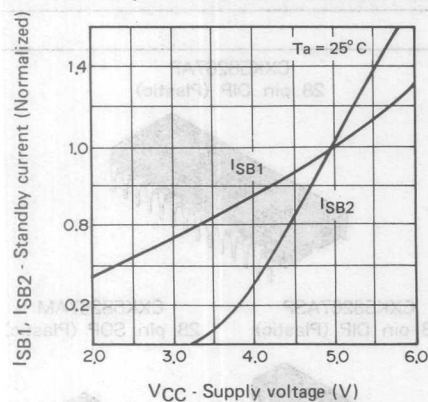
Access time vs. Supply voltage



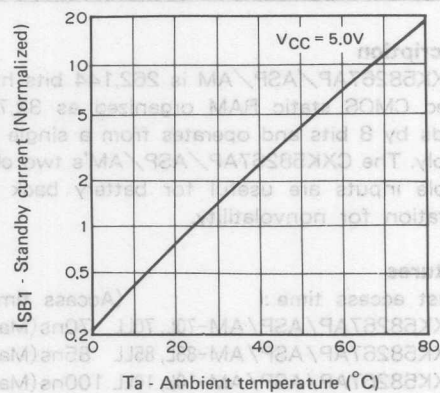
Access time vs. Ambient temperature



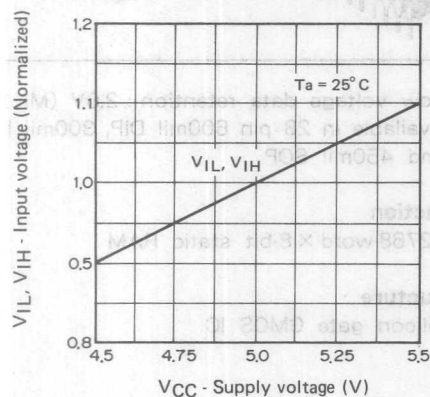
Standby current vs. Supply voltage



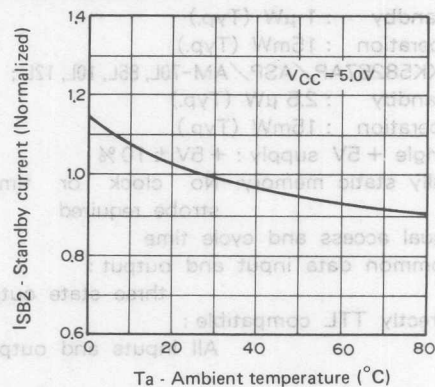
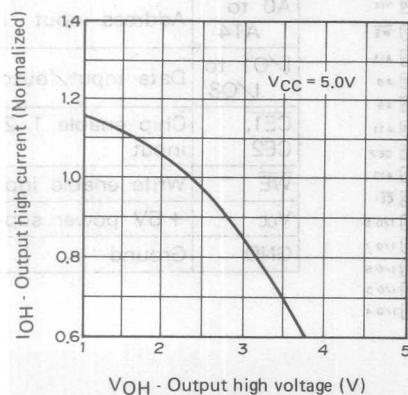
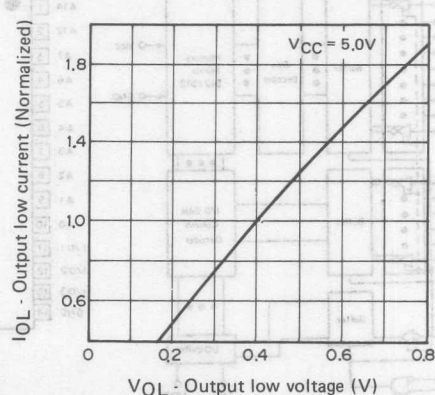
Standby current vs. Ambient temperature



Input voltage vs. Supply voltage



Standby current vs. Ambient temperature

Output high current vs.
Output high voltageOutput low current vs.
Output low voltage

SONY CXK58267AP/ASP/AM

-70L/85L/10L/12L/10LL
-70LL/85LL/10LL/12LL

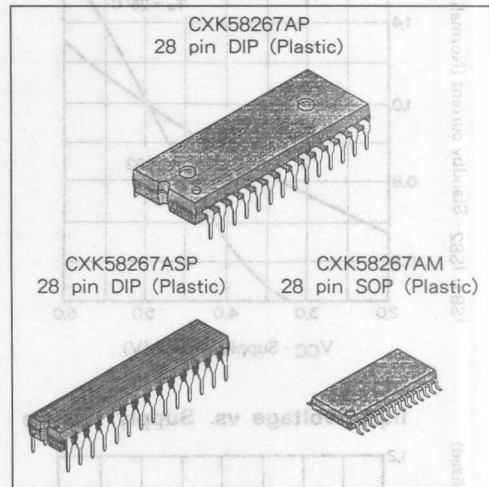
32768-word × 8-bit High Speed CMOS Static RAM

Description

CXK58267AP/ASP/AM is 262,144 bits high speed CMOS static RAM organized as 32,768 words by 8 bits and operates from a single 5V supply. The CXK58267AP/ASP/AM's two chip enable inputs are useful for battery back up operation for nonvolatility.

Features

- Fast access time : (Access time)
CXK58267AP/ASP/AM-70L, 70LL 70ns(Max.)
CXK58267AP/ASP/AM-85L, 85LL 85ns(Max.)
CXK58267AP/ASP/AM-10L, 10LL 100ns(Max.)
CXK58267AP/ASP/AM-12L, 12LL 120ns(Max.)
- Low power operation :
CXK58267AP/ASP/AM-70LL, 85LL, 10LL, 12LL ;
Standby : 1 μ W (Typ.)
Operation : 15mW (Typ.)
CXK58267AP/ASP/AM-70L, 85L, 10L, 12L ;
Standby : 2.5 μ W (Typ.)
Operation : 15mW (Typ.)
- Single +5V supply : +5V $\pm$ 10 %
- Fully static memory...No clock or timing strobe required
- Equal access and cycle time
- Common data input and output : three state output
- Directly TTL compatible : All inputs and outputs



- Low voltage data retention : 2.0V (Min.)
- Available in 28 pin 600mil DIP, 300mil DIP and 450mil SOP

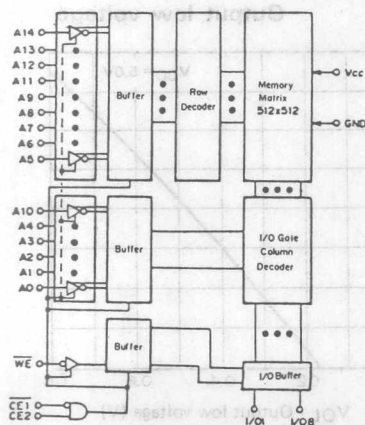
Function

32768-word × 8-bit static RAM

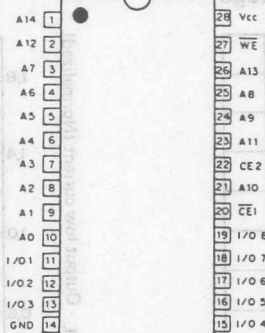
Structure

Silicon gate CMOS IC

Block Diagram



Pin Configuration (Top View)



Pin Description

Symbol	Description
A0 to A14	Address input
I/O1 to I/O8	Data input/output
CE1, CE2	Chip enable 1, 2 input
WE	Write enable input
Vcc	+ 5V power supply
GND	Ground

Absolute Maximum Ratings

(Ta = 25°C, GND = 0V)

Item	Symbol	Rating	Unit
Supply voltage	V _{CC}	- 0.5 to + 7.0	V
Input voltage	V _{IN}	- 0.5* to V _{CC} + 0.5	V
Input and output voltage	V _{I/O}	- 0.5* to V _{CC} + 0.5	V
Allowable power dissipation	P _D	CXK58267AP/ASP	1.0
		CXK58267AM	0.7
Operating temperature	T _{opr}	0 to + 70	°C
Storage temperature	T _{stg}	- 55 to + 150	°C
Soldering temperature • time	T _{solder}	260 • 10	°C • sec

* V_{IN}, V_{I/O} = - 3.0V Min. for pulse width less than 50ns.

Truth Table

CE1	CE2	WE	Mode	I/O1 to I/O8	V _{CC} Current
H	X	X	Not selected	High Z	I _{SB1} , I _{SB2}
X	L	X	Not selected	High Z	I _{SB1} , I _{SB2}
L	H	H	Read	Data out	I _{CC1} , I _{CC2}
L	H	L	Write	Data in	I _{CC1} , I _{CC2}

X : "H" or "L"

DC Recommended Operating Conditions (Ta = 0 to + 70°C, GND = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Input high voltage	V _{IH}	2.2	—	V _{CC} + 0.3	V
Input low voltage	V _{IL}	- 0.3*	—	0.8	V

* V_{IL} = - 3.0V Min. for pulse width less than 50ns.

Electrical Characteristics

• DC and operating characteristics

(V_{CC} = 5V ± 10%, GND = 0V, T_a = 0 to +70°C)

Item	Symbol	Test conditions	-70L/85L/10L/12L			-70LL/85LL/10LL/12LL			Unit	
			Min.	Typ.*	Max.	Min.	Typ.*	Max.		
Input leakage current	I _{LI}	V _{IN} = GND to V _{CC}	-0.5	—	0.5	-0.5	—	0.5	μA	
Output leakage current	I _{LO}	CE1 = V _{IH} or CE2 = V _{IL} or WE = V _{IL} , V _{I/O} = GND to V _{CC}	-0.5	—	0.5	-0.5	—	0.5	μA	
Operating power supply current	I _{CC1}	CE1 = V _{IL} , CE2 = V _{IH} , I _{OUT} = 0mA	—	3	10	—	3	10	mA	
		CE1 = 0.2V, CE2 = V _{CC} - 0.2V V _{IN} = 0.2V or V _{CC} - 0.2V	—	1	5	—	1	5		
Average operating current	I _{CC2}	Min. cycle Duty = 100 %, I _{OUT} = 0mA	70L/70LL	—	30	50	—	30	50	mA
			85L/85LL	—	25	50	—	25	50	
			10L/10LL	—	23	50	—	23	50	
			12L/12LL	—	20	50	—	20	50	
Standby current	I _{SB1}	CE2 ≤ 0.2V or (CE1 ≥ V _{CC} - 0.2V CE2 ≥ V _{CC} - 0.2V)	0 to 70°C	—	—	25	—	—	5	μA
			0 to 40°C	—	—	5	—	—	1	
			25°C	—	0.5	2	—	0.2	0.5	
			I _{SB2}	CE2 = V _{IL} , or CE1 = V _{IH}	—	0.6	3	—	0.6	
	Output high voltage	V _{OH}	I _{OH} = -1.0mA	2.4	—	—	2.4	—	—	V
Output low voltage	V _{OL}	I _{OL} = 2.1mA	—	—	0.4	—	—	0.4	V	

* V_{CC} = 5V, T_a = 25°C

I/O capacitance

(T_a = 25°C, f = 1MHz)

Item	Symbol	Test conditions	Min.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} = 0V	—	6	pF
I/O capacitance	C _{I/O}	V _{I/O} = 0V	—	8	pF

Note) This parameter is sampled and is not 100% tested.

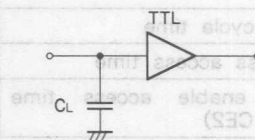
AC characteristics

● AC test conditions ($V_{CC} = 5V \pm 10\%$, $T_a = 0$ to $+70^\circ\text{C}$)

Item	Conditions
Input pulse high level	$V_{IH} = 2.2V$
Input pulse low level	$V_{IL} = 0.8V$
Input rise time	$t_r = 5ns$
Input fall time	$t_f = 5ns$
Input and output reference level	1.5V
Output load conditions	85L / 85LL / 10L / 10LL / 12L / 12LL
	70L / 70LL
	$C_L^* = 100pF, 1TTL$
	$C_L^* = 30pF, 1TTL$

* C_L includes scope and jig capacitances.

* Read cycle



* Write cycle

Item	Symbol	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
Write cycle time	t_{wc}	70	—	85	—	100	—	120	—	150	—
Address valid to end of write	t_{aw}	65	—	75	—	90	—	100	—	120	—
Chip enable to end of write	t_{cew}	65	—	75	—	90	—	100	—	120	—
Data to write time overlap	t_{dwo}	30	—	30	—	35	—	40	—	45	—
Data hold from write time	t_{dhw}	0	—	0	—	0	—	0	—	0	—
Write pulse width	t_{wp}	50	—	50	—	60	—	70	—	80	—
Address setup time	t_{as}	0	—	0	—	0	—	0	—	0	—
Write recovery time (WB)	t_{wr}	0	—	0	—	0	—	0	—	0	—
Write recovery time (CE, CEs)	t_{wr}	0	—	0	—	0	—	0	—	0	—
Output active from end of write	t_{ow}	10	—	10	—	10	—	10	—	10	—
Write to output in high Σ	t_{wh}^*	0	25	0	25	0	25	0	25	0	25

* t_{wh} is defined as the time required for outputs to turn to high impedance state and is not related to as output voltage level.

• Read cycle

Item	Symbol	-70L/70LL		-85L/85LL		-10L/10LL		-12L/12LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t _{RC}	70	—	85	—	100	—	120	—	ns
Address access time	t _{AA}	—	70	—	85	—	100	—	120	ns
Chip enable access time (CE1, CE2)	t _{CO1} , t _{CO2}	—	70	—	85	—	100	—	120	ns
Output hold from address change	t _{OH}	20	—	20	—	20	—	20	—	ns
Chip enable to output in low Z (CE1, CE2)	t _{LZ1} , t _{LZ2}	10	—	10	—	10	—	10	—	ns
Chip disable to output in high Z (CE1, CE2)	t _{HZ1} *, t _{HZ2} *	0	30	0	30	0	30	0	30	ns

* t_{HZ1} and t_{HZ2} are defined as the time required for outputs to turn to high impedance state and are not referred to as output voltage levels.

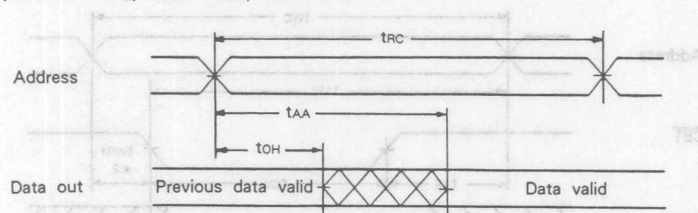
• Write cycle

Item	Symbol	-70L/70LL		-85L/85LL		-10L/10LL		-12L/12LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t _{WC}	70	—	85	—	100	—	120	—	ns
Address valid to end of write	t _{AW}	65	—	75	—	80	—	100	—	ns
Chip enable to end of write	t _{CW}	65	—	75	—	80	—	100	—	ns
Data to write time overlap	t _{DW}	30	—	30	—	35	—	40	—	ns
Data hold from write time	t _{DH}	0	—	0	—	0	—	0	—	ns
Write pulse width	t _{WP}	50	—	50	—	60	—	70	—	ns
Address setup time	t _{AS}	0	—	0	—	0	—	0	—	ns
Write recovery time (WE)	t _{WR}	0	—	0	—	0	—	0	—	ns
Write recovery time (CE1, CE2)	t _{WR1}	0	—	0	—	0	—	0	—	ns
Output active from end of write	t _{OW}	10	—	10	—	10	—	10	—	ns
Write to output in high Z	t _{WHZ} *	0	25	0	25	0	25	0	25	ns

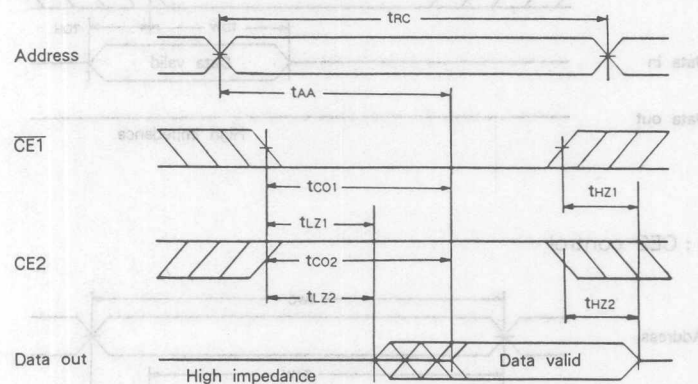
* t_{WHZ} is defined as the time required for outputs to turn to high impedance state and is not referred to as output voltage level.

Timing Waveform

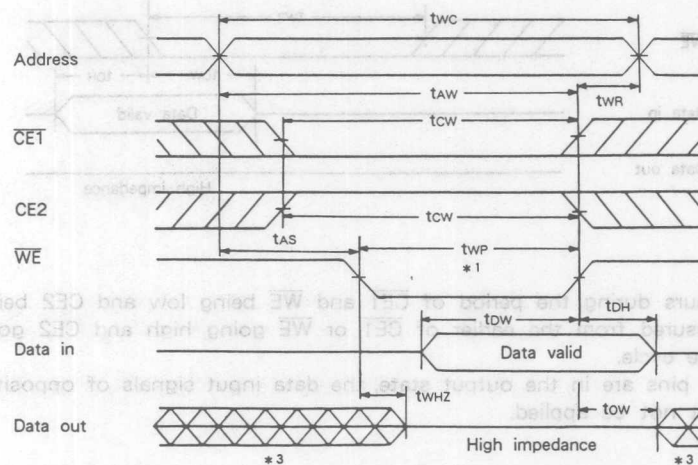
- Read cycle (1) : $\overline{CE1} = V_{IL}$, $CE2 = V_{IH}$, $\overline{WE} = V_{IH}$



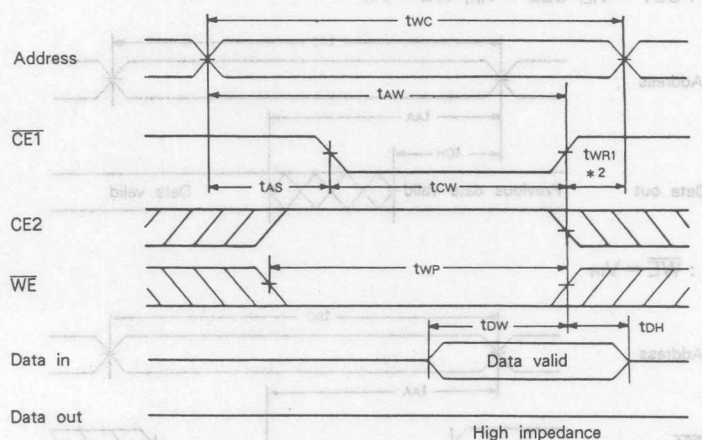
- Read cycle (2) : $\overline{WE} = V_{IH}$



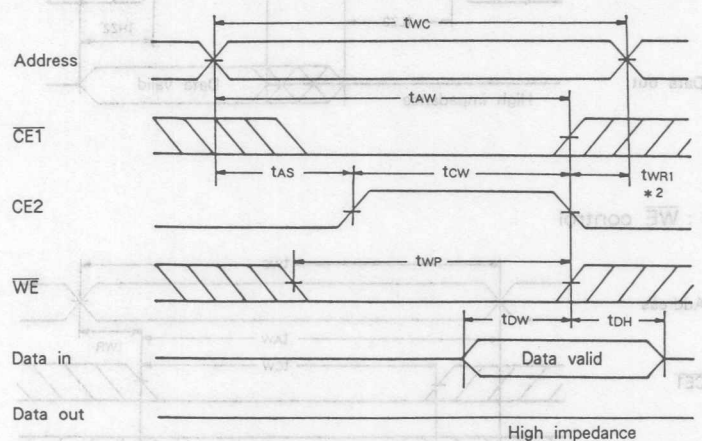
- Write cycle (1) : $\overline{WE}$ control



• Write cycle (2) : $\overline{\text{CE1}}$ control



• Write cycle (3) : CE2 control



- *1. A write occurs during the period of $\overline{\text{CE1}}$ and $\overline{\text{WE}}$ being low and CE2 being high.
- *2. tWR1 is measured from the earlier of $\overline{\text{CE1}}$ or $\overline{\text{WE}}$ going high and CE2 going low to the end of write cycle.
- *3. During I/O pins are in the output state, the data input signals of opposite phase to the output must not be applied.

Data Retention Characteristics

(Ta = 0 to 70 °C)

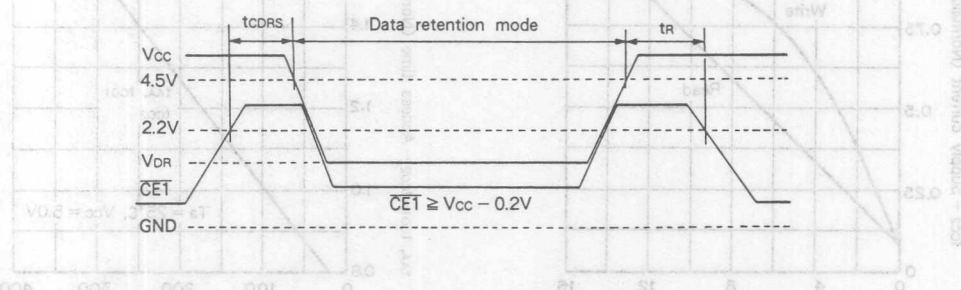
Item	Symbol	Test conditions	- 70L/85L/ 10L/12L			- 70LL/85LL/ 10LL/12LL			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Data retention voltage	V _{DR}	*1	2.0	—	5.5	2.0	—	5.5	V
Data retention current	I _{CCDR1}	V _{CC} = 3.0V *1	—	—	10	—	—	3	μA
		0 to 70 °C	—	—	10	—	—	3	
		0 to 40 °C	—	—	2	—	—	0.6	
	I _{CCDR2}	V _{CC} = 2.0 to 5.5V *1	—	0.25	1	—	0.1	0.3	μA
		25 °C	—	0.5	25	—	0.2	5	
Data retention setup time	t _{CDRS}	Chip disable to data retention mode	0	—	—	0	—	—	ns
Recovery time	t _R		t _{RC} *2	—	—	t _{RC} *2	—	—	ns

*1. $\overline{CE1} \geq V_{CC} - 0.2V$, $CE2 \geq V_{CC} - 0.2V$ ($\overline{CE1}$ control) or $CE2 \leq 0.2V$ ($CE2$ control)

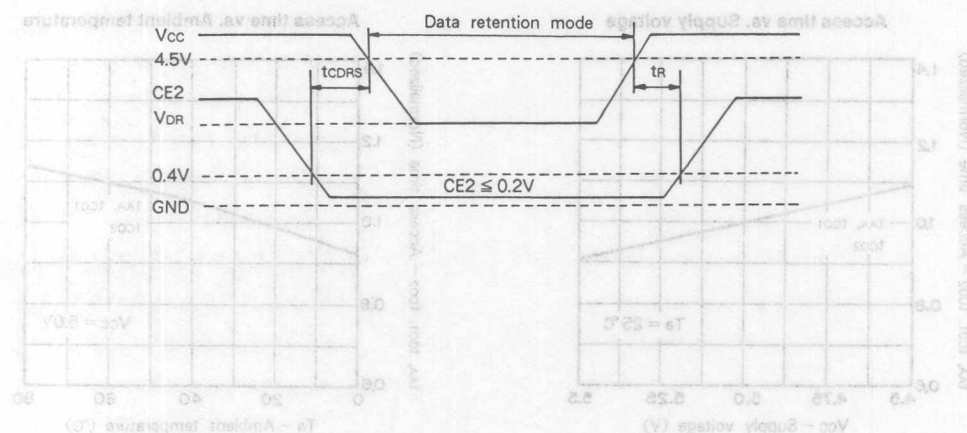
*2. t_{RC}: Read cycle time

Data retention waveform

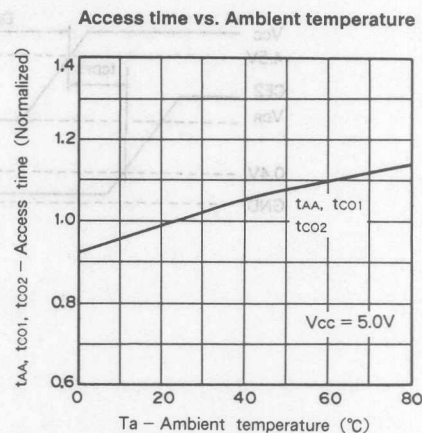
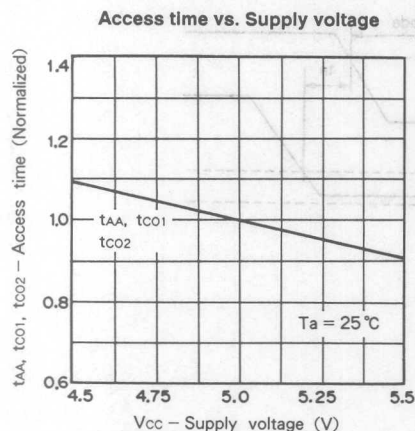
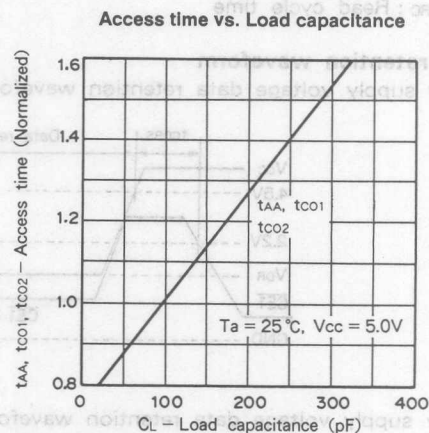
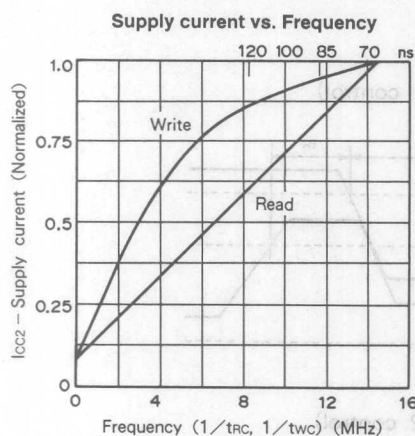
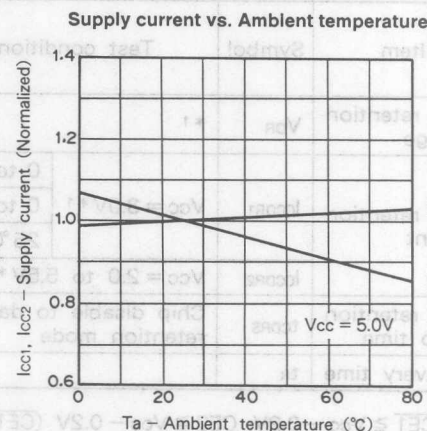
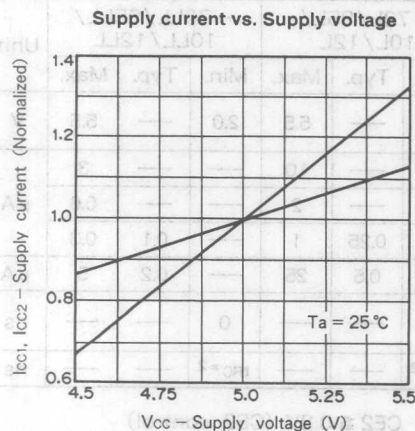
- Low supply voltage data retention waveform (1) ($\overline{CE1}$ control)



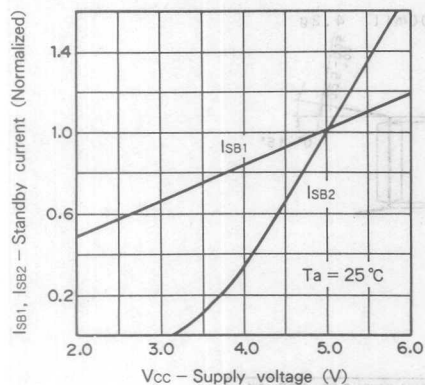
- Low supply voltage data retention waveform (2) ($CE2$ control)



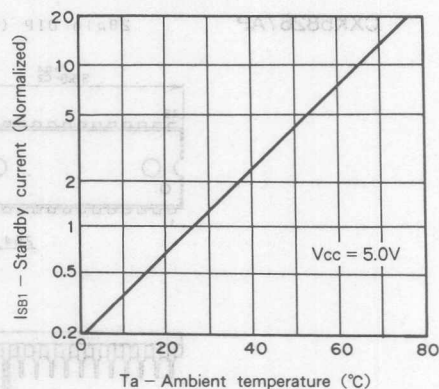
Example of Representative Characteristics



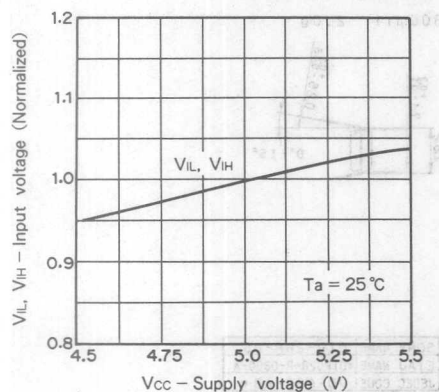
Standby current vs. Supply voltage



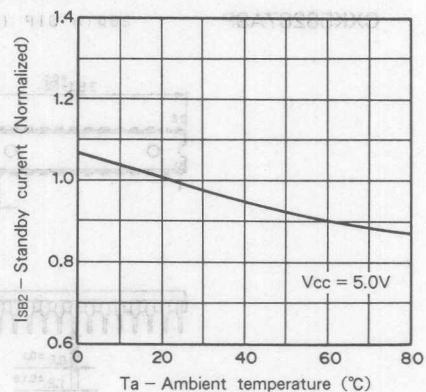
Standby current vs. Ambient temperature



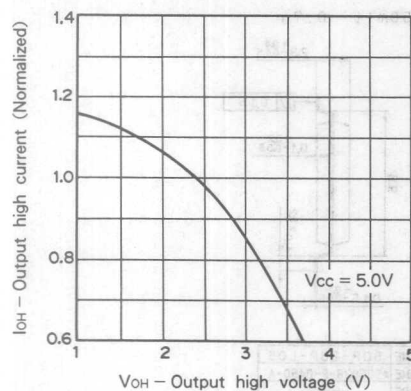
Input voltage level vs. Supply voltage



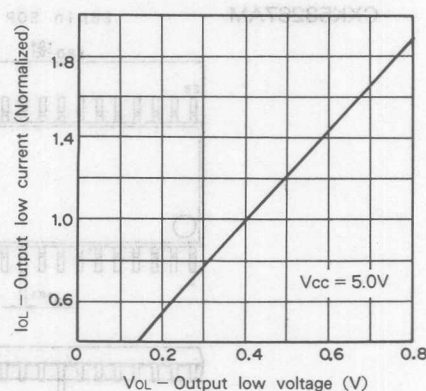
Standby current vs. Ambient temperature



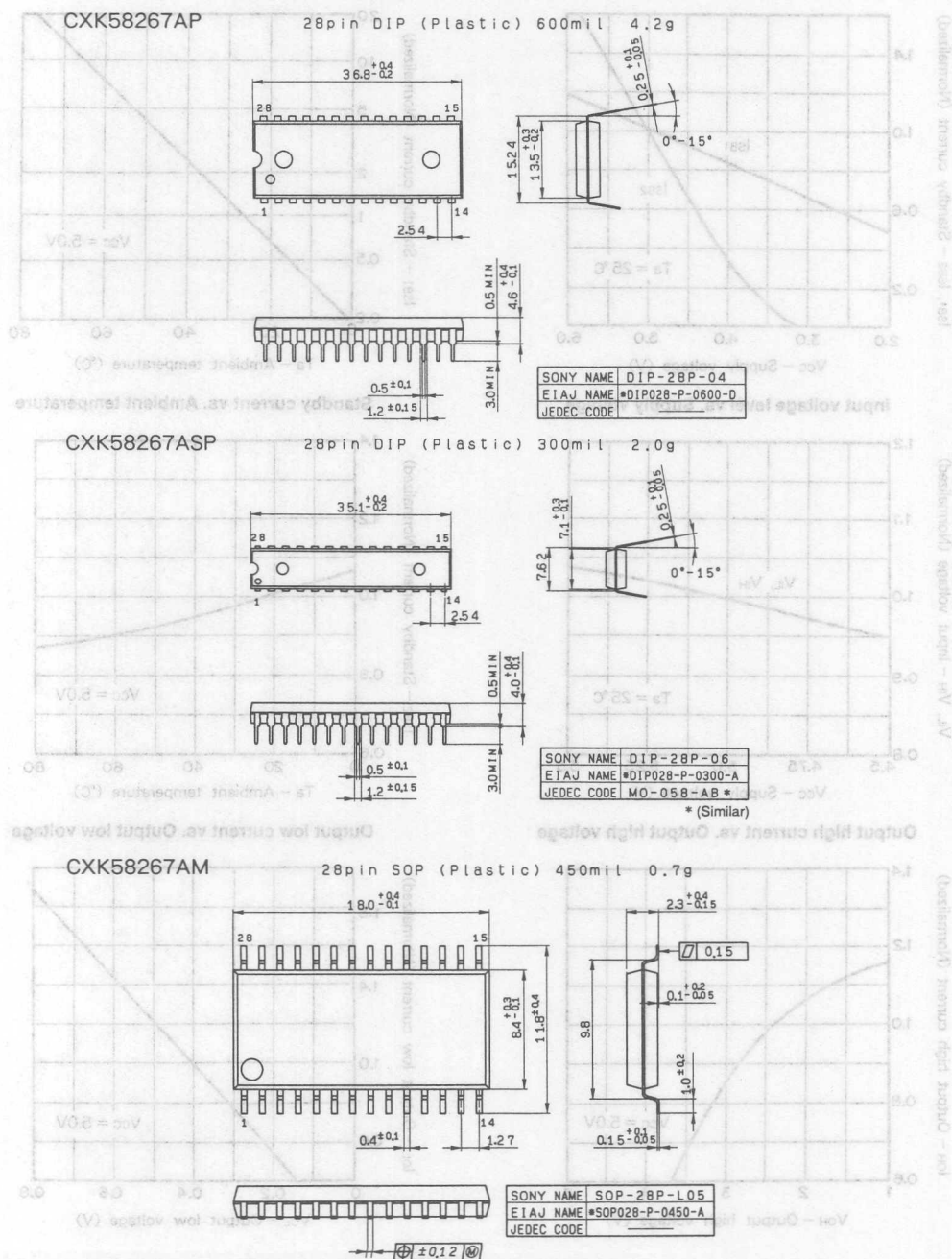
Output high current vs. Output high voltage



Output low current vs. Output low voltage



Package Outline Unit : mm



SONY® CXK58267ATM/AYM

-70L/85L/10L/12L
-70LL/85LL/10LL/12LL

32768-word × 8-bit High Speed CMOS Static RAM

Description

CXK58267ATM/AYM is a 256K bits, 32768 words by 8 bits, CMOS static RAM. It is suitable for portable and battery back-up systems which require extremely small package and low stand-by current. It has two chip enable control inputs, $\overline{CE1}$ & $\overline{CE2}$, which allow to achieve multiple memory use with battery back-up applications.

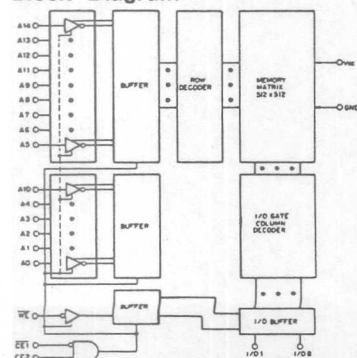
Features

- Two Chips Enable Control Inputs
Provide Stand-by/Data Retention Mode
 $\overline{CE1}$: Low Active
 $\overline{CE2}$: High Active
- Thin Small-outline Packages:
CXK58267ATM: 8mm × 13.4mm 28 pin TSOP
CXK58267AYM: 8mm × 13.4mm 28 pin TSOP
(Mirror image pinout)
- Low stand-by current:
L-Version:
25 μ A (Max.) @ $V_{CC} = 5.5V$, $T_a = 0$ to $70^\circ C$
LL-Version:
5 μ A (Max.) @ $V_{CC} = 5.5V$, $T_a = 0$ to $70^\circ C$
- Low voltage data retention: 2.0V (Min.)
- Fast access time: (Access time)
CXK58267ATM/AYM-70L, -70LL 70ns (Max.)
CXK58267ATM/AYM-85L, -85LL 85ns (Max.)
CXK58267ATM/AYM-10L, -10LL 100ns (Max.)
CXK58267ATM/AYM-12L, -12LL 120ns (Max.)
- Single +5V Supply: +5V $\pm$ 10%

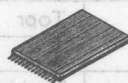
Function

32768-word × 8-bit static RAM

Block Diagram



CXK58267ATM 28 pin TSOP (Plastic) CXK58267AYM 28 pin TSOP (Plastic)



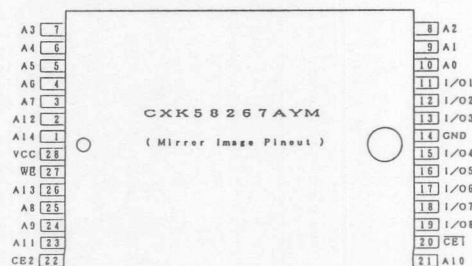
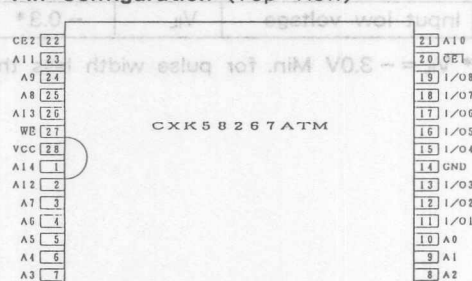
Structure

Silicon gate CMOS IC

Pin Description

Symbol	Description
A0 to A14	Address input
I/O0 to I/O7	Data input/output
$\overline{CE1}$, $\overline{CE2}$	Chip enable 1, 2 input
WE	Write enable input
VCC	+5V power supply
GND	Ground

Pin Configuration (Top View)



Absolute Maximum Ratings

(Ta = 25 °C, GND = 0V)

Item	Symbol	Rating	Unit
Supply voltage	V _{CC}	-0.5 to +7.0	V
Input voltage	V _{IN}	-0.5* to V _{CC} + 0.5	V
Input and output voltage	V _{I/O}	-0.5* to V _{CC} + 0.5	V
Allowable power dissipation	P _D	0.7	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	-55 to +150	°C
Soldering temperature • time	Tsolder	235 • 10	°C • sec

* V_{IN}, V_{I/O} = -3.0V Min. for pulse width less than 50ns.

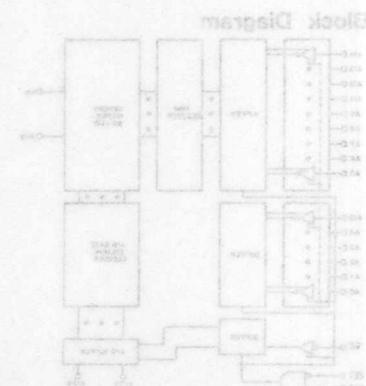
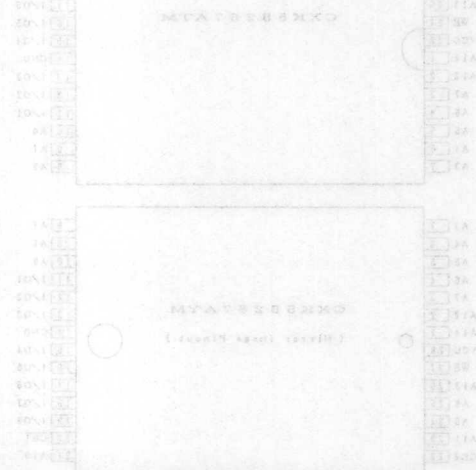
Truth Table

CET	CE2	WE	Mode	I/O1 to I/O8	V _{CC} Current
H	x	x	Not selected	High Z	Isb1, Isb2
x	L	x	Not selected	High Z	Isb1, Isb2
L	H	H	Read	Data out	Icc1, Icc2
L	H	L	Write	Data in	Icc1, Icc2

x : "H" or "L"

DC Recommended Operating Conditions (Ta = 0 to +70 °C, GND = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Input high voltage	V _{IH}	2.2	—	V _{CC} + 0.3	V
Input low voltage	V _{IL}	-0.3*	—	0.8	V

* V_{IL} = -3.0V Min. for pulse width less than 50ns.

Electrical Characteristics

• DC and operating characteristics (V_{CC} = 5V ± 10%, GND = 0V, T_a = 0 to +70°C)

Item	Symbol	Test conditions	-70L/85L/10L/12L			-70LL/85LL/10LL/12LL			Unit
			Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Input leakage current	I _{LI}	V _{IN} = GND to V _{CC}	-0.5	—	0.5	-0.5	—	0.5	μA
Output leakage current	I _{LO}	CE1 = V _{IH} or CE2 = V _{IL} or WE = V _{IL} , V _{I/O} = GND to V _{CC}	-0.5	—	0.5	-0.5	—	0.5	μA
Operating power supply current	I _{CC1}	CE1 = V _{IL} , CE2 = V _{IH} , I _{OUT} = 0mA	—	3	10	—	3	10	mA
		CE1 = 0.2V, CE2 = V _{CC} - 0.2V V _{IN} = 0.2V or V _{CC} - 0.2V	—	1	5	—	1	5	
Average operating current	I _{CC2}	Min. cycle Duty = 100%, I _{OUT} = 0mA	70L/70LL	—	30	50	—	30	mA
			85L/85LL	—	25	50	—	25	
			10L/10LL	—	23	50	—	23	
			12L/12LL	—	20	50	—	20	
Standby current	I _{SB1}	CE2 ≤ 0.2V or (CE1 ≥ V _{CC} - 0.2V CE2 ≥ V _{CC} - 0.2V)	0 to 70°C	—	—	25	—	—	μA
			0 to 40°C	—	—	5	—	—	
			25°C	—	0.5	2	—	0.2	
	I _{SB2}	CE2 = V _{IL} , or CE1 = V _{IH}	—	0.6	3	—	0.6	3	mA
Output high voltage	V _{OH}	I _{OH} = -1.0mA	2.4	—	—	2.4	—	—	V
Output low voltage	V _{OL}	I _{OL} = 2.1mA	—	—	0.4	—	—	0.4	V

* V_{CC} = 5V, T_a = 25°C

I/O capacitance

(T_a = 25°C, f = 1MHz)

Item	Symbol	Test conditions	Min.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} = 0V	—	6	pF
I/O capacitance	C _{I/O}	V _{I/O} = 0V	—	8	pF

Note) This parameter is sampled and is not 100% tested.

AC characteristics

● AC test conditions (Vcc = 5V ± 10%, Ta = 0 to +70°C)

Item	Conditions
Input pulse high level	V _{IH} = 2.2V
Input pulse low level	V _{IL} = 0.8V
Input rise time	t _r = 5ns
Input fall time	t _f = 5ns
Input and output reference level	1.5V
Output load conditions	85L / 85LL / 10L / 10LL / 12L / 12LL
	70L / 70LL
	C _L * = 100pF, 1TTL
	C _L * = 30pF, 1TTL

* C_L includes scope and jig capacitances.

Item	Symbol	Test conditions	Min.	Typ.	Max.
Average operating current	I _{OP}	Min. cycle Duty = 100% I _{OUT} = 0mA	—	—	—
Standby current	I _{STB}	CET = 0.2V or CET = V _{IL} or CET = V _{IH}	—	—	—
Output high voltage	V _{OH}	I _{OH} = -1.0mA	—	—	—
Output low voltage	V _{OL}	I _{OL} = 5.1mA	—	—	—

* V_{CC} = 5V, Ta = 25°C

Item	Symbol	Test conditions	Min.	Max.	Unit
Input capacitance	C _{IN}	V _{IH} = 0V	—	8	pF
V _{OL} capacitance	C _{VO}	V _{OL} = 0V	—	8	pF

(Note) This parameter is sampled and is not 100% tested.

• Read cycle

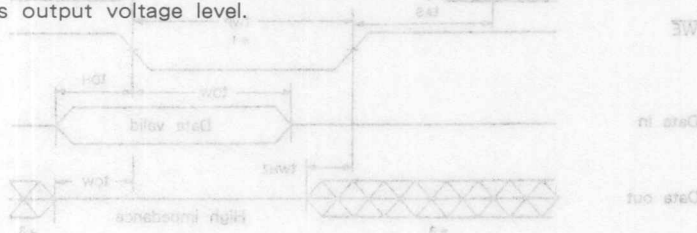
Item	Symbol	-70L/70LL		-85L/85LL		-10L/10LL		-12L/12LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t _{RC}	70	—	85	—	100	—	120	—	ns
Address access time	t _{AA}	—	70	—	85	—	100	—	120	ns
Chip enable access time (CE1, CE2)	t _{CO1} , t _{CO2}	—	70	—	85	—	100	—	120	ns
Output hold from address change	t _{OH}	20	—	20	—	20	—	20	—	ns
Chip enable to output in low Z (CE1, CE2)	t _{LZ1} , t _{LZ2}	10	—	10	—	10	—	10	—	ns
Chip disable to output in high Z (CE1, CE2)	t _{HZ1} *, t _{HZ2} *	0	30	0	30	0	30	0	30	ns

* t_{HZ1} and t_{HZ2} are defined as the time required for outputs to turn to high impedance state and are not referred to as output voltage levels.

• Write cycle

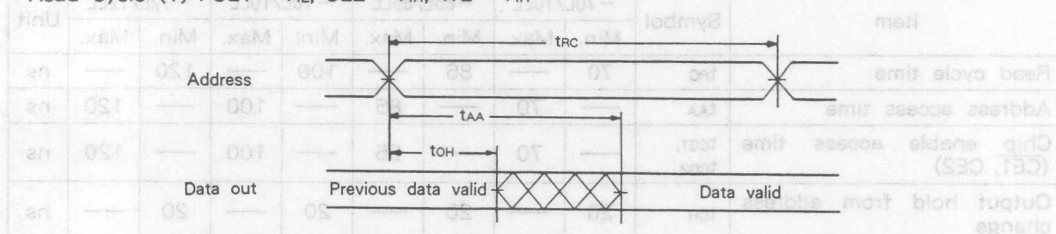
Item	Symbol	-70L/70LL		-85L/85LL		-10L/10LL		-12L/12LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t _{WC}	70	—	85	—	100	—	120	—	ns
Address valid to end of write	t _{AW}	65	—	75	—	80	—	100	—	ns
Chip enable to end of write	t _{CW}	65	—	75	—	80	—	100	—	ns
Data to write time overlap	t _{DW}	30	—	30	—	35	—	40	—	ns
Data hold from write time	t _{DH}	0	—	0	—	0	—	0	—	ns
Write pulse width	t _{WP}	50	—	50	—	60	—	70	—	ns
Address setup time	t _{AS}	0	—	0	—	0	—	0	—	ns
Write recovery time (WE)	t _{WR}	0	—	0	—	0	—	0	—	ns
Write recovery time (CE1, CE2)	t _{WR1}	0	—	0	—	0	—	0	—	ns
Output active from end of write	t _{OW}	10	—	10	—	10	—	10	—	ns
Write to output in high Z	t _{WHZ} *	0	25	0	25	0	25	0	25	ns

* t_{WHZ} is defined as the time required for outputs to turn to high impedance state and is not referred to as output voltage level.

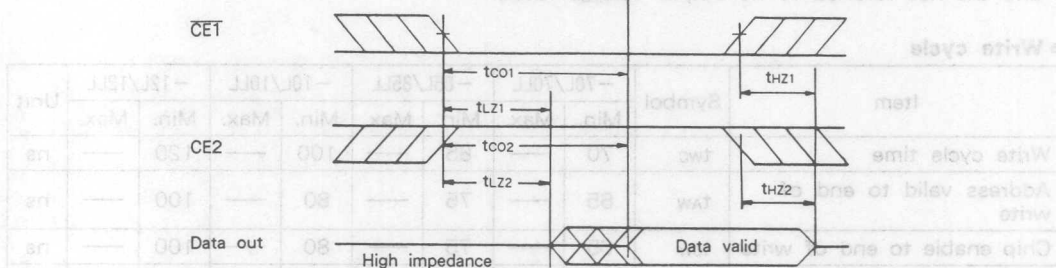
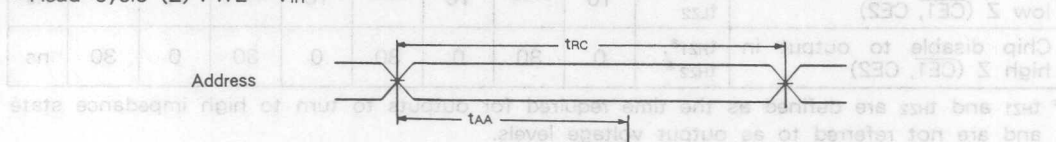


Timing Waveform

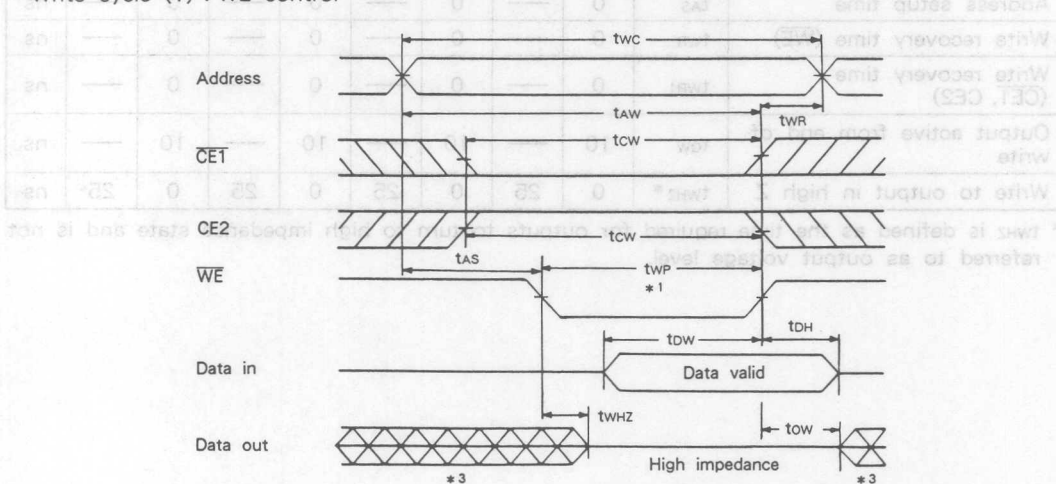
- Read cycle (1) : $\overline{CE1} = V_{IL}$, $CE2 = V_{IH}$, $\overline{WE} = V_{IH}$



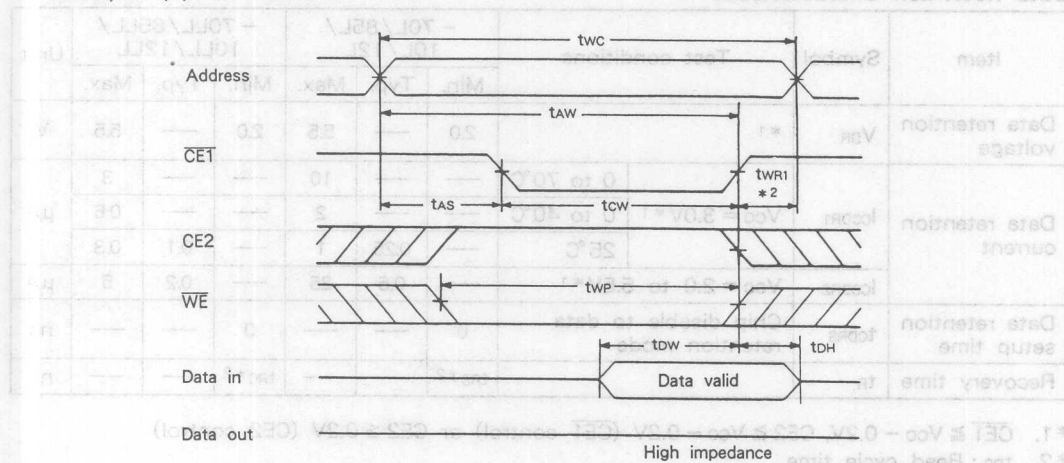
- Read cycle (2) : $\overline{WE} = V_{IH}$



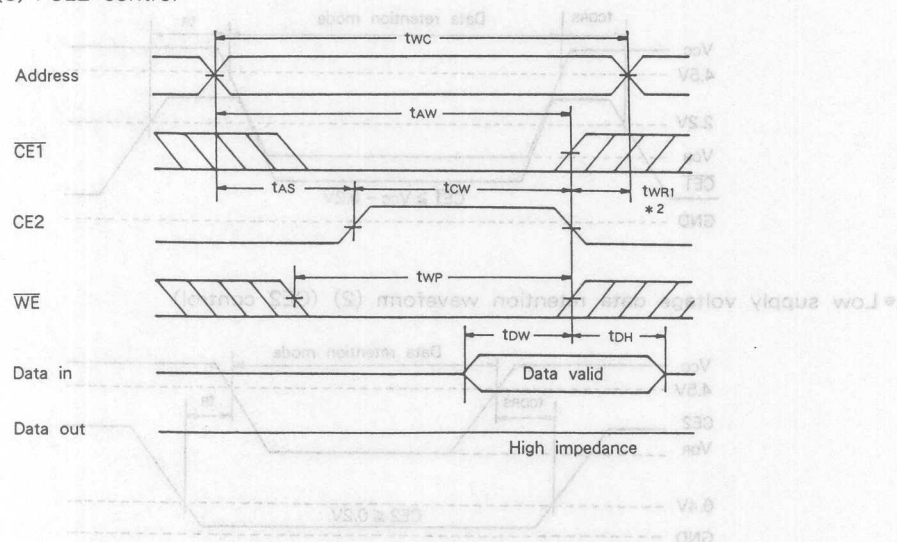
- Write cycle (1) : $\overline{WE}$ control



• Write cycle (2) : $\overline{\text{CE1}}$ control



• Write cycle (3) : $\overline{\text{CE2}}$ control



- *1. A write occurs during the period of $\overline{\text{CE1}}$ and $\overline{\text{WE}}$ being low and $\overline{\text{CE2}}$ being high.
- *2. t_{wr1} is measured from the earlier of $\overline{\text{CE1}}$ or $\overline{\text{WE}}$ going high and $\overline{\text{CE2}}$ going low to the end of write cycle.
- *3. During I/O pins are in the output state, the data input signals of opposite phase to the output must not be applied.

Data Retention Characteristics

(Ta = 0 to 70°C)

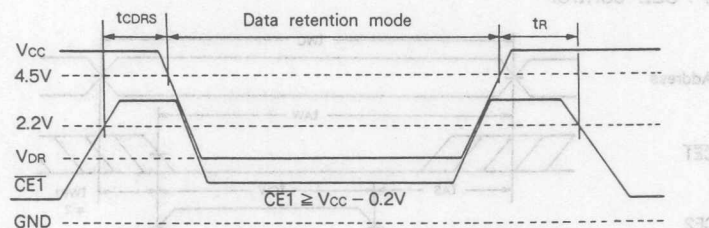
Item	Symbol	Test conditions		- 70L/85L/ 10L/12L			- 70LL/85LL/ 10LL/12LL			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
Data retention voltage	V _{DR}	*1		2.0	—	5.5	2.0	—	5.5	V
Data retention current	I _{CCDR1}		0 to 70°C	—	—	10	—	—	3	μA
			0 to 40°C	—	—	2	—	—	0.6	
			25°C	—	0.25	1	—	0.1	0.3	
	I _{CCDR2}		V _{CC} = 2.0 to 5.5V *1	—	0.5	25	—	0.2	5	μA
Data retention setup time	t _{CDRS}	Chip disable to data retention mode		0	—	—	0	—	—	ns
Recovery time	t _R			t _{RC} *2	—	—	t _{RC} *2	—	—	ns

*1. $\overline{CE1} \geq V_{CC} - 0.2V$, $CE2 \geq V_{CC} - 0.2V$ ($\overline{CE1}$ control) or $CE2 \leq 0.2V$ ($CE2$ control)

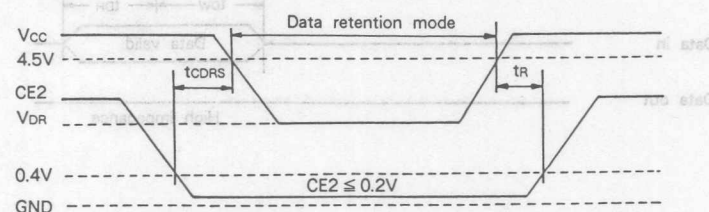
*2. t_{RC}: Read cycle time

Data retention waveform

- Low supply voltage data retention waveform (1) ($\overline{CE1}$ control)

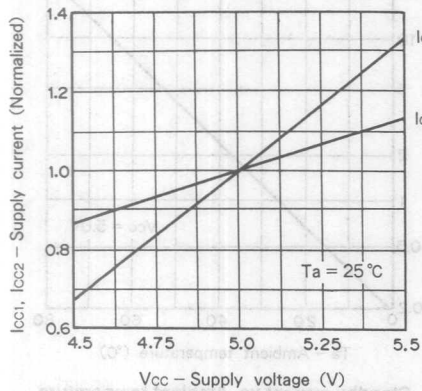


- Low supply voltage data retention waveform (2) ($CE2$ control)

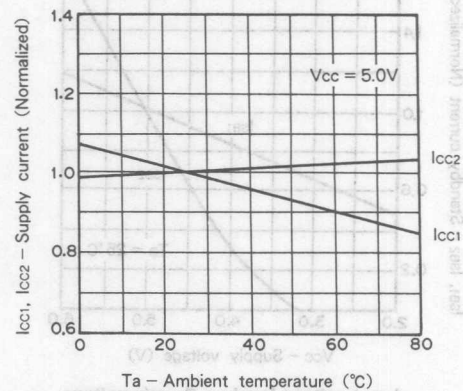


Example of Representative Characteristics

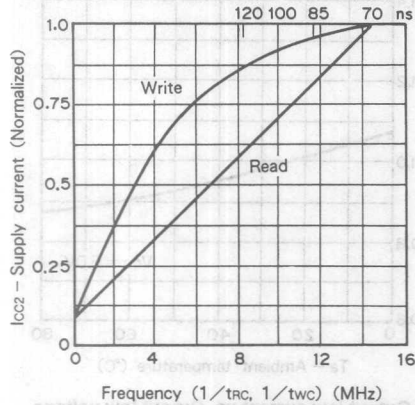
Supply current vs. Supply voltage



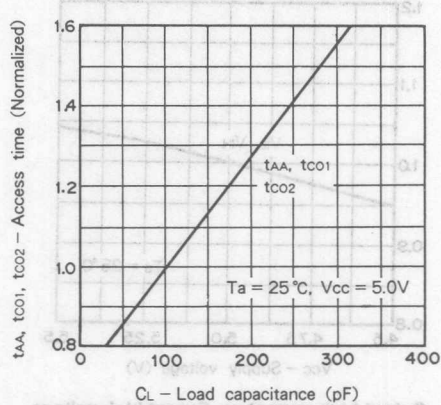
Supply current vs. Ambient temperature



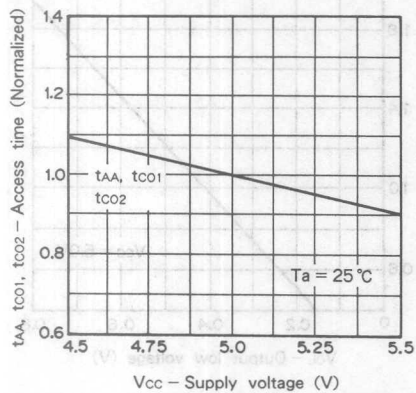
Supply current vs. Frequency



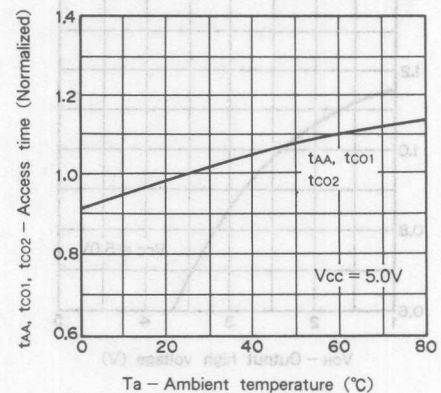
Access time vs. Load capacitance



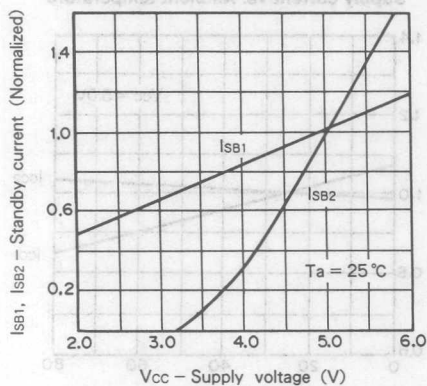
Access time vs. Supply voltage



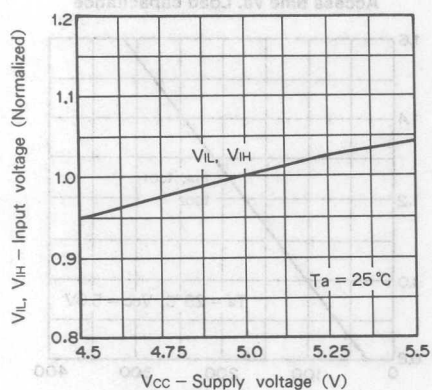
Access time vs. Ambient temperature



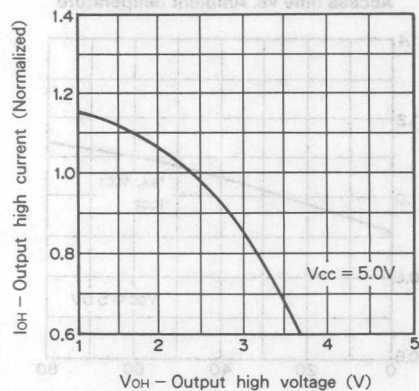
Standby current vs. Supply voltage



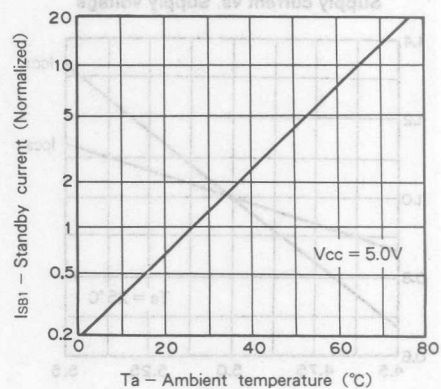
Input voltage level vs. Supply voltage



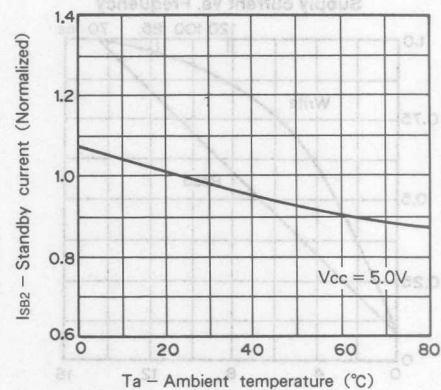
Output high current vs. Output high voltage



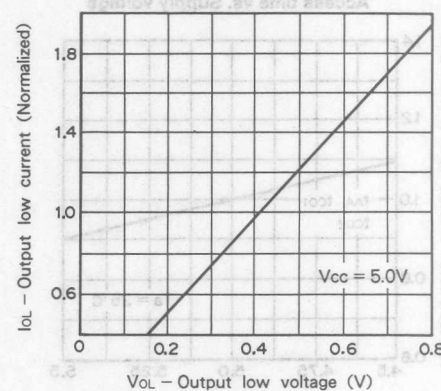
Standby current vs. Ambient temperature



Standby current vs. Ambient temperature



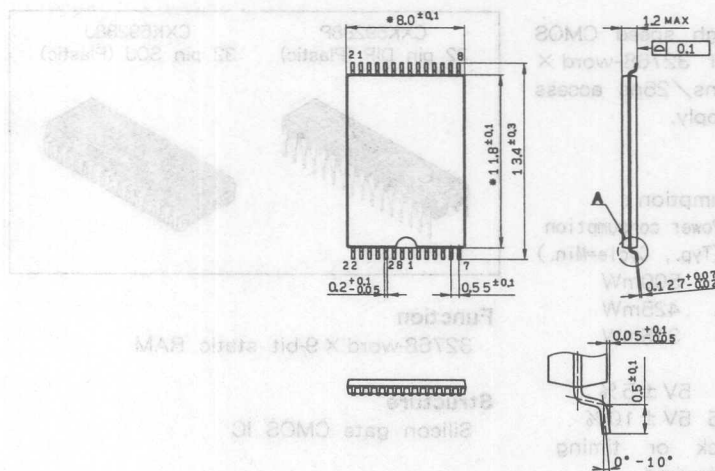
Output low current vs. Output low voltage



Package Outline Unit : mm

CXK58267ATM

28pin TSOP (Plastic)



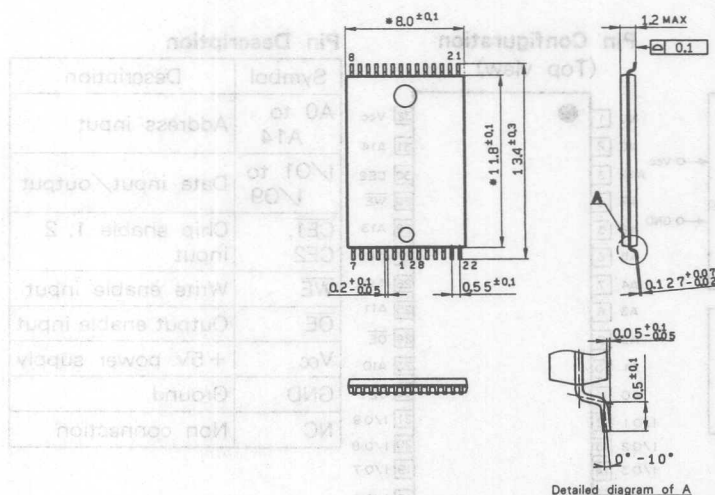
Detailed diagram of A

Note) Dimensions marked with *
do not include resin residue.

SONY NAME	TSOP-28P-L01
EIAJ NAME	TSOP028-P-0000-A
JEDEC CODE	

CXK58267AYM

28pin TSOP (Plastic)



Detailed diagram of A

Note) Dimensions marked with *
do not include resin residue.

SONY NAME	TSOP-28P-L01R
EIAJ NAME	TSOP028-P-0000-B
JEDEC CODE	

SONY

CXK59288P/J -15/20/25

32768-word × 9-bit High Speed CMOS Static RAM

Description

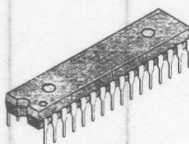
The CXK59288P/J is a high speed CMOS static RAM which consists of 32768-word × 9-bit. It operates at 15ns/20ns/25ns access time from 5V single power supply.

Features

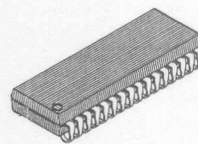
- High speed, low power consumption :

	Access time (Max.)	Power consumption (Typ., Cycle=Min.)
CXK59288P/J-15	15ns	500mW
CXK59288P/J-20	20ns	425mW
CXK59288P/J-25	25ns	375mW
- Single +5V power supply :
 - 15 5V ± 5%
 - 20/25 5V ± 10%
- Fully static memory...No clock or timing strobe required.
- Equal access and cycle time.
- Directly TTL compatible all inputs and outputs.
- Available in 32 pin 300mil DIP, 300mil SOJ package.

CXK59288P
32 pin DIP (Plastic)



CXK59288J
32 pin SOJ (Plastic)



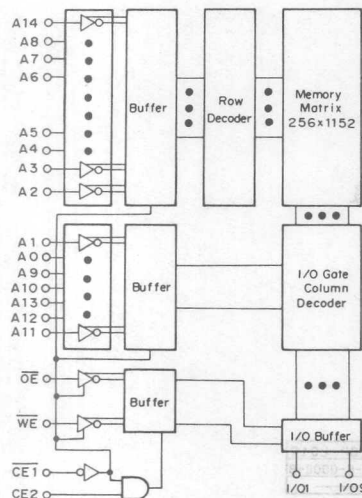
Function

32768-word × 9-bit static RAM

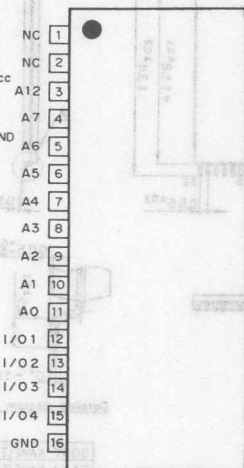
Structure

Silicon gate CMOS IC

Block Diagram



Pin Configuration (Top view)



Pin Description

Symbol	Description
A0 to A14	Address input
I/O1 to I/O9	Data input/output
CE1, CE2	Chip enable 1, 2 input
WE	Write enable input
OE	Output enable input
Vcc	+ 5V power supply
GND	Ground
NC	Non connection

Absolute Maximum Ratings

(Ta = 25°C, GND = 0V)

Item	Symbol	Rating	Unit
Supply voltage	V _{CC}	-0.5* to +7.0	V
Input voltage	V _{IN}	-0.5* to V _{CC} + 0.5	V
Input and output voltage	V _{I/O}	-0.5* to V _{CC} + 0.5	V
Allowable power dissipation	P _D	1.0	W
Operating temperature	T _{opr}	0 to +70	°C
Storage temperature	T _{stg}	-55 to +150	°C
Soldering temperature * time	T _{solder}	260 * 10	°C * sec

* V_{CC}, V_{IN}, V_{I/O} = -3.5V Min. for pulse width less than 20ns.

Truth Table

CE1	CE2	OE	WE	Mode	I/O1 to I/O9	V _{CC} Current
H	x	x	x	Not selected	High Z	I _{SB1} , I _{SB2}
L	L	x	x	Not selected	High Z	I _{CC1} , I _{CC2}
L	H	H	H	Output disable	High Z	I _{CC1} , I _{CC2}
L	H	L	H	Read	Data out	I _{CC1} , I _{CC2}
L	H	x	L	Write	Data in	I _{CC1} , I _{CC2}

x : "H" or "L"

DC Recommended Operating Conditions

(Ta = 0 to +70°C, GND = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V _{CC}	4.75	5.0	5.25	V
		4.5	5.0	5.5	
Input high voltage	V _{IH}	2.2	—	V _{CC} + 0.3	V
Input low voltage	V _{IL}	-0.3*	—	0.8	V

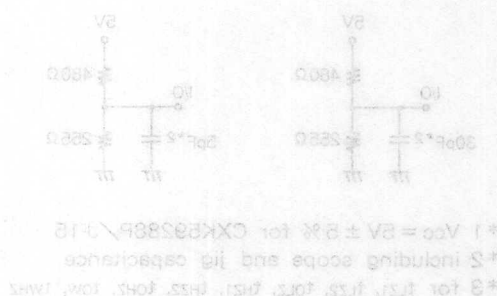
* V_{IL} = -3.0V Min. for pulse width less than 20ns.

Fig. 1

Item	Conditions
Input pulse high level	V _{IH} = 3.0V
Input pulse low level	V _{IL} = 0V
Input rise time	t _r = 3ns
Input fall time	t _f = 3ns
Input and output reference level	V _{REF} = 1.5V
Output load conditions	Fig. 1

Electrical Characteristics

• DC and operating characteristics (V_{CC} = 5V ± 10%*, GND = 0V, T_a = 0 to +70°C)

Item	Symbol	Test conditions	Min.	Typ.**	Max.	Unit
Input leakage current	I _{LI}	V _{IN} = GND to V _{CC}	-1	—	-1	μA
Output leakage current	I _{LO}	V _{I/O} = GND to V _{CC} , CE1 = V _{IH} or CE2 = V _{IL} or OE = V _{IH} or WE = V _{IL}	-1	—	-1	μA
Operating power supply current	I _{CC1}	CE1 = V _{IL} , V _{IN} = V _{IH} or V _{IL} , I _{OUT} = 0mA	—	—	—	—
Average operating current	I _{CC2}	Cycle = Min, Duty = 100%, I _{OUT} = 0mA	-15	100	130	mA
			-20	85	120	
			-25	75	120	
Standby current	I _{SB1}	CE1 ≥ V _{CC} - 0.2V, V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V	—	—	1	mA
	I _{SB2}	CE1 = V _{IH} , V _{IN} = V _{IH} /V _{IL} , Cycle = Min.	—	15	25	
Output high voltage	V _{OH}	I _{OH} = -4.0mA	2.4	—	—	V
Output low voltage	V _{OL}	I _{OL} = 8.0mA	—	—	0.4	V

* V_{CC} = 5V ± 5% for CXK59288P/J-15** V_{CC} = 5V, T_a = 25°C

I/O capacitance

(T_a = 25°C, f = 1MHz)

Item	Symbol	Test conditions	Min.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} = 0V	—	6	pF
I/O capacitance	C _{I/O}	V _{I/O} = 0V	—	7	pF

Note) This parameter is sampled and is not 100% tested.

AC characteristics

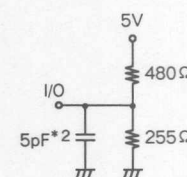
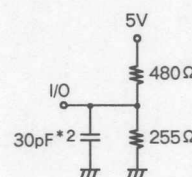
• AC test conditions

(V_{CC} = 5V ± 10%*, T_a = 0 to +70°C)

Item	Conditions
Input pulse high level	V _{IH} = 3.0V
Input pulse low level	V _{IL} = 0V
Input rise time	tr = 3ns
Input fall time	tf = 3ns
Input and output reference level	1.5V
Output load conditions	Fig. 1

Output Load (1)

Output Load (2)*3

*1 V_{CC} = 5V ± 5% for CXK59288P/J-15

*2 including scope and jig capacitance

*3 for t_{LZ1}, t_{LZ2}, t_{OLZ}, t_{HZ1}, t_{HZ2}, t_{OHZ}, t_{OW}, t_{WHZ}

Fig. 1

• Read cycle

Item	Symbol	- 15		- 20		- 25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t _{RC}	15	—	20	—	25	—	ns
Address access time	t _{AA}	—	15	—	20	—	25	ns
Chip enable access time (CE1)	t _{CO1}	—	15	—	20	—	25	ns
Chip enable access time (CE2)	t _{CO2}	—	8	—	10	—	12	ns
Output enable to output valid	t _{OE}	—	8	—	10	—	12	ns
Output hold from address change	t _{OH}	5	—	5	—	5	—	ns
Chip enable to output in low Z (CE1, CE2)	t _{LLZ1} *, t _{LLZ2} *	3	—	3	—	3	—	ns
Output enable to output in low Z (OE)	t _{OLZ} *	2	—	2	—	2	—	ns
Chip disable to output in high Z (CE1, CE2)	t _{HZ1} *, t _{HZ2} *	—	8	—	9	—	10	ns
Chip disable to output in high Z (OE)	t _{OHZ} *	—	7	—	8	—	9	ns
Chip enable to power up time (CE1)	t _{PU}	0	—	0	—	0	—	ns
Chip disable to power down time (CE1)	t _{PD}	—	15	—	20	—	25	ns

* Transition is measured $\pm 200\text{mV}$ from steady voltage with specified loading in Fig. 1-(2).
This parameter is sampled and is not 100% tested.

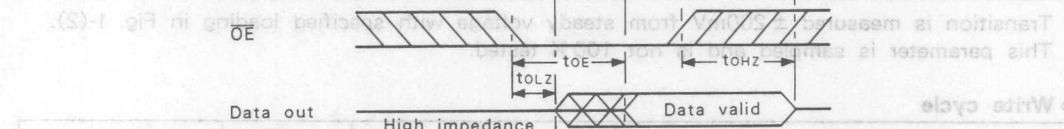
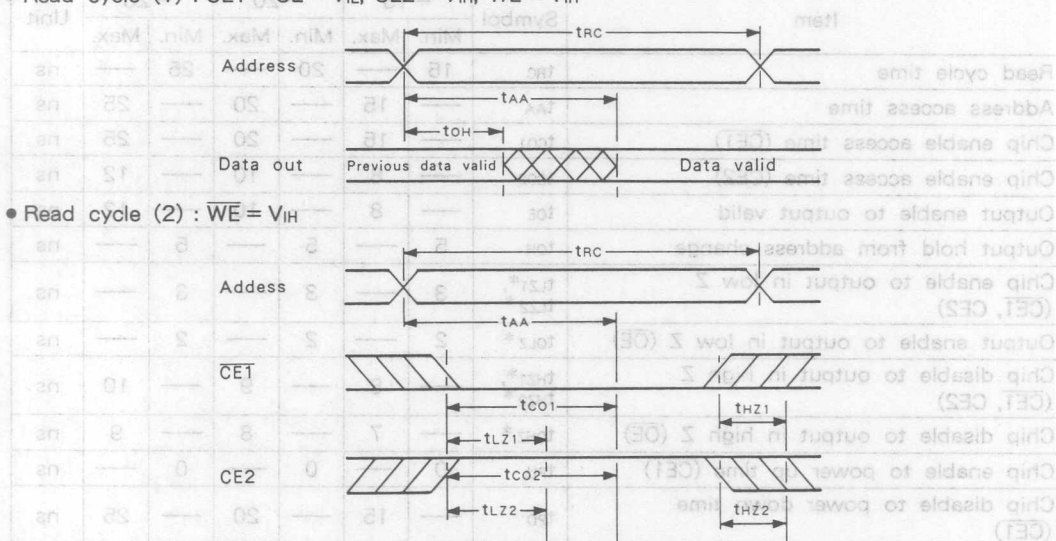
• Write cycle

Item	Symbol	- 15		- 20		- 25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t _{WC}	15	—	20	—	25	—	ns
Address valid to end of write	t _{AW}	10	—	13	—	15	—	ns
Chip enable to end of write	t _{CW}	11	—	14	—	16	—	ns
Data to write time overlap	t _{DW}	8	—	10	—	12	—	ns
Data hold from write time	t _{DH}	0	—	0	—	0	—	ns
Write pulse width	t _{WP}	10	—	13	—	15	—	ns
Address set up time	t _{AS}	0	—	0	—	0	—	ns
Write recovery time (WE)	t _{WR}	0	—	0	—	0	—	ns
Write recovery time (CE1, CE2)	t _{WR1}	0	—	0	—	0	—	ns
Output active from end of write	t _{OW} *	3	—	3	—	3	—	ns
Write to output in high Z	t _{WHZ} *	0	8	0	9	0	10	ns

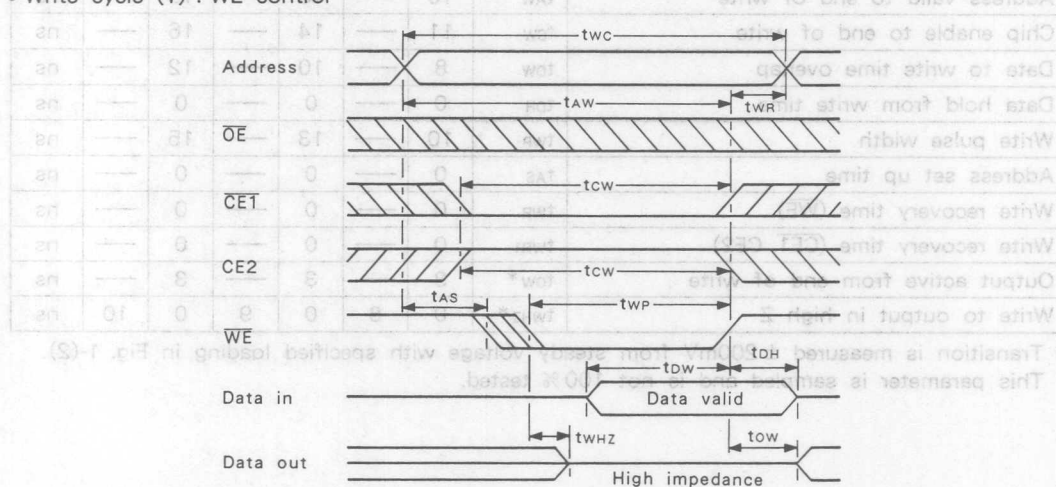
* Transition is measured $\pm 200\text{mV}$ from steady voltage with specified loading in Fig. 1-(2).
This parameter is sampled and is not 100% tested.

Timing Waveform

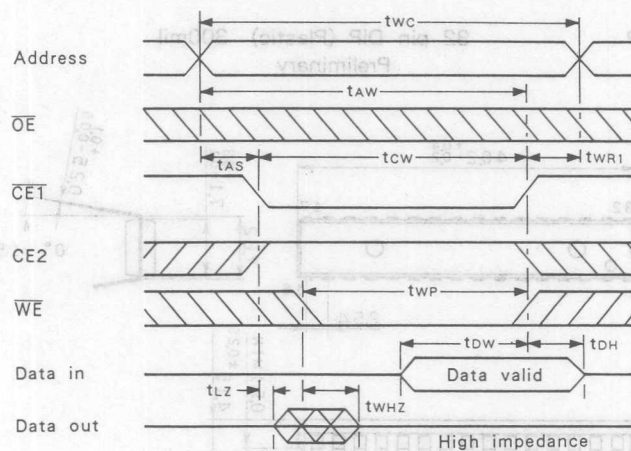
- Read cycle (1) : $\overline{CE1} = \overline{OE} = V_{IL}$, $CE2 = V_{IH}$, $WE = V_{IH}$



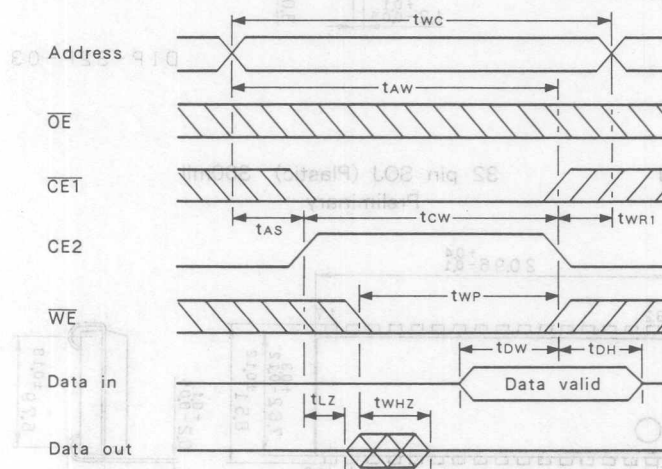
- Write cycle (1) : WE control



• Write cycle (2) : $\overline{\text{CE1}}$ control



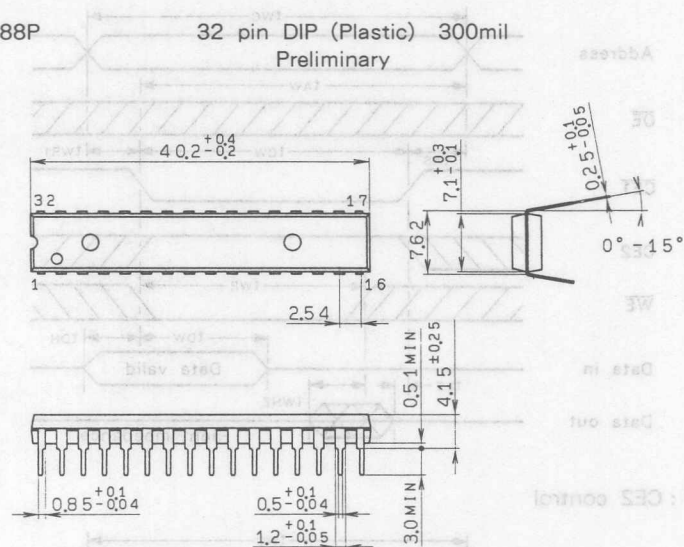
• Write cycle (3) : CE2 control



* During I/O pins are in the output state, the data input signals of opposite phase to the output must not be applied.

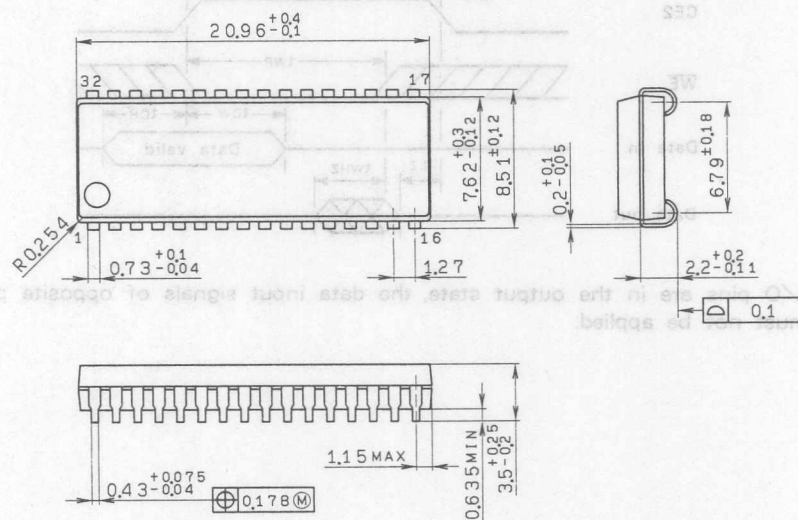
Package Outline Unit : mm

CXK59288P

32 pin DIP (Plastic) 300mil
Preliminary

DIP-32P-03

CXK59288J

32 pin SOJ (Plastic) 300mil
Preliminary

SOJ-32P-02

32768-word $\times$ 9-bit High Speed CMOS Static RAM

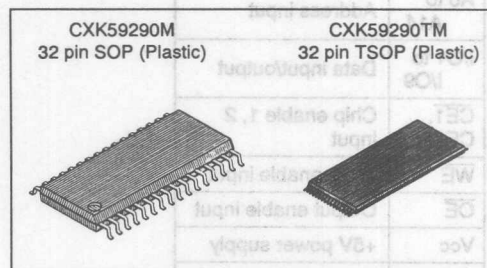
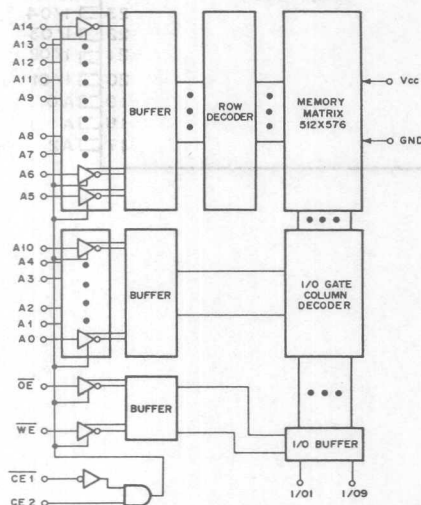
Description

The CXK59290M/TM is a 294912 bits high speed CMOS static RAM organized as 32768 words by 9 bits and operates from a single 5V supply. This device is suitable for use in high speed and low power applications in which battery back up for nonvolatility is required.

Features

- Fast access time: (Access time)
CXK59290M/TM-70L 70ns (Max.)
CXK59290M/TM-10L 100ns (Max.)
CXK59290M/TM-12L 120ns (Max.)
- Low power operation: Standby/Operation
CXK59290M/TM-70L, 10L, 12L:
2.5 μ W (Typ.)/15mW (Typ.)
- Single +5V supply: +5V $\pm$ 10%
- Fully static memory...No clock or timing strobe required.
- Equal access and cycle time
- Common data input and output: three state output
- Directly TTL compatible: All inputs and outputs
- Low voltage data retention: 2.0V (Min.)
- Available in 32 pin 450mil SOP and
32 pin 8mm $\times$ 20mm TSOP (EIAJ Standard)

Block Diagram



Function

32768-word $\times$ 9-bit static RAM

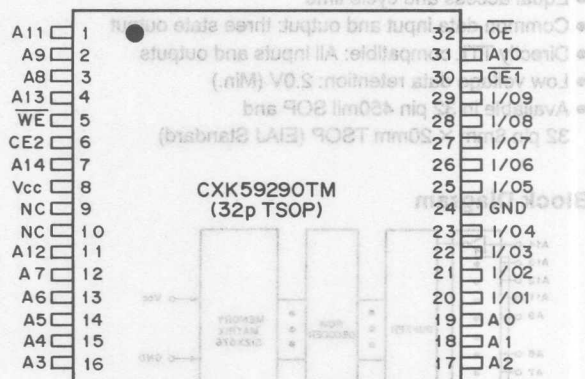
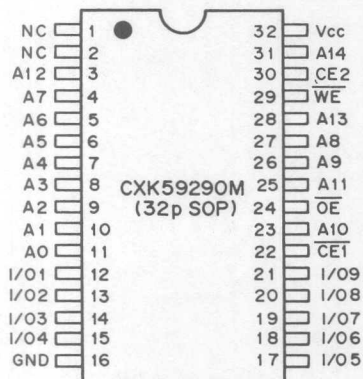
Structure

Silicon gate CMOS IC

Sony reserves the right to change products and specifications without prior notice. This information does not convey any license by any implication or otherwise under any patents or other right. Application circuits shown, if any, are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits.

Pin Description

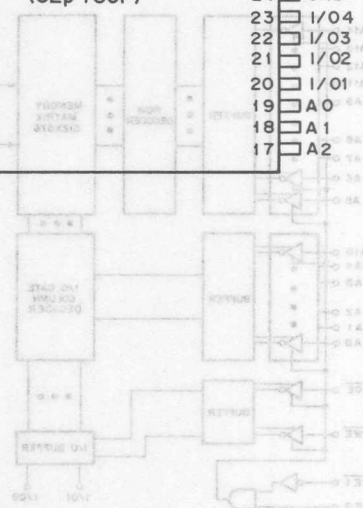
Symbol	Description
A0 to A14	Address input
I/O1 to I/O9	Data input/output
CE1, CE2	Chip enable 1, 2 input
WE	Write enable input
OE	Output enable input
Vcc	+5V power supply
GND	Ground
NC	No connection

Pin Configuration
(Top View)

The CXK59290M/TM is a 504Kbit high speed CMOS static RAM organized as 32768 words by 9 bits and operates from a single 5V supply. This device is suitable for use in high speed and low power applications in which battery back up for nonvolatility is required.

Features

- Fast access time: CXK59290M/TM-70L 70ns (Max.) CXK59290M/TM-10L 100ns (Max.) CXK59290M/TM-12L 120ns (Max.)
- Low power operation: Standby operation CXK59290M/TM-70L, 10L, 12L: 3.2uW (Typ.)/15mW (Typ.)
- Single +5V supply: +5V $\pm$ 10%
- Fully static memory: No clock or timing strobe required.
- Equal access and cycle time
- Command input and output three state output
- Command input: All inputs and outputs
- Command retention: 2.0V (Min.)
- Average I/O: 450mS SOP and 32 (TSOP) (EIA Standard)

CXK59290TM
(32p TSOP)

Sony reserves the right to change products and specifications without prior notice. This information does not constitute a warranty and is provided for reference only. Application circuits shown in this document are typical examples illustrating the operation of the device. Sony cannot assume responsibility for any conditions arising out of the use of these circuits.

Absolute Maximum Ratings

(Ta=25°C, GND=0V)

Item	Symbol	Rating	Unit
Supply voltage	V _{CC}	-0.5 to +7.0	V
Input voltage	V _{IN}	-0.5 * to V _{CC} +0.5	V
Input and output voltage	V _{I/O}	-0.5 * to V _{CC} +0.5	V
Allowable power dissipation	P _D	0.7	W
Operating temperature	T _{opr}	0 to +70	°C
Storage temperature	T _{stg}	-55 to +150	°C
Soldering temperature	T _{solder}	M	260 • 10
		TM	235 • 10

* V_{IN}, V_{I/O}=-3.0V Min. for pulse width less than 50ns.

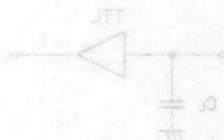
Truth Table

CE1	CE2	OE	WE	Mode	I/O1 to I/O9	V _{CC} Current
H	X	X	X	Not selected	High Z	I _{SB1} , I _{SB2}
X	L	X	X	Not selected	High Z	I _{SB1} , I _{SB2}
L	H	H	H	Output disable	High Z	I _{CC1} , I _{CC2}
L	H	L	H	Read	Data out	I _{CC1} , I _{CC2}
L	H	X	L	Write	Data in	I _{CC1} , I _{CC2}

X: "H" or "L"

DC Recommended Operating Conditions (Ta=0 to +70°C, GND=0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Input high voltage	V _{IH}	2.2	—	V _{CC} +0.3	V
Input low voltage	V _{IL}	-0.3 *	—	0.8	V

* V_{IL}=-3.0V Min. for pulse width less than 50ns.

Item	Conditions
Input pulse high level	V _{IN} =2.5V
Input pulse low level	V _{IL} =0.8V
Input rise time	t _r =2ns
Input fall time	t _f =2ns
Input and output reference level	1.8V
Output load conditions	10pF, 10kΩ, 1TTL
	30pF, 1TTL

* CL includes scope and jig capacitance.

Electrical Characteristics

• DC and operating characteristics

(V_{CC}=5V ± 10%, GND=0V, T_a=0 to +70 °C)

Item	Symbol	Test conditions	Min.	Typ.*	Max.	Unit
Input leakage current	I _{LI}	V _{IN} =GND to V _{CC}	-0.5	—	0.5	μA
Output leakage current	I _{LO}	CE1=V _{IH} or CE2=V _{IL} or OE=V _{IH} or WE=V _{IL} , V _{I/O} =GND to V _{CC}	-0.5	—	0.5	μA
Operating power supply current	I _{CC1}	CE1=V _{IL} , CE2=V _{IH} , I _{OUT} =0mA V _{IN} =V _{IH} or V _{IL}	—	3	10	mA
		CE1 ≤ 0.2V, CE2 ≥ V _{CC} -0.2V V _{IN} ≤ 0.2V or ≥ V _{CC} -0.2V	—	1	5	mA
Average operating current	I _{CC2}	Min. cycle Duty=100% I _{OUT} =0mA	70L	—	60	mA
			10L	—	60	
			12L	—	60	
Standby current	I _{SB1}	CE2 ≤ 0.2V or CE1 ≥ V _{CC} -0.2V CE2 ≥ V _{CC} -0.2V	0 to +70 °C	—	25	μA
			0 to +40 °C	—	5	
			25 °C	0.5	2	
	I _{SB2}	CE1=V _{IH} or CE2=V _{IL}	—	0.4	2	mA
Output high voltage	V _{OH}	I _{OH} =-1.0mA	2.4	—	—	V
Output low voltage	V _{OL}	I _{OL} =2.1mA	—	—	0.4	V

* V_{CC}=5V, T_a=25 °C

I/O capacitance

(T_a=25 °C, f=1MHz)

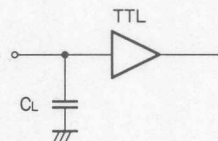
Item	Symbol	Test conditions	Min.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} =0V	—	6	pF
I/O capacitance	C _{I/O}	V _{I/O} =0V	—	8	pF

(Note) This parameter is sampled and is not 100% tested.

AC characteristics

• AC test conditions (V_{CC}=5V ± 10%, T_a=0 to +70 °C)

Item	Conditions
Input pulse high level	V _{IH} =2.2V
Input pulse low level	V _{IL} =0.8V
Input rise time	t _r =5ns
Input fall time	t _f =5ns
Input and output reference level	1.5V
Output load conditions	10L/12L
	70L
	C _L *=100pF, 1TTL
	C _L *=30pF, 1TTL

* C_L includes scope and jig capacitances.

• Read cycle

Item	Symbol	-70L		-10L		-12L		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t _{RC}	70	—	100	—	120	—	ns
Address access time	t _{AA}	—	70	—	100	—	120	ns
Chip enable access time (CE1)	t _{CO1}	—	70	—	100	—	120	ns
Chip enable access time (CE2)	t _{CO2}	—	70	—	100	—	120	ns
Output enable to output valid	t _{OE}	—	35	—	50	—	60	ns
Output hold from address change	t _{OH}	5	—	10	—	10	—	ns
Chip enable to output in low Z (CE1, CE2)	t _{LZ1} , t _{LZ2}	10	—	10	—	10	—	ns
Output enable to output in low Z (OE)	t _{OLZ}	5	—	5	—	5	—	ns
Chip disable to output in high Z (CE1, CE2)	t _{HZ1} , t _{HZ2} *	0	30	0	30	0	30	ns
Chip disable to output in high Z (OE)	t _{OHZ} *	0	30	0	30	0	30	ns

* t_{HZ} and t_{OHZ} are defined as the time at which the outputs become the high impedance state and are not referred to as output voltage levels.

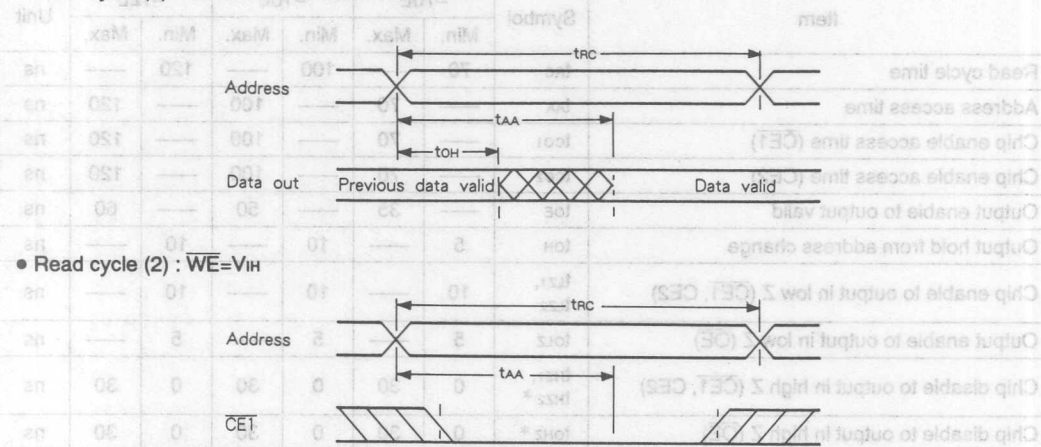
• Write cycle

Item	Symbol	-70L		-10L		-12L		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t _{WC}	70	—	100	—	120	—	ns
Address valid to end of write	t _{AW}	65	—	80	—	100	—	ns
Chip enable to end of write	t _{CW}	65	—	80	—	100	—	ns
Data to write time overlap	t _{DW}	30	—	35	—	40	—	ns
Data hold from write time	t _{DH}	0	—	0	—	0	—	ns
Write pulse width	t _{WP}	50	—	60	—	70	—	ns
Address set up time	t _{AS}	0	—	0	—	0	—	ns
Write recovery time (WE)	t _{WR}	0	—	0	—	0	—	ns
Write recovery time (CE1, CE2)	t _{WR1}	0	—	0	—	0	—	ns
Output active from end of write	t _{OW}	10	—	10	—	10	—	ns
Write to output in high Z	t _{WHZ} *	0	25	0	25	0	25	ns

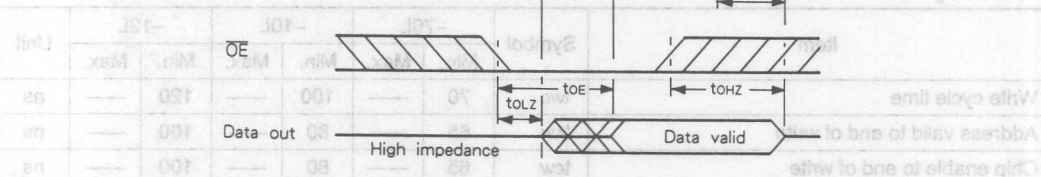
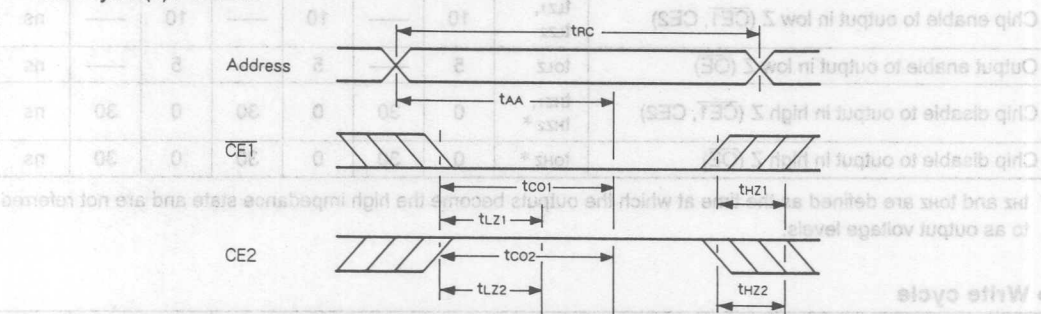
* t_{WHZ} is defined as the time at which the outputs become the high impedance state and are not referred to as output voltage levels.

Timing Waveform

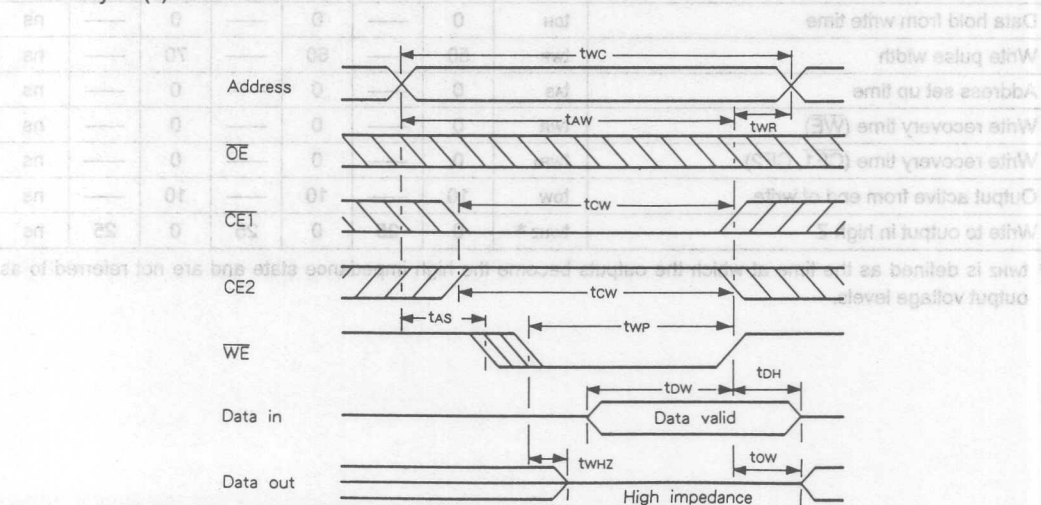
- Read cycle (1) : $\overline{CE1}=\overline{OE}=V_{IL}$, $CE2=V_{IH}$, $\overline{WE}=V_{IH}$



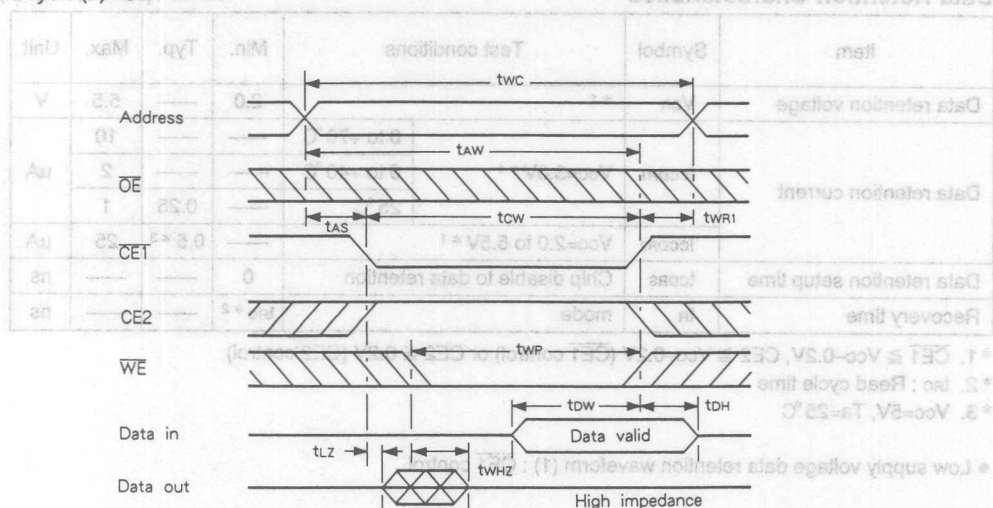
- Read cycle (2) : $\overline{WE}=V_{IH}$



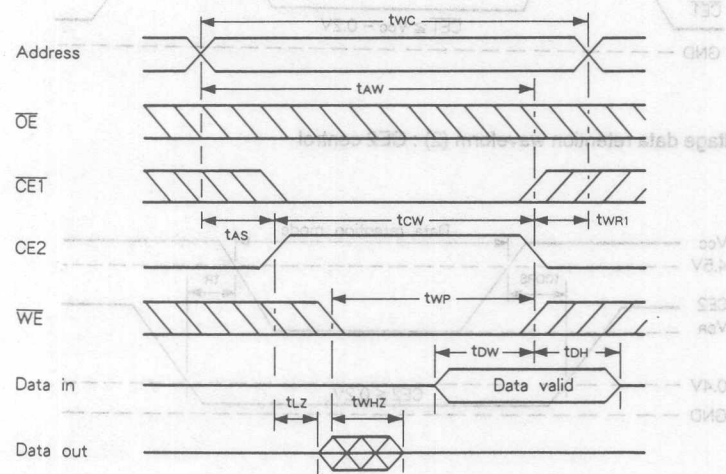
- Write cycle (1) : $\overline{WE}$ control



• Write cycle (2) : $\overline{\text{CE1}}$ control



• Write cycle (3) : CE2 control

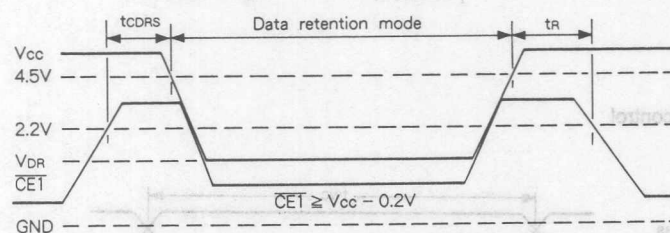
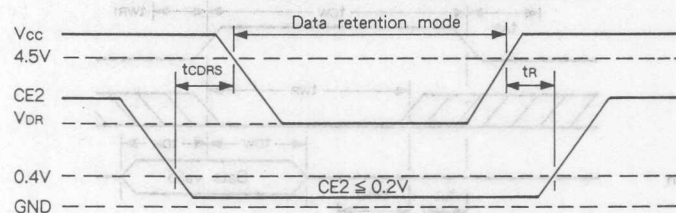


* During I/O pins are in the output state, the data input signals of opposite phase to the output must not be applied.

Data Retention Characteristics

(Ta=0 to +70°C)

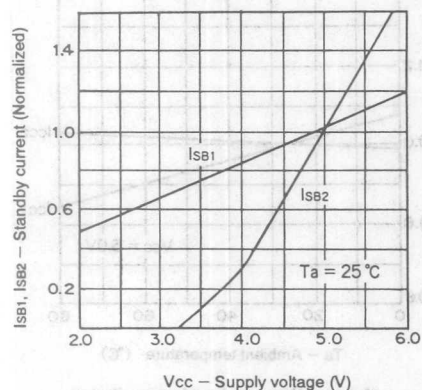
Item	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Data retention voltage	V _{DR}	*1	2.0	—	5.5	V
Data retention current	I _{CCDR1}	V _{CC} =3.0V *1	0 to +70°C	—	10	μA
			0 to +40°C	—	2	
			25°C	—	0.25	
	I _{CCDR2}	V _{CC} =2.0 to 5.5V *1	—	0.5 *3	25	μA
Data retention setup time	t _{CDRS}	Chip disable to data retention	0	—	—	ns
Recovery time	t _r	mode	t _{rc} *2	—	—	ns

*1. $\overline{\text{CE1}} \geq V_{\text{CC}} - 0.2\text{V}$, $\text{CE2} \geq V_{\text{CC}} - 0.2\text{V}$ ($\overline{\text{CE1}}$ control) or $\text{CE2} \leq 0.2\text{V}$ (CE2 control)*2. t_{rc} : Read cycle time*3. V_{CC}=5V, Ta=25°C• Low supply voltage data retention waveform (1) : $\overline{\text{CE1}}$ control• Low supply voltage data retention waveform (2) : CE2 control

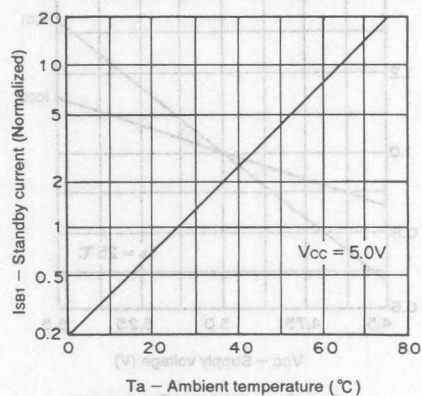
* During I/O pins are in the output state, the data input signals of opposite phase to the output must not be applied.

Example of Representative Characteristics

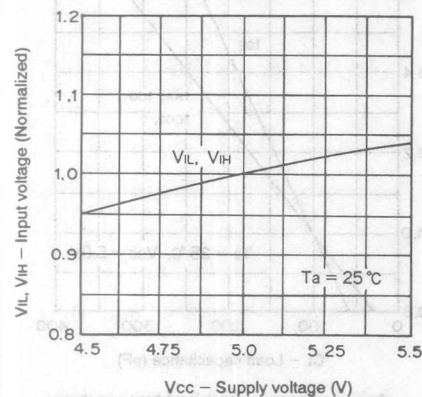
Standby current vs. Supply voltage



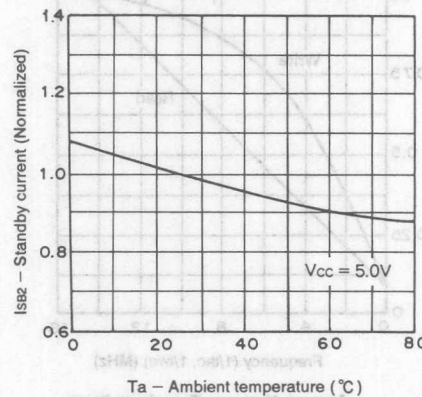
Standby current vs. Ambient temperature



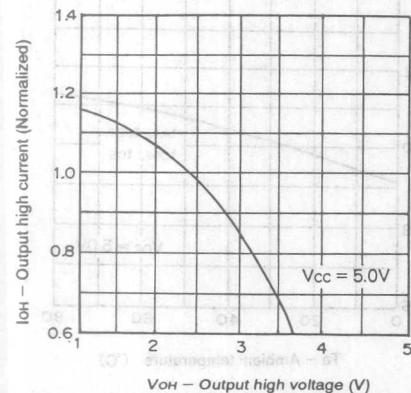
Input voltage level vs. Supply voltage



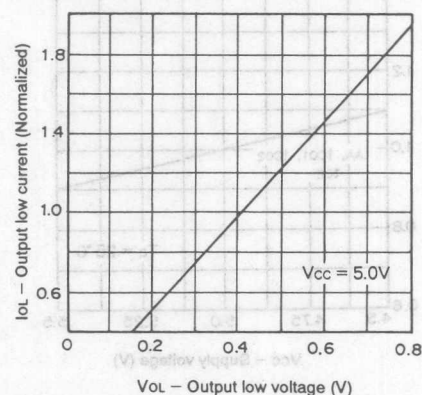
Standby current vs. Ambient temperature



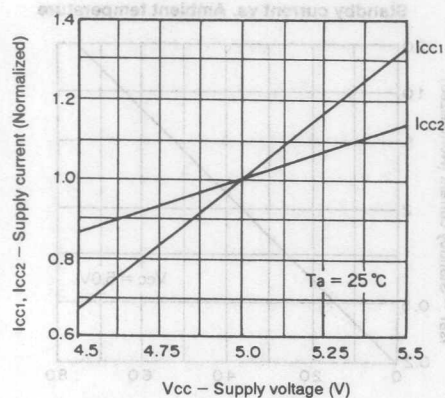
Output high current vs. Output high voltage



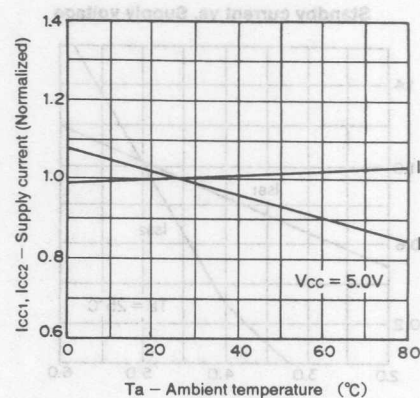
Output low current vs. Output low voltage



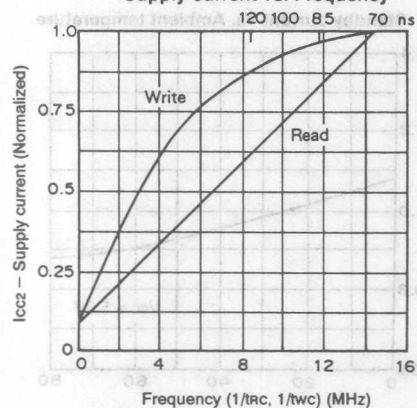
Supply current vs. Supply voltage



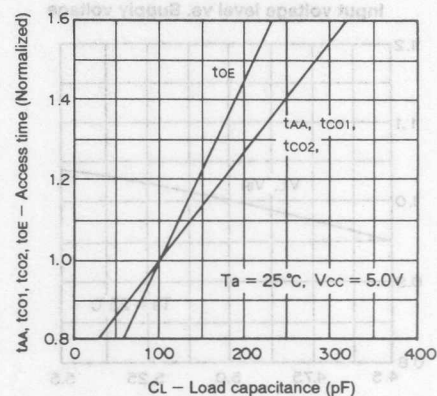
Supply current vs. Ambient temperature



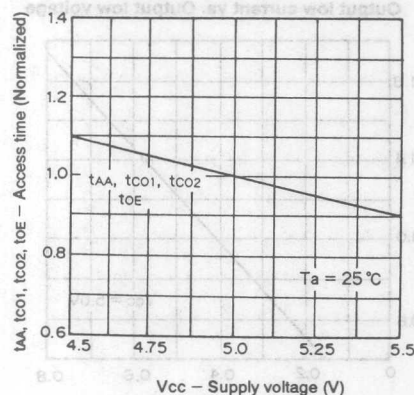
Supply current vs. Frequency



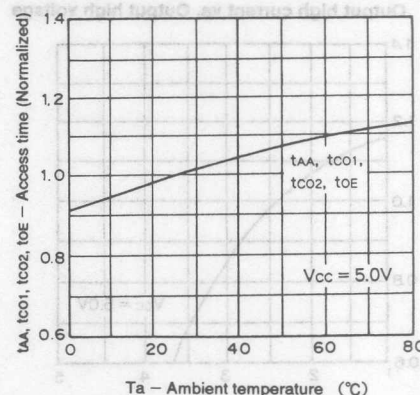
Access time vs. Load capacitance



Access time vs. Supply voltage

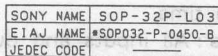


Access time vs. Ambient temperature

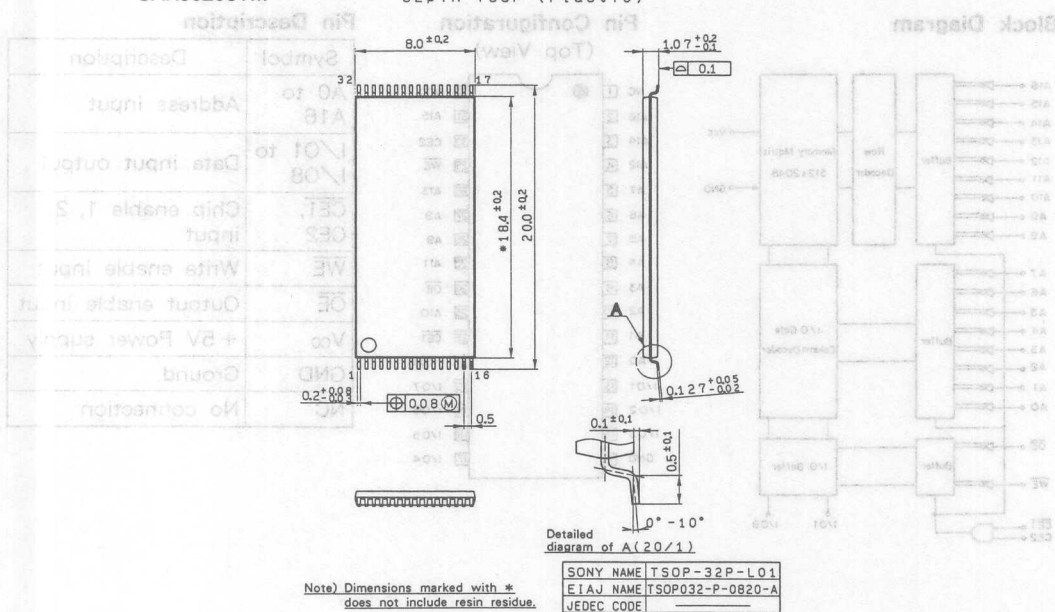


Unit : mm

32pin SOP (Plastic) 450mil



32pin TSOP (Plastic)



SONY®

CXK581020SP/J -35/45/55

131072-word × 8-bit High Speed CMOS Static RAM

Description

CXK581020SP/J are 131,072-word × 8-bit high speed CMOS static RAMs suitable for use in high speed and low power applications.

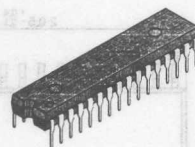
Organized as 131,072 words by 8 bits, it operates from a single 5V supply.

Features

- Fast access time : (Access time)
CXK581020SP/J-35 35ns (Max.)
CXK581020SP/J-45 45ns (Max.)
CXK581020SP/J-55 55ns (Max.)
- Low power operation : (Operation)
CXK581020SP/J-35, 45, 55
300mW(Typ, Cycle = Min.)
- Single +5V supply : +5V ± 10 %
- Fully static memory ... No clock or timing strobe required.
- Equal access and cycle time.
- Directly TTL compatible : All inputs and outputs.
- Available in 32 pin 400-mil DIP and 400-mil SOJ

CXK581020SP
32 pin DIP (Plastic)

CXK581020J
32 pin SOJ (Plastic)



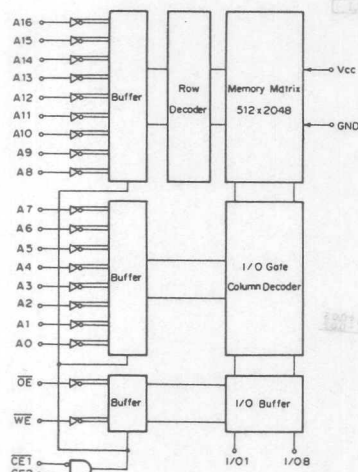
Function

131,072-word × 8-bit static RAM

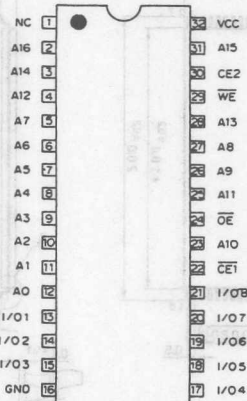
Structure

Silicon gate CMOS IC

Block Diagram



Pin Configuration (Top View)



Pin Description

Symbol	Description
A0 to A16	Address input
I/O1 to I/O8	Data input output
CE1, CE2	Chip enable 1, 2 input
WE	Write enable input
OE	Output enable input
Vcc	+ 5V Power supply
GND	Ground
NC	No connection

Absolute Maximum Ratings

(Ta = 25 °C, GND = 0V)

Item	Symbol	Rating	Unit
Supply voltage	V _{CC}	- 0.5 * to + 7.0	V
Input voltage	V _{IN}	- 0.5 * to V _{CC} + 0.5	V
Input and output voltage	V _{I/O}	- 0.5 * to V _{CC} + 0.5	V
Allowable power dissipation	P _D	1.0	W
Operating temperature	T _{opr}	0 to + 70	°C
Storage temperature	T _{stg}	- 55 to + 150	°C
Soldering temperature • time	T _{solder}	260 • 10	°C • sec

* **Note)** V_{CC}, V_{IN}, V_{I/O} = - 3.5V Min. for pulse width less than 20ns.

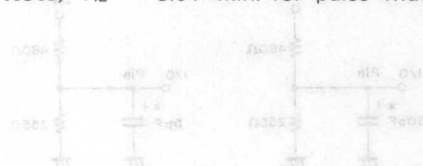
Truth Table

CE1	CE2	OE	WE	Mode	I/O1 to I/O8	V _{CC} current
H	X	X	X	Not selected	High Z	I _{SB1} , I _{SB2}
X	L	X	X	Not selected	High Z	I _{SB1} , I _{SB2}
L	H	H	H	Output disable	High Z	I _{CC2}
L	H	L	H	Read	Data out	I _{CC2}
L	H	X	L	Write	Data in	I _{CC2}

Note) X : "H" or "L"

DC Recommended Operating Conditions (Ta = 0 to + 70 °C, GND = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Input high voltage	V _{IH}	2.2	—	V _{CC} + 0.3	V
Input low voltage	V _{IL}	- 0.3 *	—	0.8	V

* **Note)** V_{IL} = - 3.0V Min. for pulse width less than 20ns.

*1. CL includes scope and its capacitance.
 *2. For first rise time test, use two pins.

Fig. 1

Electrical Characteristics

DC and operating characteristics

(V_{CC} = 5V ± 10%, GND = 0V, T_a = 0 to +70°C)

Item	Symbol	Test conditions	Min.	Typ.*	Max.	Unit
Input leakage current	I _{LI}	V _{IN} = GND to V _{CC}	-2	—	2	μA
Output leakage current	I _{LO}	V _{I/O} = GND to V _{CC} , $\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$	-2	—	2	μA
Operating power supply current	I _{CC1}	$\overline{CE1} = V_{IL}$, $CE2 = V_{IH}$, V _{IN} = V _{IH} or V _{IL} , I _{OUT} = 0mA	—	—	—	mA
Average operating current	I _{CC2}	Cycle = Min., Duty = 100%, I _{OUT} = 0mA	—	60	120	mA
Standby current	I _{SB1}	$\overline{CE1} \geq V_{CC} - 0.2V$ or $CE2 \leq 0.2V$, V _{IN} $\geq V_{CC} - 0.2V$ or V _{IN} $\leq 0.2V$	—	0.01	2	mA
	I _{SB2}	$\overline{CE1} = V_{IH}$ or $CE2 = V_{IL}$, Cycle = Min.	—	5	35	mA
Output high voltage	V _{OH}	I _{OH} = -4.0mA	2.4	—	—	V
Output low voltage	V _{OL}	I _{OL} = 8.0mA	—	—	0.4	V

* Note) V_{CC} = 5V, T_a = 25°C

I/O capacitance

(T_a = 25°C, f = 1MHz)

Item	Symbol	Test Conditions	Min.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} = 0V	—	7	pF
I/O capacitance	C _{I/O}	V _{I/O} = 0V	—	7	pF

Note) This parameter is sampled and is not 100% tested.

AC characteristics

• AC test conditions (V_{CC} = 5V ± 10%, T_a = 0 to +70°C)

Item	Conditions
Input pulse high level	V _{IH} = 3.0V
Input pulse low level	V _{IL} = 0V
Input rise time	t _r = 5ns
Input fall time	t _f = 5ns
Input and output reference level	1.5V
Output load	Fig. 1

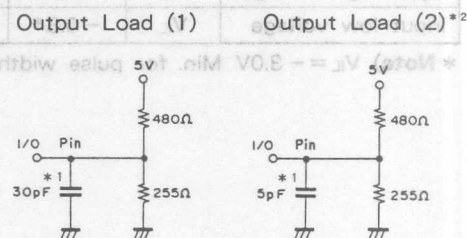
*1. C_L includes scope and jig capacitances.*2. For t_{LZ1}, t_{LZ2}, t_{OLZ}, t_{HZ1}, t_{HZ2}, t_{OHZ}, t_{OW}, t_{WHZ}

Fig. 1

• Read cycle

Item	Symbol	-35		-45		-55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t _{RC}	35	—	45	—	55	—	ns
Address access time	t _{AA}	—	35	—	45	—	55	ns
Chip enable access time ($\overline{\text{CE1}}$)	t _{CO1}	—	35	—	45	—	55	ns
Chip enable access time (CE2)	t _{CO2}	—	35	—	45	—	55	ns
Output enable to output valid	t _{OE}	—	20	—	25	—	30	ns
Output hold from address change	t _{OH}	5	—	5	—	5	—	ns
Chip enable to output in low Z ($\overline{\text{CE1}}$, CE2)	t _{LLZ1} *, t _{LLZ2} *	5	—	5	—	5	—	ns
Output enable to output in low Z ($\overline{\text{OE}}$)	t _{OLZ} *	0	—	0	—	0	—	ns
Chip disable to output in high Z ($\overline{\text{CE1}}$, CE2)	t _{HZ1} *, t _{HZ2} *	0	15	0	20	0	25	ns
Chip disable to output in high Z ($\overline{\text{OE}}$)	t _{OHZ} *	0	15	0	20	0	25	ns
Chip enable to power up time ($\overline{\text{CE1}}$, CE2)	t _{PU}	0	—	0	—	0	—	ns
Chip enable to power down time ($\overline{\text{CE1}}$, CE2)	t _{PD}	—	35	—	45	—	55	ns

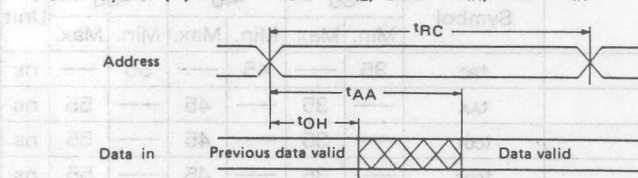
• Write cycle

Item	Symbol	-35		-45		-55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t _{WC}	35	—	45	—	55	—	ns
Address valid to end of write	t _{AW}	30	—	40	—	45	—	ns
Chip enable to end of write	t _{CW}	30	—	40	—	45	—	ns
Data to write time overlap	t _{DW}	18	—	20	—	25	—	ns
Data hold from write time	t _{DH}	0	—	0	—	0	—	ns
Write pulse width	t _{WP}	30	—	35	—	40	—	ns
Address set up time	t _{AS}	0	—	0	—	0	—	ns
Write recovery time ($\overline{\text{WE}}$, $\overline{\text{CE1}}$)	t _{WR1}	3	—	3	—	3	—	ns
Write recovery time (CE2)	t _{WR2}	5	—	5	—	5	—	ns
Output active from end of write	t _{OW} *	5	—	5	—	5	—	ns
Write to output in high Z	t _{WHZ} *	0	15	0	15	0	15	ns

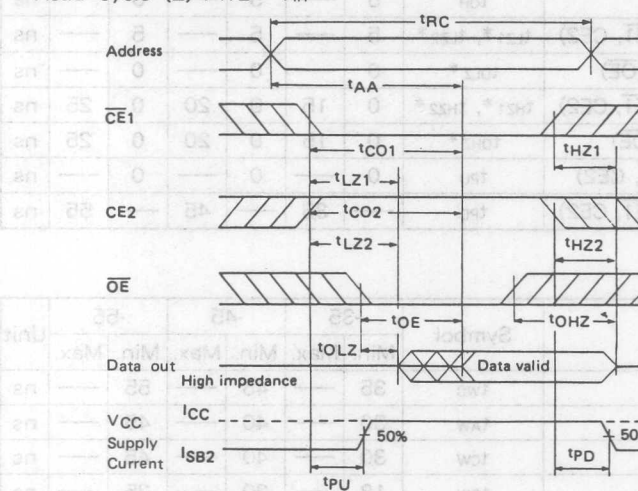
* Transition is measured $\pm 500\text{mV}$ from steady voltage with specified loading in Fig. 1 (2). This parameter is sampled and not 100% tested.

Timing Waveform

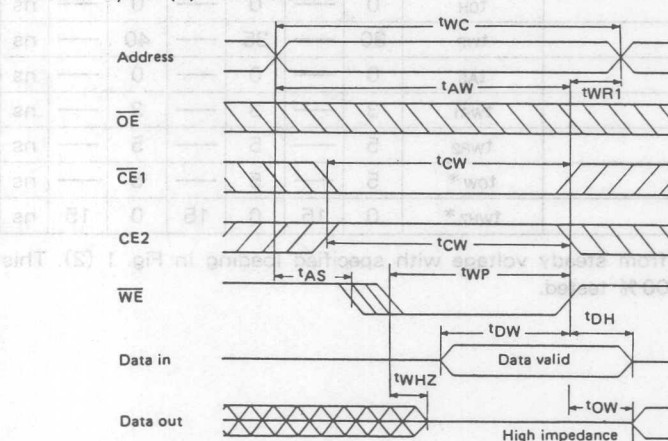
- Read cycle (1) : $\overline{CE1} = \overline{OE} = V_{IL}$, $CE2 = V_{IH}$, $\overline{WE} = V_{IH}$



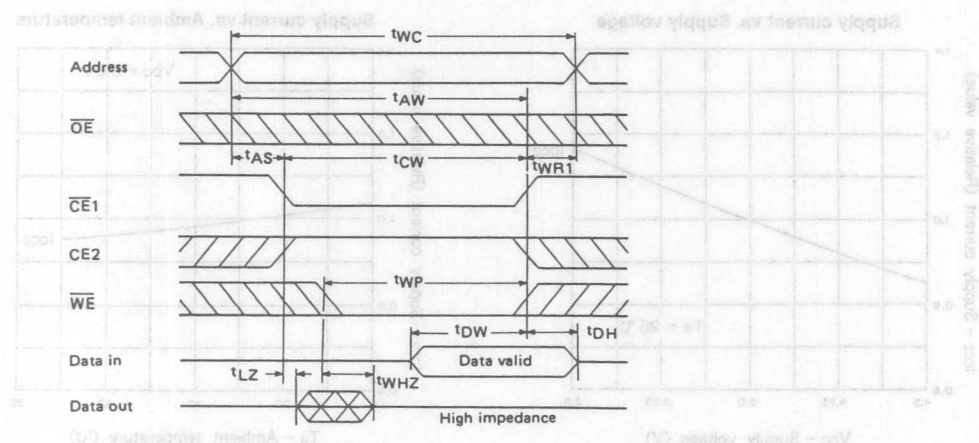
- Read cycle (2) : $\overline{WE} = V_{IH}$



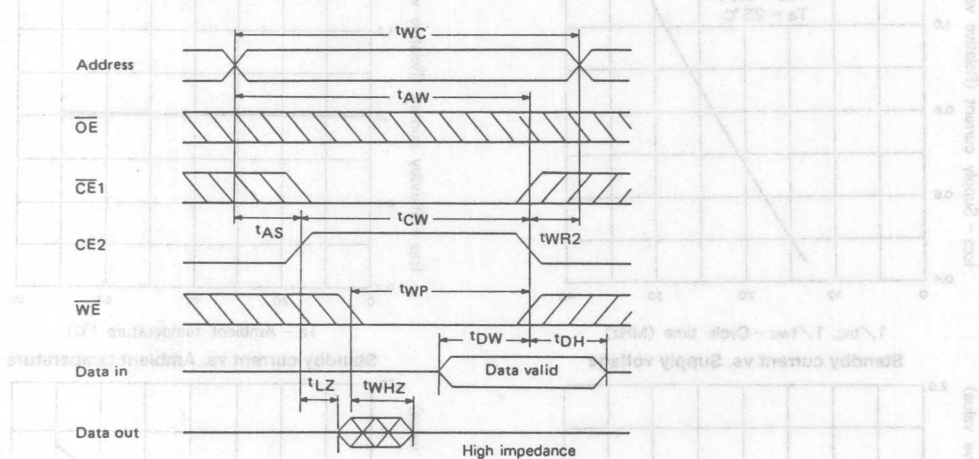
- Write cycle (1) : $\overline{WE}$ control



• Write cycle (2) : $\overline{\text{CE1}}$ control



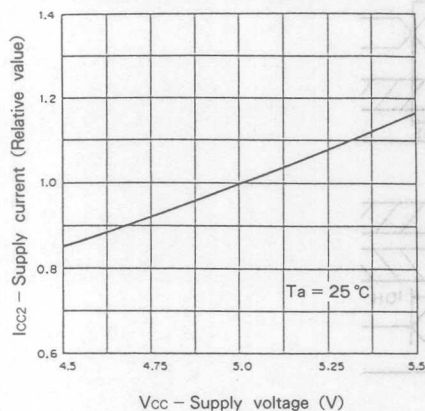
• Write cycle (3) : CE2 control



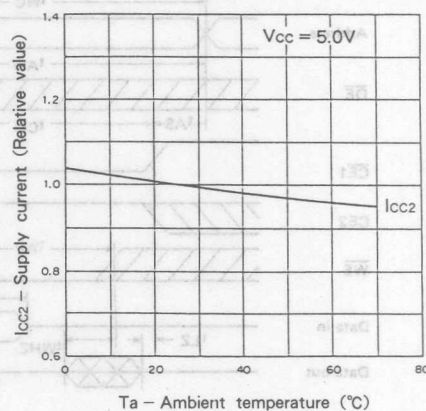
Note) During I/O pins are in the output state, the data input signals of opposite phase to the output must not be applied.

Example of Representative Characteristics

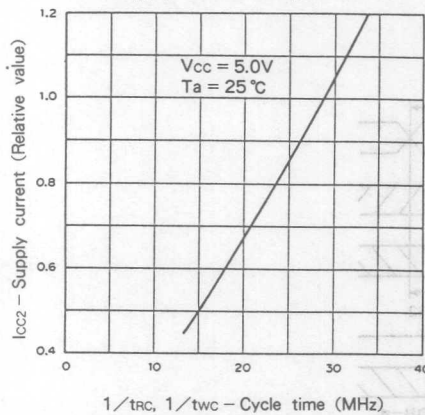
Supply current vs. Supply voltage



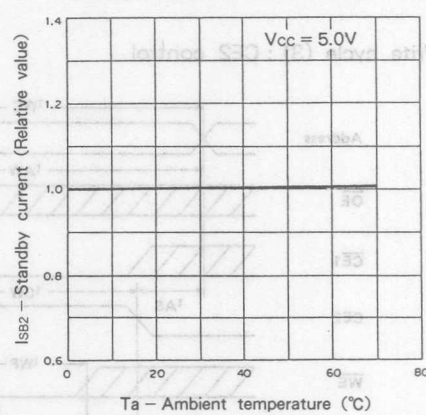
Supply current vs. Ambient temperature



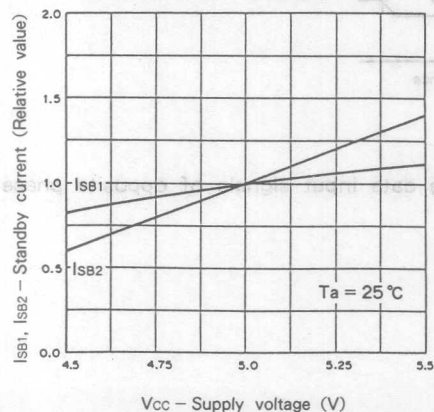
Supply current vs. Cycle time



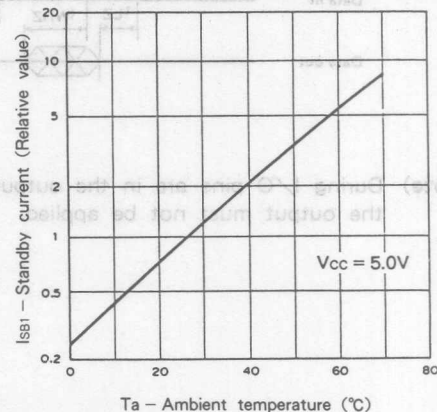
Standby current vs. Ambient temperature



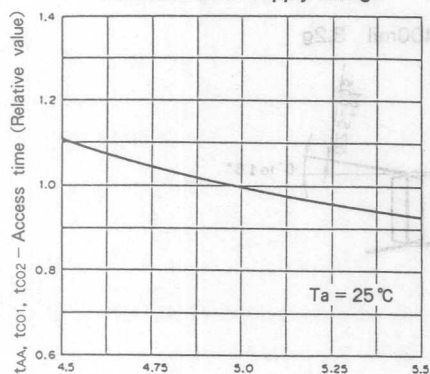
Standby current vs. Supply voltage



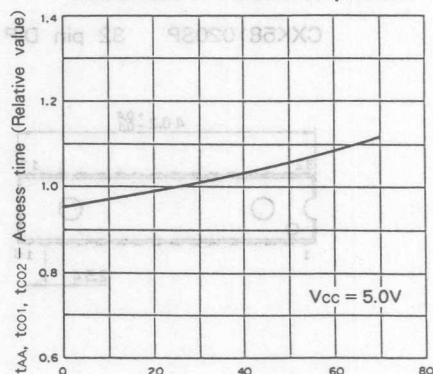
Standby current vs. Ambient temperature



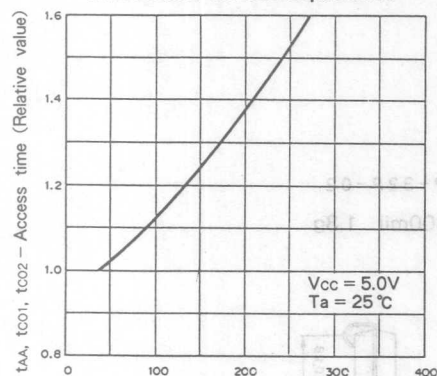
Access time vs. Supply voltage



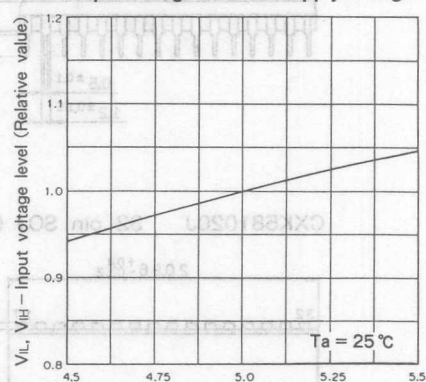
Access time vs. Ambient temperature

V_{CC} - Supply voltage (V)T_a - Ambient temperature (°C)

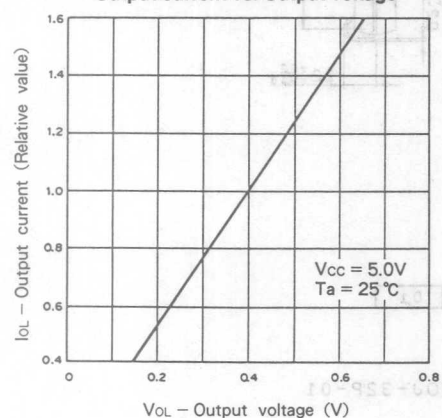
Access time vs. Load capacitance



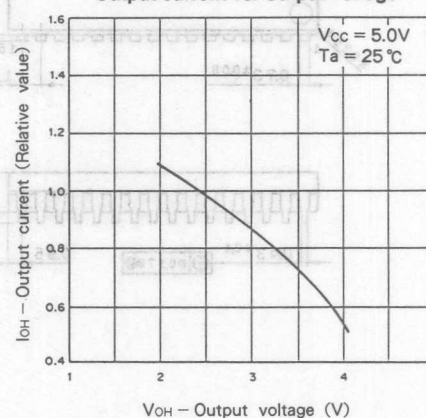
Input voltage level vs. Supply voltage

C_L - Load capacitance (pF)V_{CC} - Supply voltage (V)

Output current vs. Output voltage

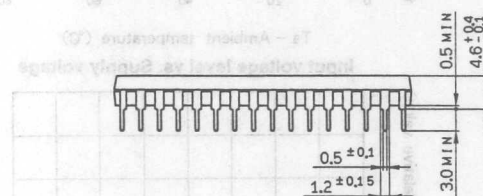
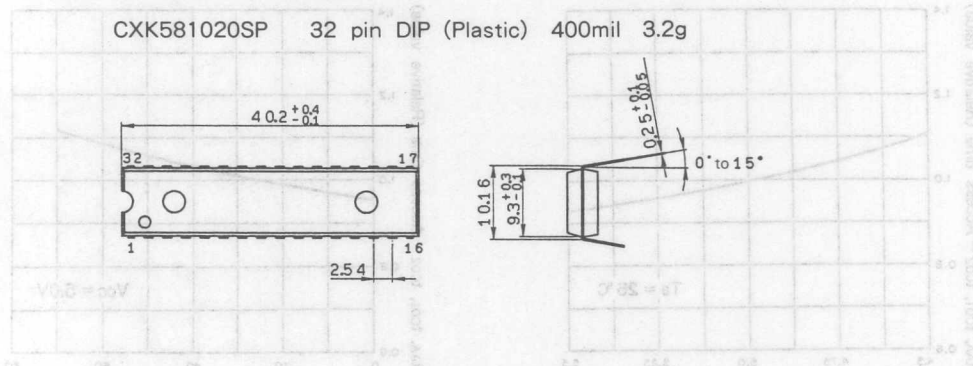


Output current vs. Output voltage



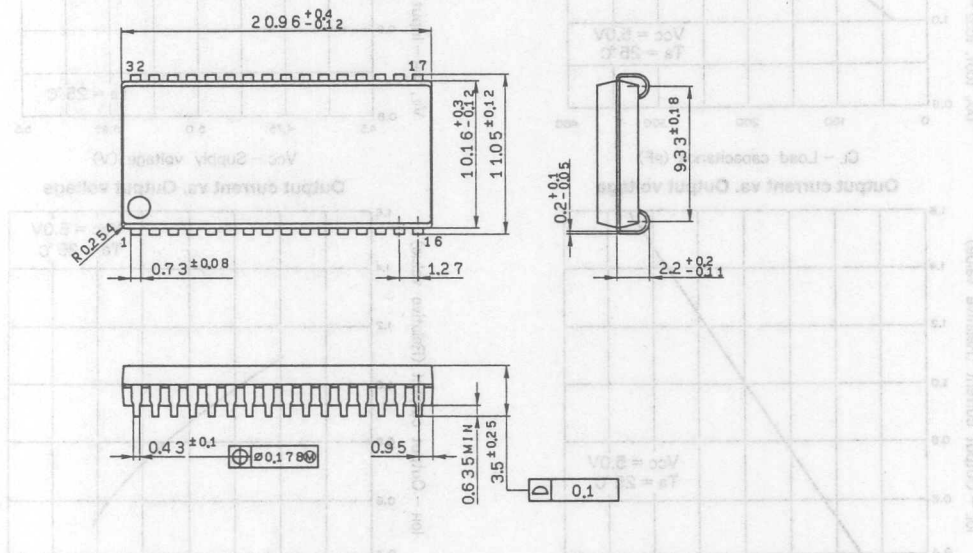
Package Outline Unit : mm

CXK581020SP 32 pin DIP (Plastic) 400mil 3.2g



DIP-32P-02

CXK581020J 32 pin SOJ (Plastic) 400mil 1.3g



SOJ-32P-01

SONY

CXK581001P/M -70L/85L 70LL/85LL

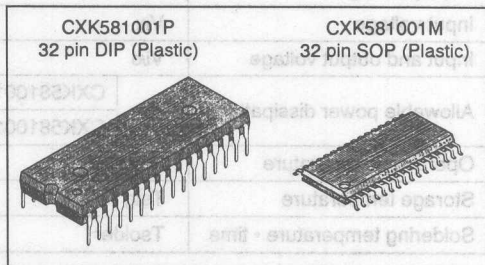
131,072-word × 8-bit High Speed CMOS Static RAM

Description

CXK581001P/M is a 1,048,576 bits high speed CMOS static RAMs organized as 131,072 words by 8-bit and operates from a single 5V supply. This IC is suitable for use in high speed and low power applications in which battery back up for nonvolatility is required.

Features

- Fast access time: (Access time)
CXK581001P/M-70L/70LL 70ns (Max.)
CXK581001P/M-85L/85LL 85ns (Max.)
- Low power operation :
CXK581001P/M Standby/Operation
-70L/85L : 10 μ W (Typ.)/237.5mW (Typ., Cycle=Min.)
-70LL/85LL : 3.5 μ W (Typ.)/237.5mW (Typ., Cycle=Min.)
- Single + 5V supply : +5V $\pm$ 10%
- Fully static memory... No clock or timing strobe required.
- Equal access and cycle time.
- Common data input and output : three state output.
- Directly TTL compatible : All inputs and outputs.
- Low voltage data retention : 2.0V (Min.)
- CXK581001P 600mil 32 pin DIP package
- CXK581001M 525mil 32 pin SOP package



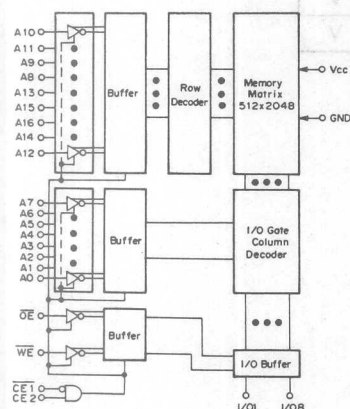
Function

131,072-word × 8-bit static RAM

Structure

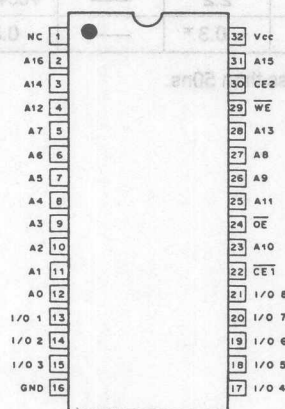
Silicon gate CMOS IC

Block diagram



Pin Configuration

(Top View)



Pin Description

Symbol	Description
A ₀ to A ₁₆	Address input
I/O ₁ to I/O ₈	Data input/output
CE ₁ , CE ₂	Chip enable 1, 2 input
WE	Write enable input
OE	Output enable input
V _{CC}	+5V power supply
GND	Ground
NC	No connection

Sony reserves the right to change products and specifications without prior notice. This information does not convey any license by any implication or otherwise under any patents or other right. Application circuits shown, if any, are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits.

Absolute Maximum Ratings (Ta=25°C, GND=0V)

Item	Symbol	Rating	Unit
Supply voltage	V _{CC}	- 0.5 to +7.0	V
Input voltage	V _{IN}	- 0.5 * to V _{CC} +0.5	V
Input and output voltage	V _{I/O}	- 0.5 * to V _{CC} +0.5	V
Allowable power dissipation	P _D	CXK581001P	1.0
		CXK581001M	0.7
Operating temperature	T _{opr}	0 to +70	°C
Storage temperature	T _{stg}	- 55 to +150	°C
Soldering temperature • time	T _{solder}	260 • 10	°C • sec

* V_{IN}, V_{I/O} = - 3.0V Min. for pulse width less than 50ns.**Truth Table**

CE1	CE2	OE	WE	Mode	I/O1 to I/O8	V _{CC} Current
H	X	X	X	Not selected	High Z	I _{SB1} , I _{SB2}
X	L	X	X	Not selected	High Z	I _{SB1} , I _{SB2}
L	H	H	H	Output disable	High Z	I _{CC}
L	H	L	H	Read	Data out	I _{CC}
L	H	X	L	Write	Data in	I _{CC}

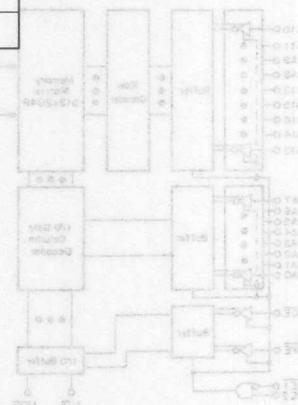
X : "H" or "L"

DC Recommended Operating Conditions (Ta=0 to +70°C, GND=0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Input high voltage	V _{IH}	2.2	—	V _{CC} +0.3	V
Input low voltage	V _{IL}	- 0.3 *	—	0.8	V

* V_{IL} = - 3.0V Min. for pulse width less than 50ns.

CE1	Chip enable 1
CE2	Chip enable 2
OE	Output enable
WE	Write enable
V _{CC}	+5V power supply
GND	Ground
NC	No connection



Electrical Characteristics

• DC and operating characteristics

(V_{CC}=5V ± 10%, GND=0V, T_a=0 to +70 °C)

Item	Symbol	Test conditions	- 70L/85L			- 70LL/85LL			Unit
			Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Input leakage current	I _{LI}	V _{IN} =GND to V _{CC}	-1	—	1	-1	—	1	μA
Output leakage current	I _{LO}	CE1=V _{IH} or CE2=V _{IL} or OE=V _{IH} or WE=V _{IL} V _{I/O} =GND to V _{CC}	-1	—	1	-1	—	1	μA
Average operating current	I _{CC}	Cycle=Min, Duty=100% I _{OUT} =0mA	—	47.5	80	—	47.5	80	mA
Standby current	I _{SB1}	CE2 ≤ 0.2V or CE1 ≥ V _{CC} - 0.2V CE2 ≥ V _{CC} - 0.2V	0 to 70 °C	—	100	—	—	20	μA
			0 to 40 °C	—	20	—	—	4	
			+25 °C	—	2	—	0.7	2	
	I _{SB2}	CE1=V _{IH} or CE2=V _{IL}	—	1.2	3	—	1.2	3	mA
Output high voltage	V _{OH}	I _{OH} = -1.0mA	2.4	—	—	2.4	—	—	V
Output low voltage	V _{OL}	I _{OL} =2.1mA	—	—	0.4	—	—	0.4	V

* V_{CC}=5V, T_a=25 °C

I/O capacitance

(T_a=25 °C, f=1MHz)

Item	Symbol	Test conditions	Min.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} =0V	—	6	pF
I/O capacitance	C _{I/O}	V _{I/O} =0V	—	8	pF

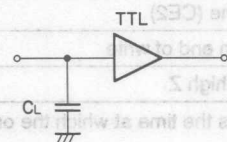
Note) This parameter is sampled and is not 100% tested.

AC characteristics

• AC test conditions

(V_{CC}=5V ± 10%, T_a=0 to +70 °C)

Item	Conditions
Input pulse high level	V _{IH} =2.2V
Input pulse low level	V _{IL} =0.8V
Input rise time	t _r =5ns
Input fall time	t _f =5ns
Input and output reference level	1.5V
Output load conditions	C _L * =100pF, 1TTL

* C_L includes scope and jig capacitances.

• Read cycle ($\overline{WE}$ ="H")

Item	Symbol	- 70L/70LL		- 85L/85LL		Unit
		Min.	Max.	Min.	Max.	
Read cycle time	t _{RC}	70	—	85	—	ns
Address access time	t _{AA}	—	70	—	85	ns
Chip enable access time ($\overline{CE1}$)	t _{CO1}	—	70	—	85	ns
Chip enable access time (CE2)	t _{CO2}	—	70	—	85	ns
Output enable to output valid	t _{OE}	—	40	—	45	ns
Output hold from address change	t _{OH}	10	—	10	—	ns
Chip enable to output in low Z ($\overline{CE1}$, CE2)	t _{lZ1} , t _{lZ2}	10	—	10	—	ns
Output enable to output in low Z ($\overline{OE}$)	t _{OLZ}	5	—	5	—	ns
Chip disable to output in high Z ($\overline{CE1}$, CE2)	t _{hZ1} , t _{hZ2} *	—	25	—	25	ns
Chip disable to output in high Z ($\overline{OE}$)	t _{OHZ} *	—	25	—	25	ns

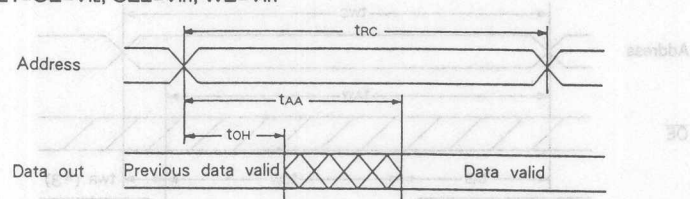
* t_{hZ1}, t_{hZ2} and t_{OHZ} are defined as the time at which the outputs become the high impedance state and are not referred to output voltage levels.

• Write cycle

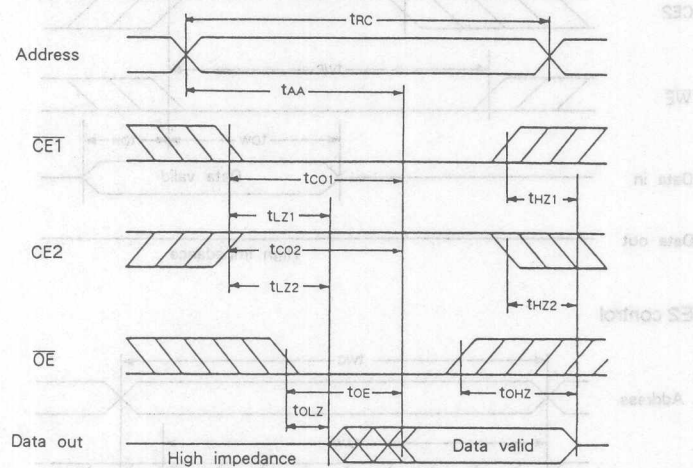
Item	Symbol	- 70L/70LL		- 85L/85LL		Unit
		Min.	Max.	Min.	Max.	
Write cycle time	t _{WC}	70	—	85	—	ns
Address valid to end of write	t _{AW}	60	—	75	—	ns
Chip enable to end of write	t _{CW}	60	—	75	—	ns
Data to write time overlap	t _{DW}	25	—	30	—	ns
Data hold from write time	t _{DH}	0	—	0	—	ns
Write pulse width	t _{WP}	50	—	60	—	ns
Address set up time	t _{AS}	0	—	0	—	ns
Write recovery time ($\overline{WE}$, $\overline{CE1}$)	t _{WR}	5	—	5	—	ns
Write recovery time (CE2)	t _{WR1}	10	—	10	—	ns
Output active from end of write	t _{OW}	5	—	5	—	ns
Write to output in high Z	t _{WHZ} *	—	25	—	30	ns

* t_{WHZ} is defined as the time at which the outputs become the high impedance state and are not referred to output voltage levels.

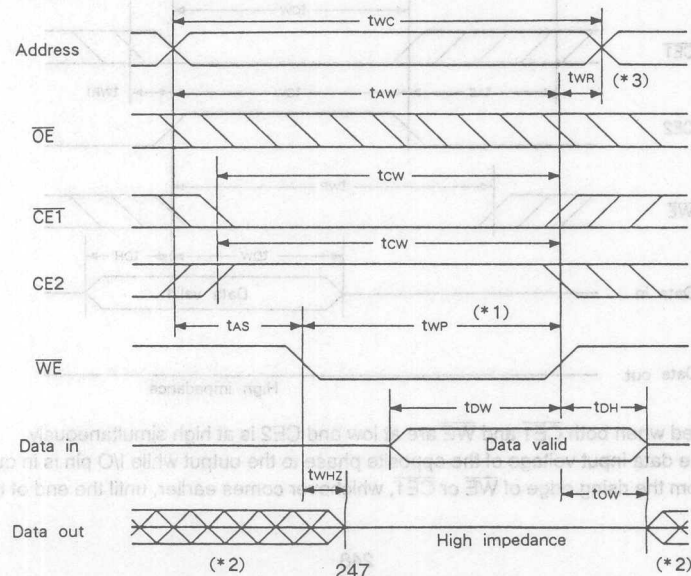
• Read cycle (1): $\overline{CE1}=\overline{OE}=V_{IL}$, $\overline{CE2}=V_{IH}$, $\overline{WE}=V_{IH}$



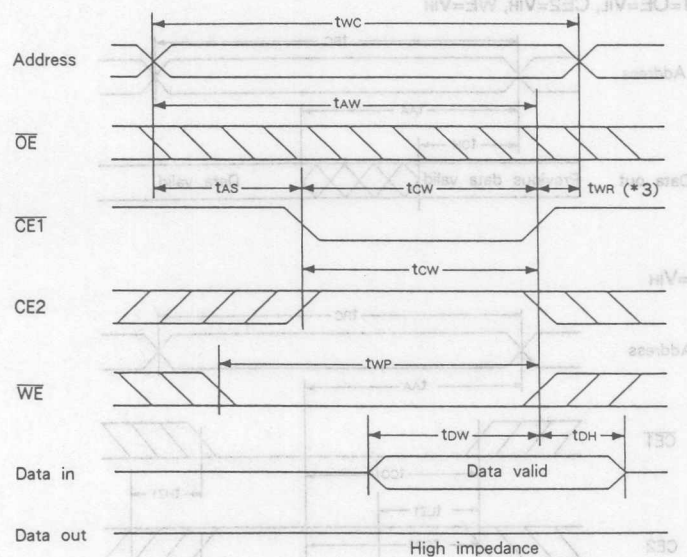
• Read cycle (2): $\overline{WE}=V_{IH}$



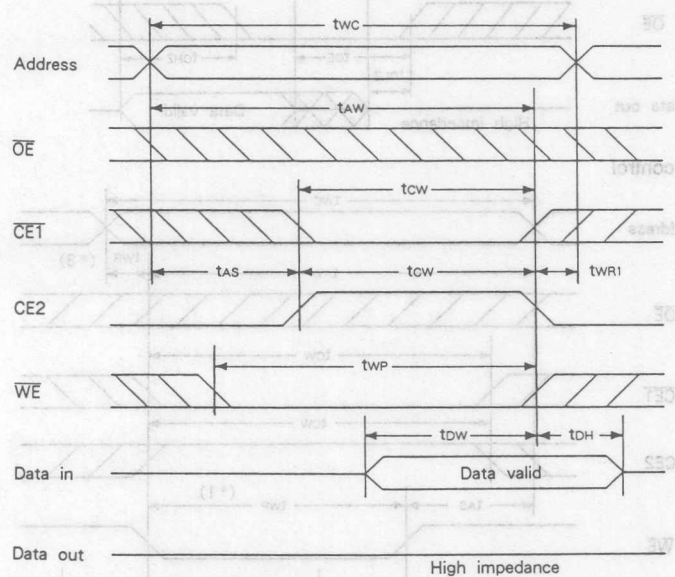
• Write cycle (1): $\overline{WE}$ control



• Write cycle (2): $\overline{CE1}$ control



• Write cycle (3): $\overline{CE2}$ control



- * 1. Write is executed when both $\overline{CE1}$ and $\overline{WE}$ are at low and $\overline{CE2}$ is at high simultaneously.
- * 2. Do not apply the data input voltage of the opposite phase to the output while I/O pin is in output condition.
- * 3. t_{WH} is tested from the rising edge of $\overline{WE}$ or $\overline{CE1}$, whichever comes earlier, until the end of the write cycle.

Data Retention Characteristics

(Ta=0 to 70 °C)

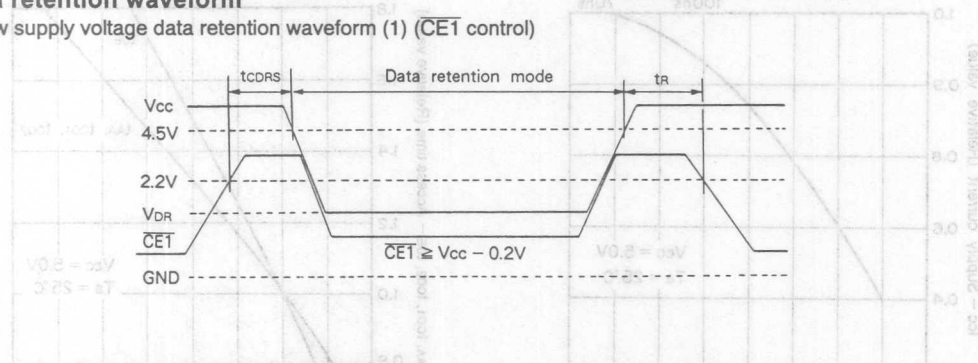
Item	Symbol	Test conditions	-70L/85L			-70LL/85LL			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Data retention voltage	V _{DR}	*1	2.0	—	5.5	2.0	—	5.5	V
Data retention current	I _{CCDR1}	V _{CC} =0.3V *1	0 to 70 °C	—	50	—	—	12	μA
			0 to 40 °C	—	10	—	—	2.4	
			+25 °C	—	1	—	0.4	1.2	
	I _{CCDR2}	V _{CC} =2.0 to 5.5V *1	—	2	100	—	0.7	20	μA
Data retention setup time	t _{CDRS}	Chip disable to data retention mode	0	—	—	0	—	—	ns
Recovery time	t _R		t _{RC} *2	—	—	t _{RC} *2	—	—	ns

*1. $\overline{\text{CE1}} \geq V_{\text{CC}} - 0.2\text{V}$, $\text{CE2} \geq V_{\text{CC}} - 0.2\text{V}$ ($\overline{\text{CE1}}$ control) or $\text{CE2} \leq 0.2\text{V}$ (CE2 control)

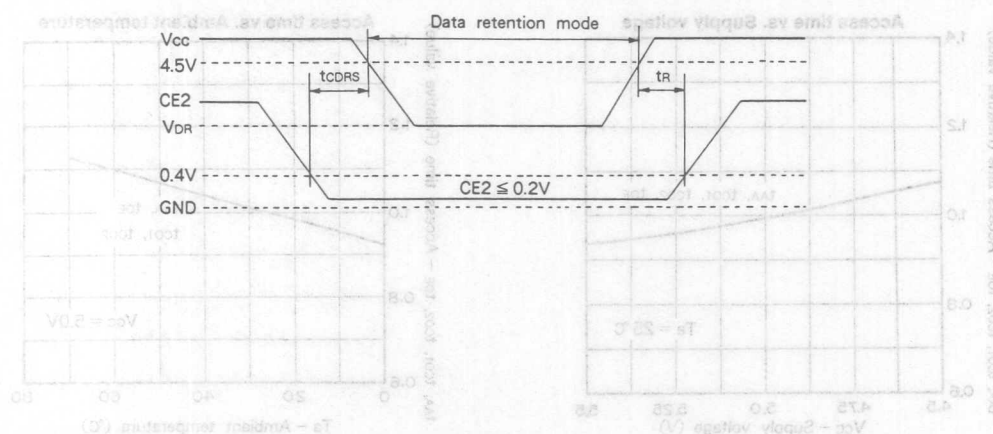
*2. t_{RC} : Read cycle time

Data retention waveform

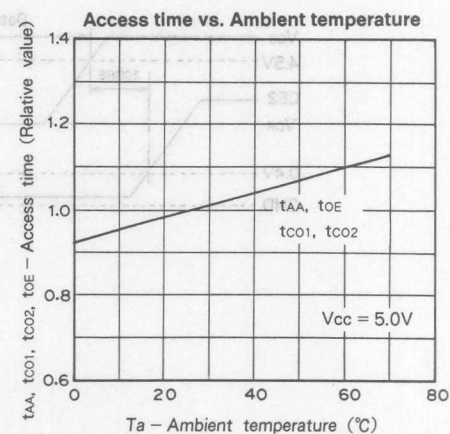
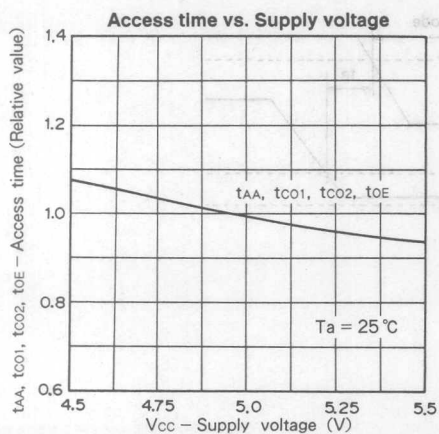
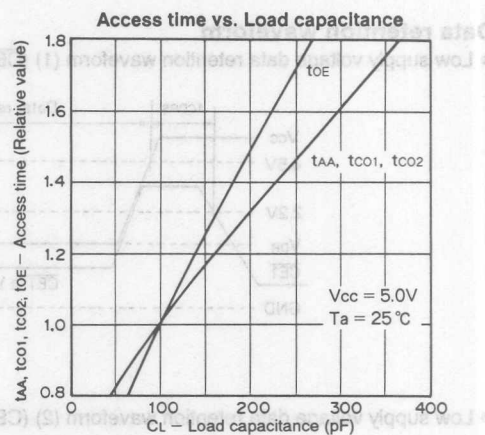
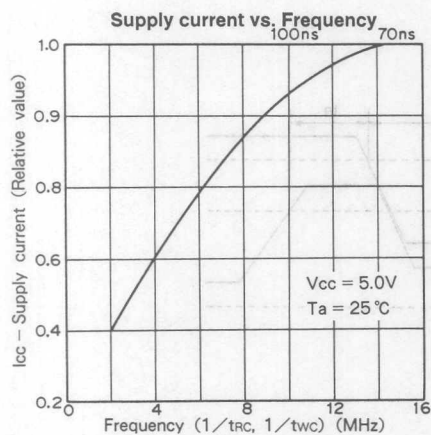
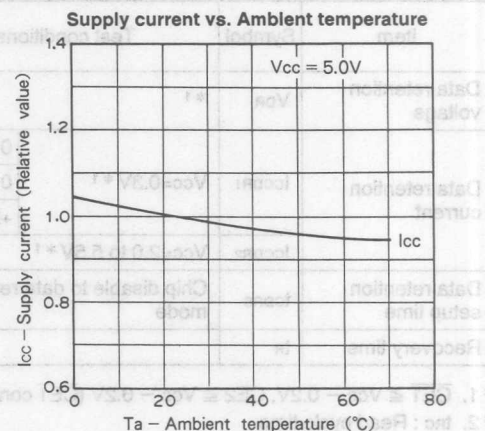
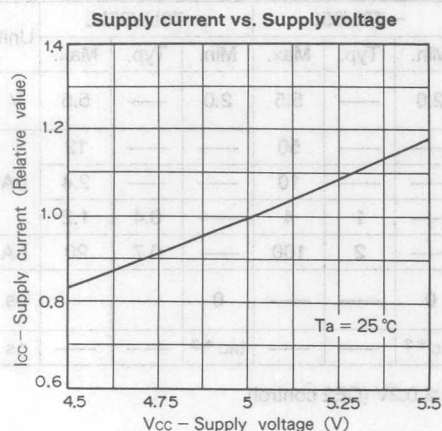
- Low supply voltage data retention waveform (1) ($\overline{\text{CE1}}$ control)



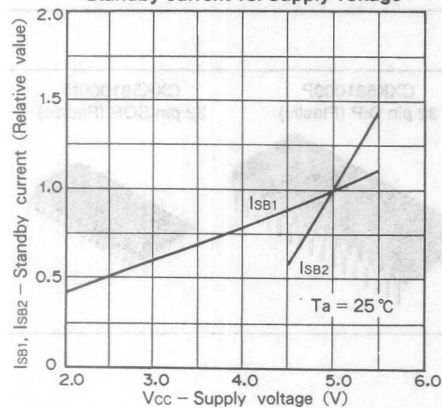
- Low supply voltage data retention waveform (2) (CE2 control)



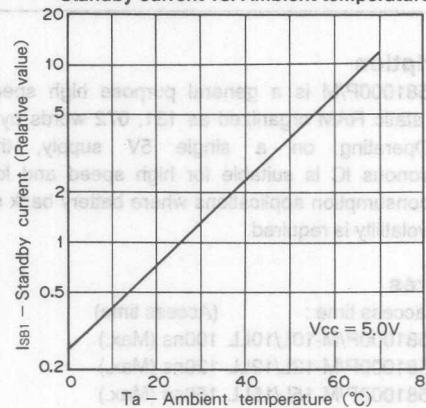
Example of Representative Characteristics



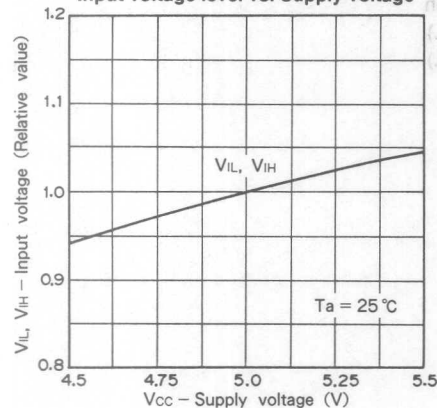
Standby current vs. Supply voltage



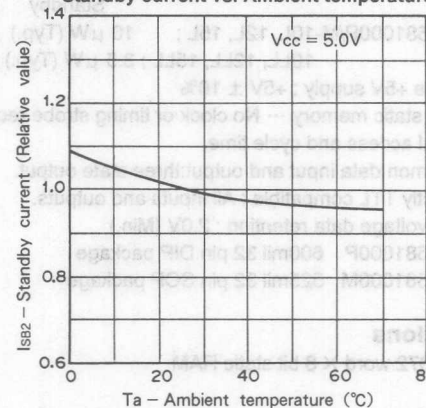
Standby current vs. Ambient temperature



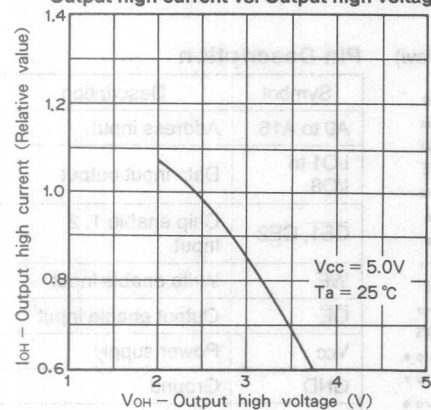
Input voltage level vs. Supply voltage



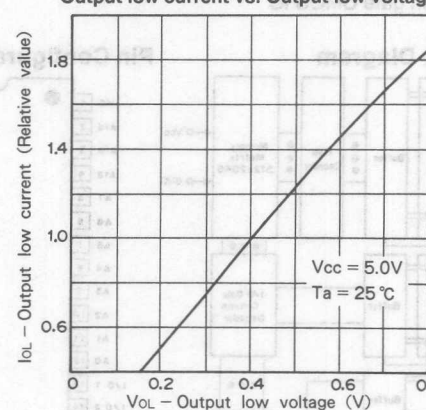
Standby current vs. Ambient temperature



Output high current vs. Output high voltage



Output low current vs. Output low voltage



SONY® CXK581000P/M -10L/12L/15L -10LL/12LL/15LL

131072-word × 8-bit High Speed CMOS Static RAM

Description

CXK581000P/M is a general purpose high speed CMOS static RAM organized as 131,072 words by 8 bits. Operating on a single 5V supply, this asynchronous IC is suitable for high speed and low power consumption applications where battery back up for nonvolatility is required.

Features

- Fast access time : (Access time)
CXK581000P/M-10L/10LL 100ns (Max.)
CXK581000P/M-12L/12LL 120ns (Max.)
CXK581000P/M-15L/15LL 150ns (Max.)
- Low power consumption operation :
Standby /DC operation
CXK581000P/M-10L, 12L, 15L ; 10 μ W (Typ.) /35mW (Typ.)
10LL, 12LL, 15LL ; 3.5 μ W (Typ.) /35mW (Typ.)
- Single +5V supply : +5V $\pm$ 10%
- Fully static memory ... No clock or timing strobe required.
- Equal access and cycle time.
- Common data input and output: three state output.
- Directly TTL compatible : All inputs and outputs.
- Low voltage data retention : 2.0V (Min.)
- CXK581000P 600mil 32 pin DIP package
- CXK581000M 525mil 32 pin SOP package

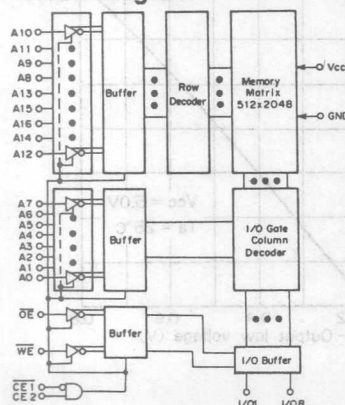
Functions

131,072 word × 8 bit static RAM

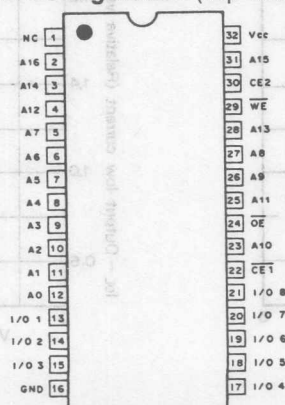
Structure

Silicon gate CMOS IC

Block Diagram



Pin Configuration (Top View)



Pin Description

Symbol	Description
A0 to A16	Address input
I/O1 to I/O8	Data input output
CE1, CE2	Chip enable 1, 2 input
WE	Write enable input
OE	Output enable input
Vcc	Power supply
GND	Ground
NC	No connection

Absolute Maximum Ratings

(Ta=25°C, GND=0V)

Item	Symbol	Rating	Unit
Supply voltage	V _{CC}	− 0.5 to +7.0	V
Input voltage	V _{IH}	− 0.5 * to V _{CC} +0.5	V
Input and output voltage	V _{I/O}	− 0.5 * to V _{CC} +0.5	V
Allowable power dissipation	P _D	CXK581000P 1.0	W
		CXK581000M 0.7	
Operating temperature	T _{opr}	0 to +70	°C
Storage temperature	T _{stg}	− 55 to +150	°C
Soldering temperature	T _{solder}	260•10	°C • sec

* V_{IH}, V_{I/O} = − 3.0V Min. for pulse width less than 50ns.

Truth Table

CE1	CE2	OE	WE	Mode	I/O pin	V _{CC} current
H	x	x	x	Not selected	High Z	I _{SB1} , I _{SB2}
x	L	x	x	Not selected	High Z	I _{SB1} , I _{SB2}
L	H	H	H	Output disable	High Z	I _{CC1} , I _{CC2} , I _{CC3}
L	H	L	H	Read	Data out	I _{CC1} , I _{CC2} , I _{CC3}
L	H	x	L	Write	Data in	I _{CC1} , I _{CC2} , I _{CC3}

x : "H" or "L"

DC Recommended Operating Conditions (Ta=0 to +70°C, GND=0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Input high voltage	V _{IH}	2.2	—	V _{CC} +0.3	V
Input low voltage	V _{IL}	− 0.3 *	—	0.8	V

* V_{IL} = − 3.0V Min. for pulse width less than 50ns.

Item	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Input capacitance	C _{in}	V _{in} =0V	—	—	8	pF
I/O capacitance	C _{IO}	V _{IO} =0V	—	—	3	pF

(Note) This parameter is sampled and is not 100% tested.

Electrical Characteristics

• DC characteristics

(V_{CC}=5V ± 10%, GND=0V, T_a=0 to +70 °C)

Item	Symbol	Test conditions		- 10L/12L/15L			- 10LL/12LL/15LL			Unit
				Min.	Typ. *	Max.	Min.	Typ. *	Max.	
Input leakage current	I _{LI}	V _{IN} =GND to V _{CC}		- 1	—	1	- 1	—	1	μA
Output leakage current	I _{LO}	CE1=V _{IH} or CE2=V _{IL} or OE=V _{IH} or WE=V _{IL} V _{I/O} =GND to V _{CC}		- 1	—	1	- 1	—	1	μA
Operating power supply current	I _{CC1}	CE1=V _{IL} , CE2=V _{IH} V _{IN} =V _{IH} or V _{IL} I _{OUT} =0mA		—	7	15	—	7	15	mA
Average operating current	I _{CC2}	Min. cycle Duty=100% I _{OUT} =0mA	Write cycle	—	35	60	—	35	60	mA
			Read cycle	—	25	40	—	25	40	
	I _{CC3}	Cycle time 1 μs Duty=100% I _{OUT} =0mA CE1 ≤ 0.2V, CE2 ≥ V _{CC} - 0.2V V _{IL} ≤ 0.2V, V _{IH} ≥ V _{CC} - 0.2V	Write cycle	—	10	20	—	10	20	mA
			Read cycle	—	5	10	—	5	10	
Standby current	I _{SB1}	CE2 ≤ 0.2V or CE1 ≥ V _{CC} - 0.2V CE2 ≥ V _{CC} - 0.2V	0 to 70 °C	—	—	100	—	—	20	μA
			0 to 40 °C	—	—	20	—	—	4	
			+25 °C	—	2	8	—	0.7	2	
	I _{SB2}	CE1=V _{IH} or CE2=V _{IL}	—	0.6	3	—	0.6	3	mA	
Output high voltage	V _{OH}	I _{OH} = - 1.0mA		2.4	—	—	2.4	—	—	V
Output low voltage	V _{OL}	I _{OL} =2.1mA		—	—	0.4	—	—	0.4	V

* V_{CC}=5V, T_a=25 °C

I/O capacitance

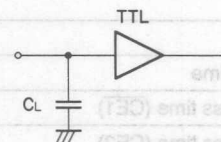
(T_a=25 °C, f=1MHz)

Item	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} =0V	—	—	6	pF
I/O capacitance	C _{I/O}	V _{I/O} =0V	—	—	8	pF

Note) This parameter is sampled and is not 100% tested.

AC characteristics**• AC test conditions** ($V_{CC}=5V \pm 10\%$, $T_a=0$ to $+70^\circ C$)

Item	Conditions
Input pulse high level	$V_{IH}=2.2V$
Input pulse low level	$V_{IL}=0.8V$
Input rise time	$t_r=5ns$
Input fall time	$t_f=5ns$
Input and output reference level	1.5V
Output load conditions	$C_L^*=100pF$, 1TTL

* C_L includes scope and jig capacitances.**• Test circuit**

* $t_{r/f}$, t_{dH} and t_{dL} are defined as the time required for outputs to turn to high impedance state and are not referred to as output voltage levels.

• White cycle

Item	Symbol	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Write cycle time	t_{wc}	100	—	120	—	130	—	ns
Address valid to end of write	t_{aw}	70	—	85	—	100	—	ns
Chip enable to end of write	t_{cew}	70	—	85	—	100	—	ns
Data to write time overlap	t_{dow}	40	—	50	—	60	—	ns
Data hold from write time	t_{dhw}	0	—	0	—	0	—	ns
Write pulse width	t_{wp}	70	—	80	—	90	—	ns
Address setup time	t_{as}	0	—	0	—	0	—	ns
Write recovery time (W_R)	t_{wr}	0	—	0	—	0	—	ns
Write recovery time (CE , $CE\bar$)	t_{wrc}	0	—	0	—	0	—	ns
Output active from end of write	t_{ow}	10	—	10	—	10	—	ns
Write to output in high Z	t_{wto}^*	—	30	—	30	—	30	ns

* t_{wto} is defined as the time required for outputs to turn to high impedance state and is not referred to as output voltage level.

• Read cycle ($\overline{WE}$ ="H")

Item	Symbol	- 10L/10LL		- 12L/12LL		- 15L/15LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t_{RC}	100	—	120	—	150	—	ns
Address access time	t_{AA}	—	100	—	120	—	150	ns
Chip enable access time ($\overline{CE1}$)	t_{CO1}	—	100	—	120	—	150	ns
Chip enable access time (CE2)	t_{CO2}	—	100	—	120	—	150	ns
Output enable to output valid	t_{OE}	—	50	—	60	—	70	ns
Output hold from address change	t_{OH}	15	—	15	—	15	—	ns
Chip enable to output in low Z ($\overline{CE1}$, CE2)	t_{LZ1} , t_{LZ2}	10	—	10	—	10	—	ns
Output enable to output in low Z ($\overline{OE}$)	t_{OLZ}	5	—	5	—	5	—	ns
Chip disable to output in high Z ($\overline{CE1}$, CE2)	t_{HZ1}^* , t_{HZ2}^*	—	35	—	40	—	50	ns
Output disable to output in high Z ($\overline{OE}$)	t_{OHZ}^*	—	35	—	40	—	50	ns

* t_{HZ1} , t_{HZ2} and t_{OHZ} are defined as the time required for outputs to turn to high impedance state and are not referred to as output voltage levels.

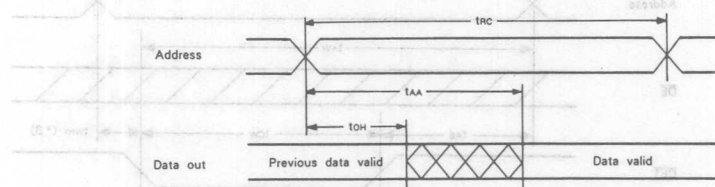
• Write cycle

Item	Symbol	- 10L/10LL		- 12L/12LL		- 15L/15LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t_{WC}	100	—	120	—	150	—	ns
Address valid to end of write	t_{AW}	70	—	85	—	100	—	ns
Chip enable to end of write	t_{CW}	70	—	85	—	100	—	ns
Data to write time overlap	t_{DW}	40	—	50	—	60	—	ns
Data hold from write time	t_{DH}	0	—	0	—	0	—	ns
Write pulse width	t_{WP}	70	—	80	—	90	—	ns
Address setup time	t_{AS}	0	—	0	—	0	—	ns
Write recovery time ($\overline{WE}$)	t_{WR}	0	—	0	—	0	—	ns
Write recovery time ($\overline{CE1}$, CE2)	t_{WR1}	0	—	0	—	0	—	ns
Output active from end of write	t_{OW}	10	—	10	—	10	—	ns
Write to output in high Z	t_{WHZ}^*	—	30	—	30	—	30	ns

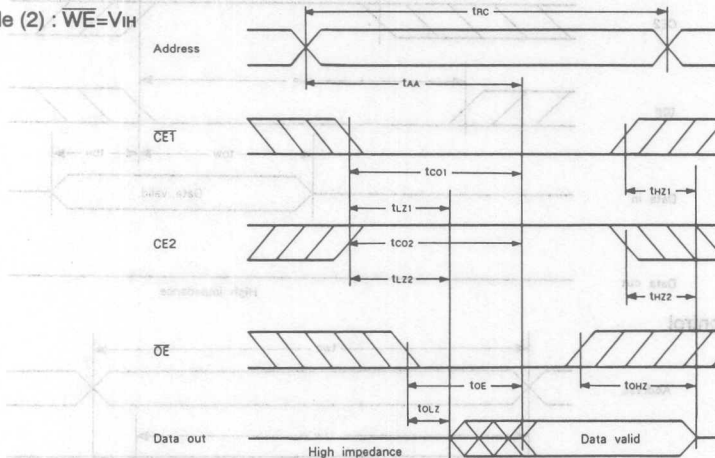
* t_{WHZ} is defined as the time required for outputs to turn to high impedance state and is not referred to as output voltage level.

Timing Waveform

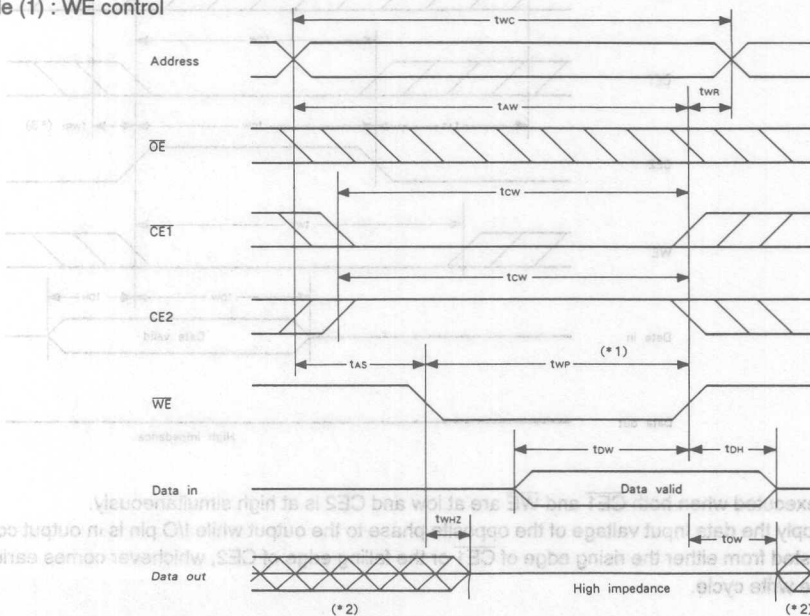
- Read cycle (1) : $\overline{CE1}=\overline{OE}=V_{IL}$, $\overline{CE2}=V_{IH}$, $\overline{WE}=V_{IH}$



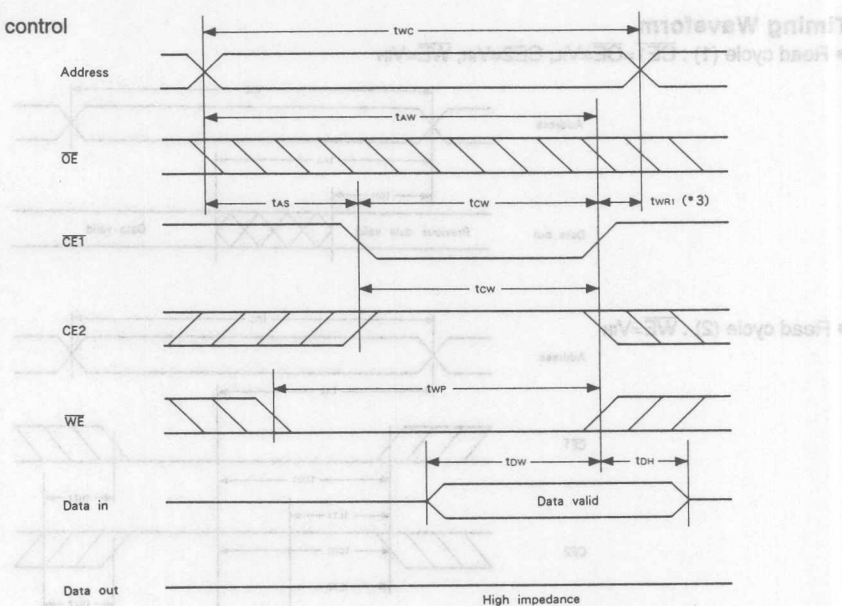
- Read cycle (2) : $\overline{WE}=V_{IH}$



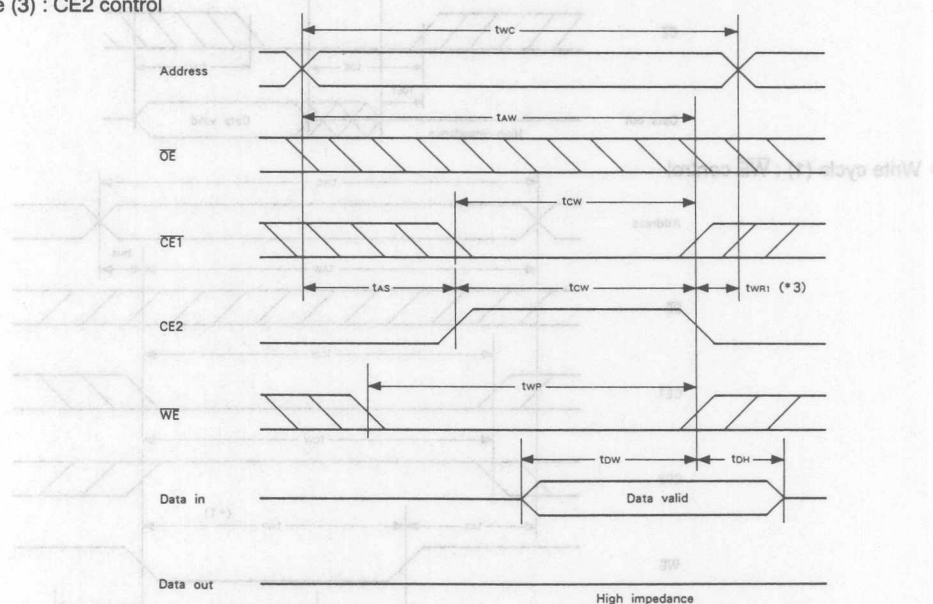
- Write cycle (1) : $\overline{WE}$ control



• Write cycle (2) : $\overline{CE1}$ control



• Write cycle (3) : CE2 control



Note)

- * 1. Write is executed when both $\overline{CE1}$ and $\overline{WE}$ are at low and CE2 is at high simultaneously.
- * 2. Do not apply the data input voltage of the opposite phase to the output while I/O pin is in output condition.
- * 3. t_{WR1} is tested from either the rising edge of $\overline{CE1}$ or the falling edge of CE2, whichever comes earlier, until the end of the write cycle.

Data Retention Characteristics

(Ta=0 to 70 °C)

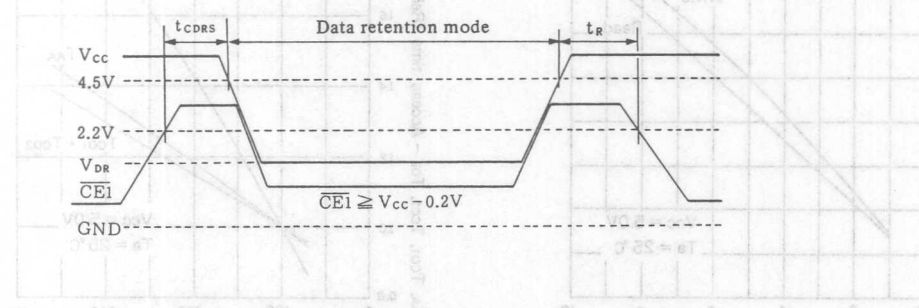
Item	Symbol	Test conditions	- 10L/12L/15L			- 10LL/12LL/15LL			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Data retention voltage	V _{DR}	* 1	2.0	—	5.5	2.0	—	5.5	V
Data retention current	I _{CCDR1}	V _{CC} =3.0V * 1	0 to 70 °C	—	50	—	—	12	μA
			0 to 40 °C	—	10	—	—	2.4	
			+25 °C	—	1	—	0.4	1.2	
	I _{CCDR2}	V _{CC} =2.0 to 5.5V * 1	—	2	100	—	0.7	20	mA
Data retention setup time	t _{CDRS}	Chip disable to data retention mode	0	—	—	0	—	—	ns
Recovery time	t _R		t _{RC} * 2	—	—	t _{RC} * 2	—	—	ns

Note)

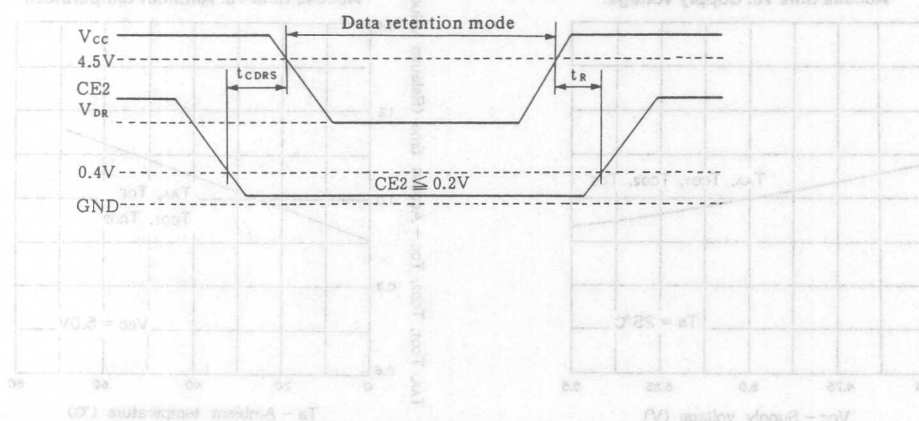
* 1. $\overline{CE1} \geq V_{CC} - 0.2V$, $CE2 \geq V_{CC} - 0.2V$ ($\overline{CE1}$ control) or $CE2 \leq 0.2V$ ($CE2$ control)* 2. t_{RC}: Read cycle time

Data retention waveform

- Low supply voltage data retention waveform (1) ($\overline{CE1}$ control)

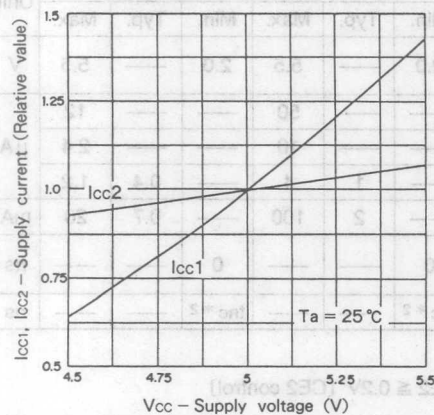


- Low supply voltage data retention waveform (2) ($CE2$ control)

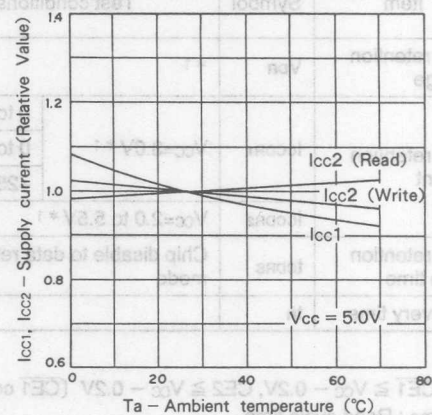


Example of Representative Characteristics

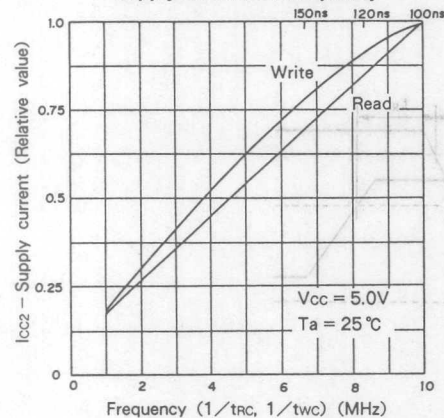
Supply current vs. Supply voltage



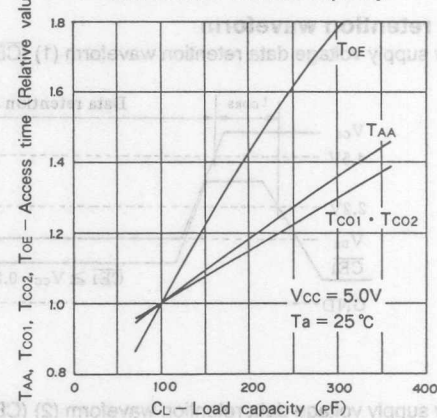
Supply current vs. Ambient temperature



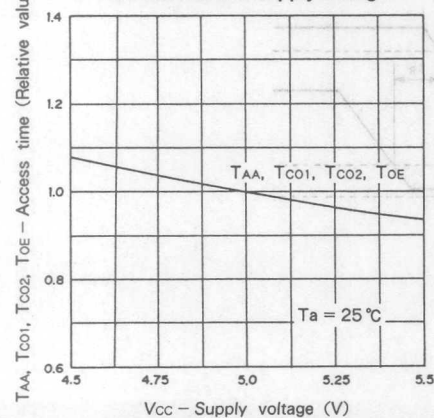
Supply current vs. Frequency



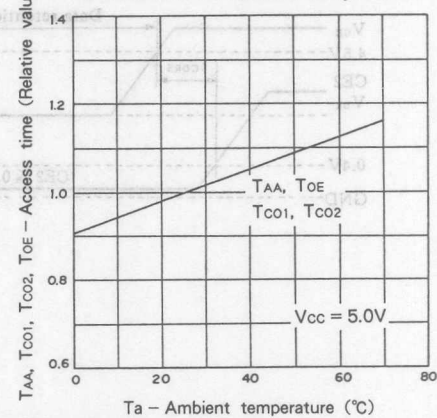
Access time vs. Load capacity



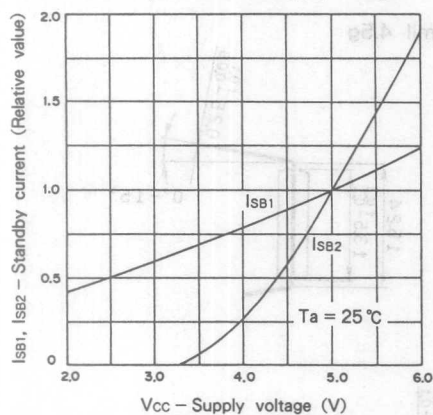
Access time vs. Supply voltage



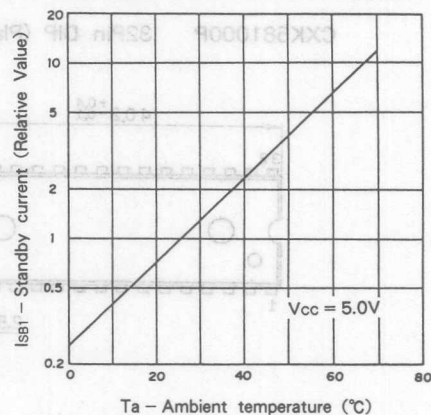
Access time vs. Ambient temperature



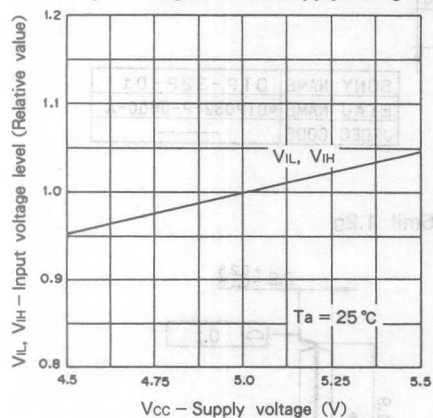
Standby current vs. Supply voltage



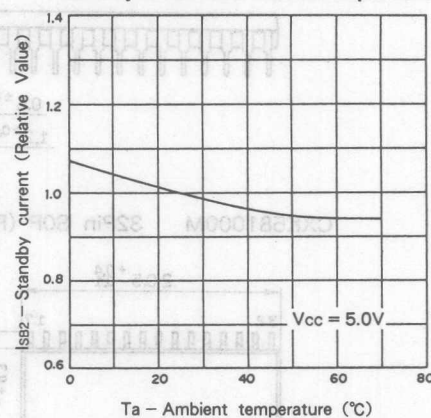
Standby current vs. Ambient temperature



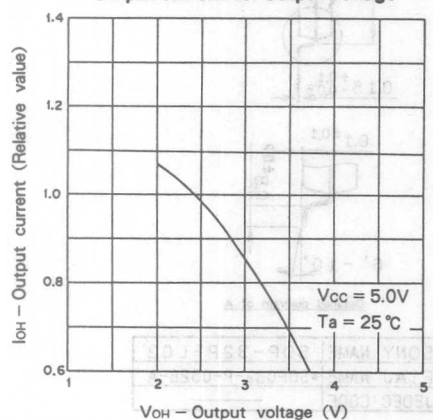
Input voltage level vs. Supply voltage



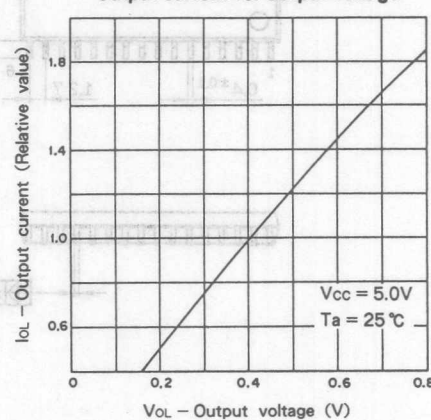
Standby current vs. Ambient temperature



Output current vs. Output voltage

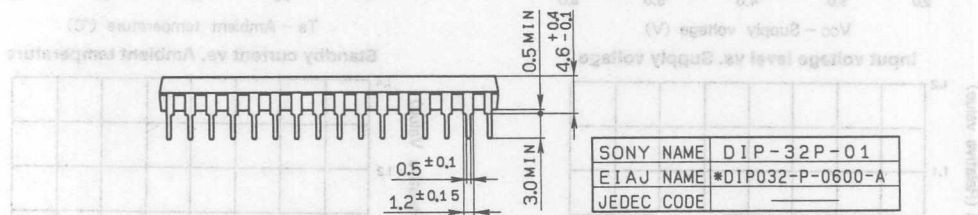
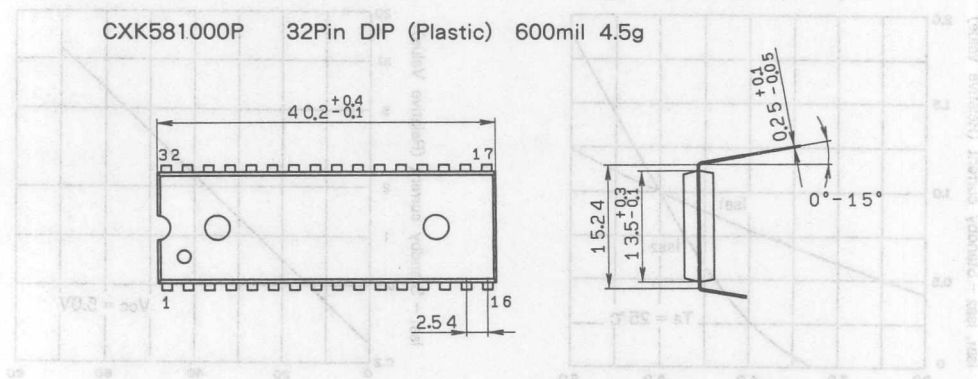


Output current vs. Output voltage

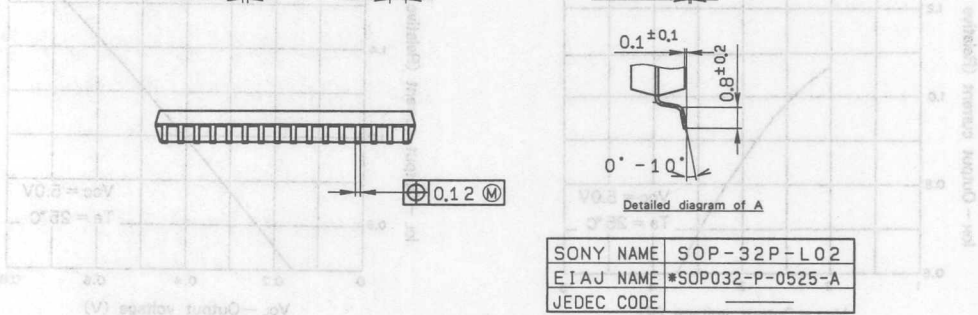
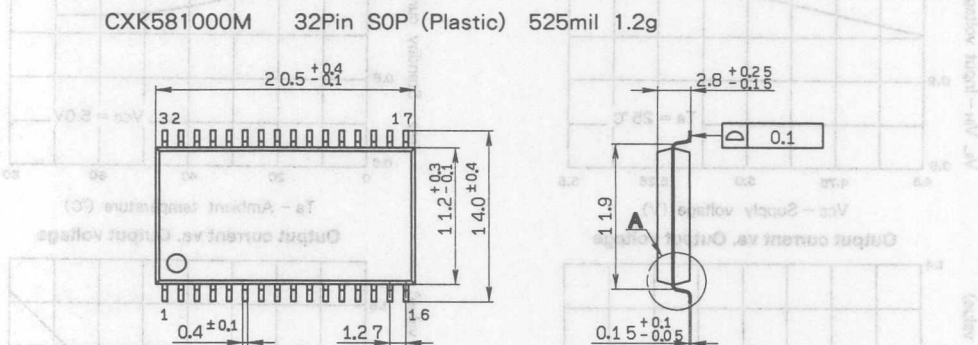


Package Outline Unit : mm

CXK581000P 32Pin DIP (Plastic) 600mil 4.5g



CXK581000M 32Pin SOP (Plastic) 525mil 1.2g



SONY CXK581000P/M -10LX/12LX/15LX/ 10LLX/12LLX/15LLX

131072-word × 8-bit High Speed CMOS Static RAM

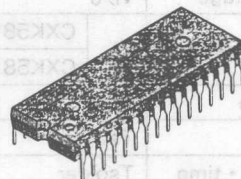
Description

The CXK581000P/M is a general purpose high speed CMOS static RAM organized as 131072 words by 8 bits. Operating on a single 5V supply, this asynchronous IC is suitable for high speed and low power consumption applications where battery back-up for nonvolatility is required.

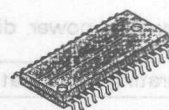
Features

- Extended operating temperature range
(-25°C to +85°C)
- Fast access time (Access time)
CXK581000P/M-10LX/10LLX 100ns (Max.)
CXK581000P/M-12LX/12LLX 120ns (Max.)
CXK581000P/M-15LX/15LLX 150ns (Max.)
- Low power consumption operation
Standby/DC operation
CXK581000P/M-10LX, 12LX, 15LX 10 μW(Typ.)/35mW(Typ.)
CXK581000P/M-10LLX, 12LLX, 15LLX 3.5 μW(Typ.)/35mW(Typ.)
- Single +5V power supply: +5V ± 10%
- Fully static memory...No clock or timing strobe required.
- Equal access and cycle time.
- Common data input and output: three state output.
- Directly TTL compatible: All inputs and outputs.
- Low voltage data retention: 2.2V (Min.)
- CXK581000P 600mil 32 pin DIP package
- CXK581000M 525mil 32 pin SOP package

CXK581000P
32 pin DIP (Plastic)



CXK581000M
32 pin SOP (Plastic)



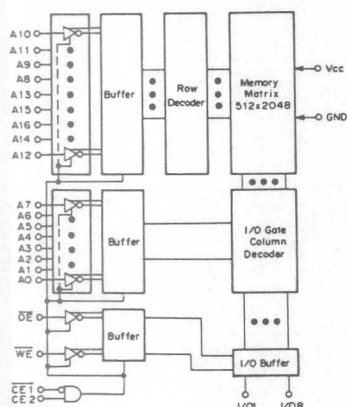
Function

131072-word × 8-bit static RAM

Structure

Silicon gate CMOS IC

Block Diagram



Pin Configuration (Top View)



Pin Description

Symbol	Description
A0 to A16	Address input
I/O1 to I/O8	Data input/output
CE1, CE2	Chip enable 1, 2 input
WE	Write enable input
OE	Output enable input
Vcc	+ 5V power supply
GND	Ground
NC	No connection

Absolute Maximum Ratings (Ta = 25°C, GND = 0V)

Item	Symbol	Rating	Unit
Supply voltage	V _{CC}	-0.5 to +7.0	V
Input voltage	V _{IN}	-0.5* to V _{CC} + 0.5	V
Input and output voltage	V _{I/O}	-0.5* to V _{CC} + 0.5	V
Allowable power dissipation	P _D	CXK581000P	1.0
		CXK581000M	0.7
Operating temperature	T _{opr}	-25 to +85	°C
Storage temperature	T _{stg}	-55 to +150	°C
Soldering temperature • time	T _{solder}	260 • 10	°C • sec

* V_{IN}, V_{I/O} = -3.0V Min. for pulse width less than 50ns.**Truth Table**

CE1	CE2	OE	WE	Mode	I/O1 to I/O8	V _{CC} Current
H	x	x	x	Not selected	High Z	Isb1, Isb2
x	L	x	x	Not selected	High Z	Isb1, Isb2
L	H	H	H	Output disable	High Z	Icc1, Icc2, Icc3
L	H	L	H	Read	Data out	Icc1, Icc2, Icc3
L	H	x	L	Write	Data in	Icc1, Icc2, Icc3

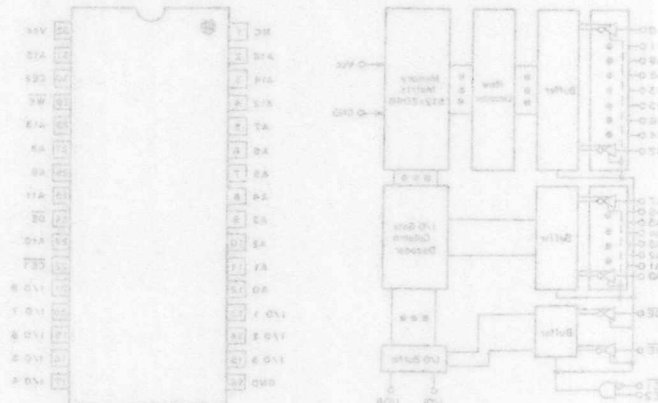
x : "H" or "L"

DC Recommended Operating Conditions (Ta = -25 to +85°C, GND = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Input high voltage	V _{IH}	2.4	—	V _{CC} + 0.3	V
Input low voltage	V _{IL}	-0.3*	—	0.6	V

* V_{IL} = -3.0V Min. for pulse width less than 50ns.

Address input	A0 to A16
Data input/output	I/O1 to I/O8
Chip enable 1, 2	CE1, CE2
Write enable input	WE
Output enable input	OE
+5V power supply	V _{CC}
Ground	GND
No connection	NC



Electrical Characteristics

• DC and operating characteristics

(V_{CC} = 5V ± 10%, GND = 0V, T_a = -25 to +85°C)

Item	Symbol	Test conditions	-10LX/12LX/15LX			-10LLX/12LLX/15LLX			Unit	
			Min.	Typ.*	Max.	Min.	Typ.*	Max.		
Input leakage current	I _{LI}	V _{IN} = GND to V _{CC}	-1	—	1	-1	—	1	μA	
Output leakage current	I _{LO}	CE1 = V _{IH} or CE2 = V _{IL} or OE = V _{IH} or WE = V _{IL} , V _{I/O} = GND to V _{CC}	-1	—	1	-1	—	1	μA	
Operating power supply current	I _{CC1}	CE1 = V _{IL} , CE2 = V _{IH} , V _{IN} = V _{IH} or V _{IL} I _{OUT} = 0mA	—	7	15	—	7	15	mA	
Average operating current	I _{CC2}	Cycle = Min. Duty = 100 %, I _{OUT} = 0mA	Write cycle	—	35	60	—	35	60	mA
			Read cycle	—	25	40	—	25	40	
	I _{CC3}	Cycle time 1 μs Duty = 100 %, I _{OUT} = 0mA CE1 ≤ 0.2V, CE2 ≥ V _{CC} - 0.2V V _{IL} ≤ 0.2V, V _{IH} ≥ V _{CC} - 0.2V	Write cycle	—	10	20	—	10	20	mA
			Read cycle	—	5	10	—	5	10	
Standby current	I _{SB1}	CE2 ≤ 0.2V or CE1 ≥ V _{CC} - 0.2V CE2 ≥ V _{CC} - 0.2V	-25 to 85°C	—	—	200	—	—	40	μA
			-25 to 70°C	—	—	100	—	—	20	
			-25 to 40°C	—	—	20	—	—	4	
			+25°C	—	2	8	—	0.7	2	
	I _{SB2}	CE1 = V _{IH} or CE2 = V _{IL}	—	0.6	3	—	0.6	3	mA	
Output high voltage	V _{OH}	I _{OH} = -1.0mA	2.4	—	—	2.4	—	—	V	
Output low voltage	V _{OL}	I _{OL} = 2.1mA	—	—	0.4	—	—	0.4	V	

* V_{CC} = 5V, T_a = 25°C

I/O capacitance

(T_a = 25°C, f = 1MHz)

Item	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} = 0V	—	—	6	pF
I/O capacitance	C _{I/O}	V _{I/O} = 0V	—	—	8	pF

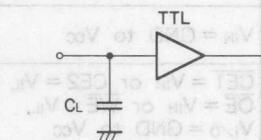
(Note) This parameter is sampled and is not 100% tested.

AC characteristics

● AC test conditions

(V_{CC} = 5V ± 10%, T_a = -25 to +85°C)

Item	Conditions
Input pulse high level	V _{IH} = 2.4V
Input pulse low level	V _{IL} = 0.6V
Input rise time	t _r = 5ns
Input fall time	t _f = 5ns
Input and output reference level	1.5V
Output load conditions	C _L * = 100pF, 1TTL

* C_L includes scope and jig capacitances

Item	Symbol	Test conditions	Min.	Typ.	Max.
Input leakage current	I _{IL}	V _{IH} = 2.4V, V _{IL} = 0.6V, V _{CC} = 5V, T _a = 25°C	—	—	—
Output leakage current	I _{OL}	V _{IH} = 2.4V, V _{IL} = 0.6V, V _{CC} = 5V, T _a = 25°C	—	—	—
Operating power supply current	I _{CC}	V _{IH} = 2.4V, V _{IL} = 0.6V, V _{CC} = 5V, T _a = 25°C	—	—	—
Average operating current	I _{CC}	V _{IH} = 2.4V, V _{IL} = 0.6V, V _{CC} = 5V, T _a = 25°C	—	—	—
Standby current	I _{CC}	V _{IH} = 2.4V, V _{IL} = 0.6V, V _{CC} = 5V, T _a = 25°C	—	—	—
Output high voltage	V _{OH}	I _{OH} = -1.0mA, V _{CC} = 5V, T _a = 25°C	2.4	—	—
Output low voltage	V _{OL}	I _{OL} = 5.1mA, V _{CC} = 5V, T _a = 25°C	0.4	—	—

* V_{CC} = 5V, T_a = 25°C(T_a = 25°C, f = 1MHz)

Item	Symbol	Test conditions	Min.	Typ.	Max.
Input capacitance	C _{IN}	V _{IH} = 0V, V _{IL} = 0V	—	—	8
Output capacitance	C _{OUT}	V _{IH} = 0V, V _{IL} = 0V	—	—	8

(Note) This parameter is sampled and is not 100% tested.

• Read cycle ($\overline{WE}$ = "H")

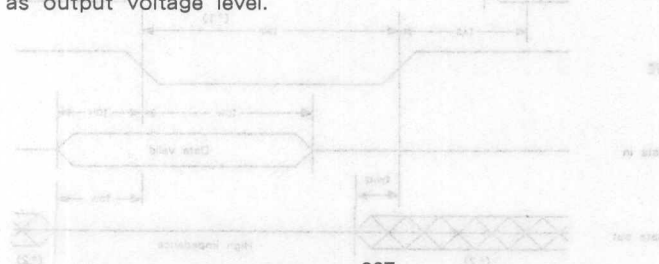
Item	Symbol	-10LX/10LLX		-12LX/12LLX		-15LX/15LLX		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t _{RC}	100	—	120	—	150	—	ns
Address access time	t _{AA}	—	100	—	120	—	150	ns
Chip enable access time (CE1)	t _{CO1}	—	100	—	120	—	150	ns
Chip enable access time (CE2)	t _{CO2}	—	100	—	120	—	150	ns
Output enable to output valid	t _{OE}	—	50	—	60	—	70	ns
Output hold from address change	t _{OH}	10	—	10	—	10	—	ns
Chip enable to output in low Z (CE1, CE2)	t _{LZ1} , t _{LZ2}	10	—	10	—	10	—	ns
Output enable to output in low Z ($\overline{OE}$)	t _{OLZ}	5	—	5	—	5	—	ns
Chip disable to output in high Z (CE1, CE2)	t _{HZ1} *, t _{HZ2} *	—	35	—	40	—	50	ns
Chip disable to output in high Z ($\overline{OE}$)	t _{OHZ} *	—	35	—	40	—	50	ns

* t_{HZ1}, t_{HZ2} and t_{OHZ} are defined as the time required for outputs to turn to high impedance state and are not referred to as output voltage levels.

• Write cycle

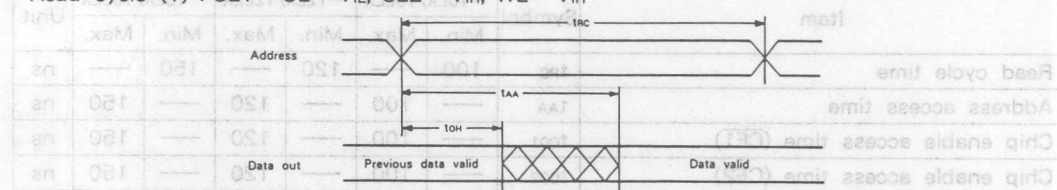
Item	Symbol	-10LX/10LLX		-12LX/12LLX		-15LX/15LLX		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t _{WC}	100	—	120	—	150	—	ns
Address valid to end of write	t _{AW}	70	—	85	—	100	—	ns
Chip enable to end of write	t _{CW}	70	—	85	—	100	—	ns
Data to write time overlap	t _{DW}	40	—	50	—	60	—	ns
Data hold from write time	t _{DH}	0	—	0	—	0	—	ns
Write pulse width	t _{WP}	70	—	80	—	90	—	ns
Address setup time	t _{AS}	0	—	0	—	0	—	ns
Write recovery time ($\overline{WE}$)	t _{WR}	5	—	5	—	5	—	ns
Write recovery time (CE1, CE2)	t _{WR1}	0	—	0	—	0	—	ns
Output active from end of write	t _{OW}	10	—	10	—	10	—	ns
Write to output in high Z	t _{WHZ} *	—	30	—	30	—	30	ns

* t_{WHZ} is defined as the time required for outputs to turn to high impedance state and is not referred to as output voltage level.

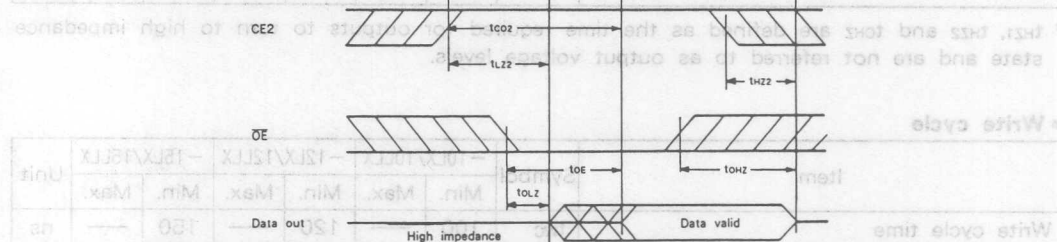
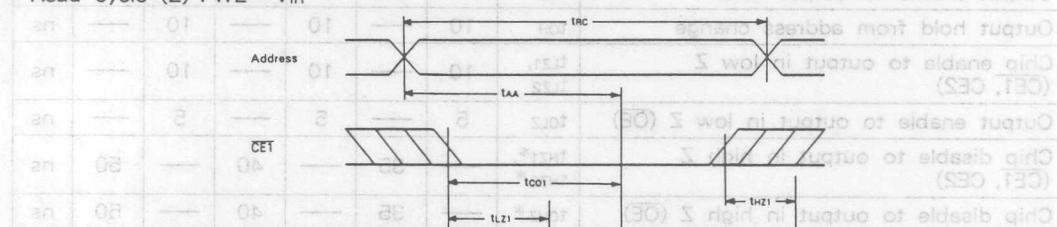


Timing Waveform

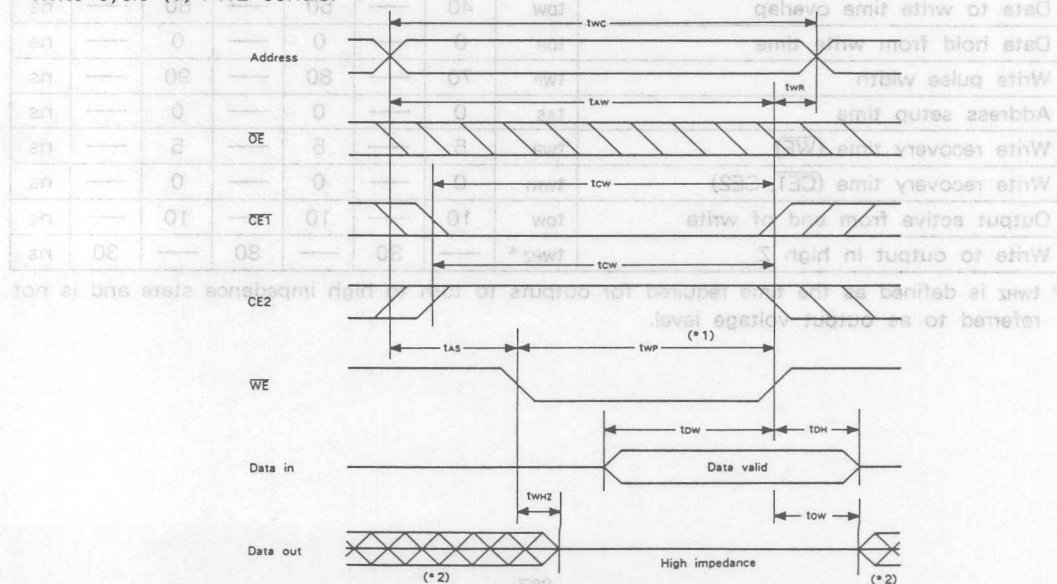
- Read cycle (1) : $\overline{CE1} = \overline{OE} = V_{IL}$, $\overline{CE2} = V_{IH}$, $\overline{WE} = V_{IH}$



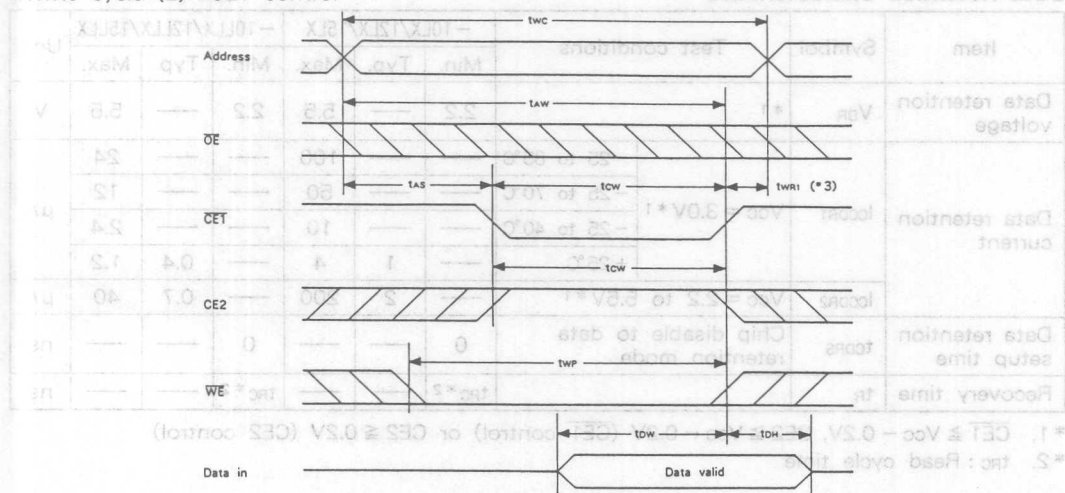
- Read cycle (2) : $\overline{WE} = V_{IH}$



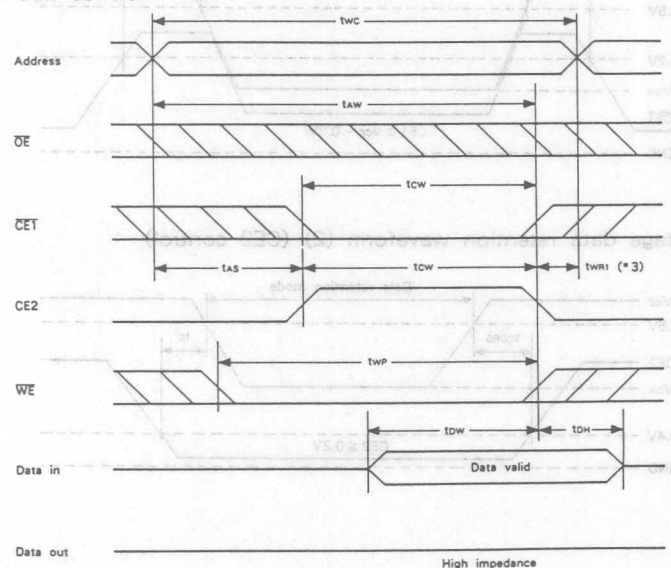
- Write cycle (1) : $\overline{WE}$ control



• Write cycle (2) : $\overline{\text{CE1}}$ control



• Write cycle (3) : CE2 control



Note)

- *1. Write is executed when both $\overline{\text{CE1}}$ and $\overline{\text{WE}}$ are at low and CE2 is at high simultaneously.
- *2. Do not apply the data input voltage of the opposite phase to the output while I/O pin is in output condition.
- *3. twr1 is tested from either the rising edge of $\overline{\text{CE1}}$ or the falling edge of CE2, whichever comes earlier, until the end of the write cycle.

Data Retention Characteristics

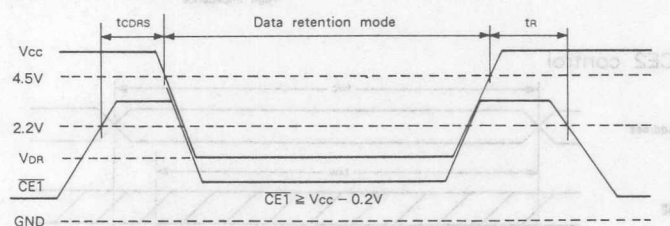
(Ta = -25 to 85°C)

Item	Symbol	Test conditions	-10LX/12LX/15LX			-10LLX/12LLX/15LLX			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Data retention voltage	V _{DR}	*1	2.2	—	5.5	2.2	—	5.5	V
Data retention current	I _{CCDR1}	V _{CC} = 3.0V *1	-25 to 85°C	—	100	—	—	24	μA
			-25 to 70°C	—	50	—	—	12	
			-25 to 40°C	—	10	—	—	2.4	
			+25°C	—	1	—	0.4	1.2	
	I _{CCDR2}	V _{CC} = 2.2 to 5.5V *1	—	2	200	—	0.7	40	μA
Data retention setup time	t _{CDRS}	Chip disable to data retention mode	0	—	—	0	—	—	ns
Recovery time	t _R		t _{RC} *2	—	—	t _{RC} *2	—	—	ns

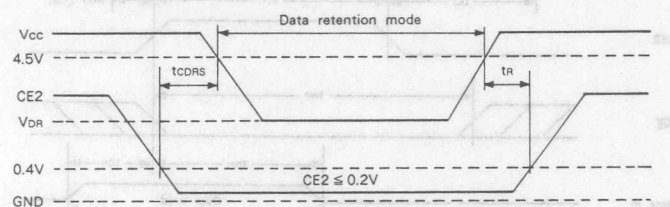
*1. $\overline{CE1} \geq V_{CC} - 0.2V$, $CE2 \geq V_{CC} - 0.2V$ ($\overline{CE1}$ control) or $CE2 \leq 0.2V$ ($CE2$ control)*2. t_{RC}: Read cycle time

Data retention waveform

- Low supply voltage data retention waveform (1) ($\overline{CE1}$ control)



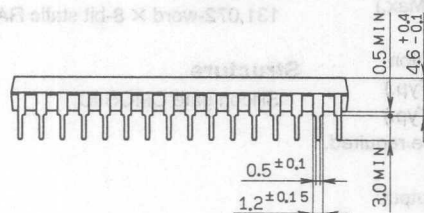
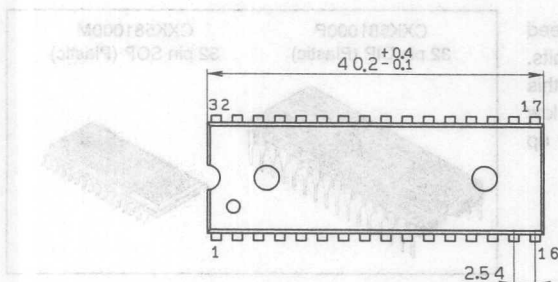
- Low supply voltage data retention waveform (2) ($CE2$ control)



Package Outline Unit : mm

CXK581000P

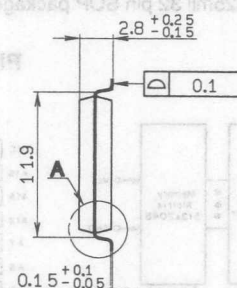
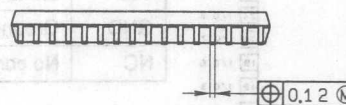
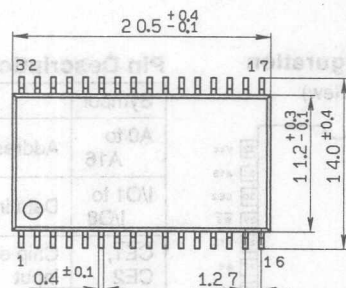
32 pin DIP (Plastic) 600mil 4.5g



SONY NAME	DIP-32P-01
EIAJ NAME	*DIP032-P-0600-A
JEDEC CODE	

CXK581000M

32 pin SOP (Plastic) 525mil 1.2g



Detailed diagram of A

SONY NAME	SOP-32P-L02
EIAJ NAME	*SOP032-P-0525-A
JEDEC CODE	

SONY

CXK581000P/M -12LB

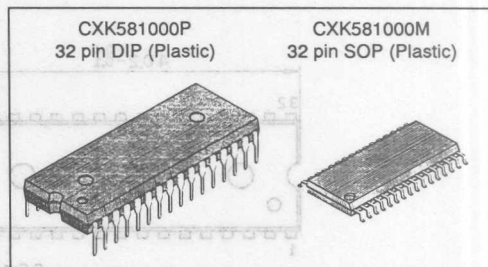
131072-word × 8-bit High Speed CMOS Static RAM

Description

The CXK581000P/M is a general purpose high speed CMOS static RAM organized as 131,072 words by 8 bits. Operating on a single 2.7 to 5.5V supply, this asynchronous IC is suitable for high speed and low power consumption applications where battery back up for nonvolatility is required.

Features

- Wide supply voltage range operation: 2.7 to 5.5V
- Fast access time: (Access time)
 - 3V Operation; 240ns (Max.)
 - 5V Operation; 120ns (Max.)
- Low power consumption operation:
 - Standby/ DC operation
 - 3V Operation; 3 μ W (Typ.) / 1.2mW (Typ.)
 - 5V Operation; 10 μ W (Typ.) / 35mW (Typ.)
- Fully static memory... No clock or timing strobe required.
- Equal access and cycle time.
- Common data input and output: three state output.
- Directly TTL compatible: All inputs and outputs.
- Low voltage data retention: 2.0V (Min.)
- CXK581000P 600mil 32 pin DIP package
- CXK581000M 525mil 32 pin SOP package



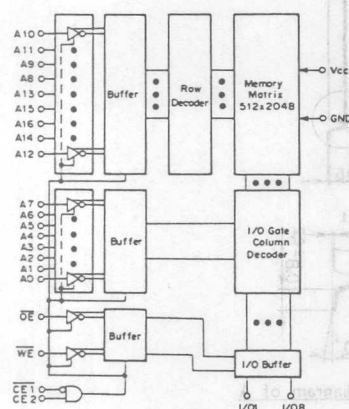
Function

131,072-word × 8-bit static RAM

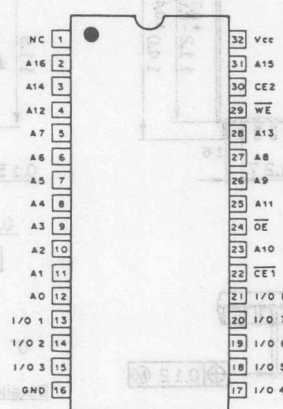
Structure

Silicon gate CMOS IC

Block Diagram



Pin Configuration (Top View)



Pin Description

Symbol	Description
A0 to A16	Address input
I/O1 to I/O8	Data input/output
CE1, CE2	Chip enable 1, 2 input
WE	Write enable input
OE	Output enable input
Vcc	2.7 to 5.5V power supply
GND	Ground
NC	No connection

Sony reserves the right to change products and specifications without prior notice. This information does not convey any license by any implication or otherwise under any patents or other right. Application circuits shown, if any, are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits.

Absolute Maximum Ratings

(Ta=25°C, GND=0V)

Item	Symbol	Rating	Unit
Supply voltage	V _{CC}	-0.5 to +7.0	V
Input voltage	V _{IN}	-0.5 * to V _{CC} +0.5	V
Input and output voltage	V _{I/O}	-0.5 * to V _{CC} +0.5	V
Allowable power dissipation	P _D	CXK581000P	1.0
		CXK581000M	0.7
			W
Operating temperature	T _{opr}	0 to +70	°C
Storage temperature	T _{stg}	-55 to +150	°C
Soldering temperature * time	T _{solder}	260 * 10	°C * sec

* V_{IN}, V_{I/O}=-3.0V Min. for pulse width less than 50ns.

Truth Table

CE1	CE2	OE	WE	Mode	I/O pin	V _{CC} current
H	x	x	x	Not selected	High Z	I _{SB1} , I _{SB2}
x	L	x	x	Not selected	High Z	I _{SB1} , I _{SB2}
L	H	H	H	Output disable	High Z	I _{CC1} , I _{CC2} , I _{CC3}
L	H	L	H	Read	Data out	I _{CC1} , I _{CC2} , I _{CC3}
L	H	x	L	Write	Data in	I _{CC1} , I _{CC2} , I _{CC3}

x : "H" or "L"

DC Recommended Operating Conditions

(Ta=0 to +70°C, GND=0V)

Item	Symbol	V _{CC} =5V ± 10%			V _{CC} =2.7 to 5.5V			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Supply voltage	V _{CC}	4.5	—	5.5	2.7	—	5.5	V
Input high voltage	V _{IH}	2.2	—	V _{CC} +0.3	2.2	—	V _{CC} +0.3	V
Input low voltage	V _{IL}	-0.3 *	—	0.8	-0.3 *	—	0.4	V

* V_{IL}=-3.0V Min. for pulse width less than 50ns.

Item	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} =0V	—	—	8	pF
I/O capacitance	C _{I/O}	V _{I/O} =0V	—	—	8	pF

(Note) This parameter is sampled and is not 100% tested.

Electrical Characteristics

• DC characteristics

(GND=0V, Ta=0 to +70 °C)

Item	Symbol	Test conditions		Vcc=3V ± 10%			Vcc=5V ± 10%			Unit
				Min.	Typ. *	Max.	Min.	Typ. *	Max.	
Input leakage current	I _{LI}	V _{IN} =GND to V _{CC}		-1	—	1	-1	—	1	μA
Output leakage current	I _{LO}	CE1=V _{IH} or CE2=V _{IL} or OE=V _{IH} or WE=V _{IL} V _{I/O} =GND to V _{CC}		-1	—	1	-1	—	1	μA
Operating power supply current	I _{CC1}	CE1=V _{IL} , CE2=V _{IH} V _{IN} =V _{IH} or V _{IL} I _{OUT} =0mA		—	0.4	0.8	—	7	15	mA
Average operating current	I _{CC2}	Min. cycle Duty=100% I _{OUT} =0mA	Write cycle	—	10	15	—	35	60	mA
			Read cycle	—	10	15	—	25	40	
	I _{CC3}	Cycle time 1 μs Duty=100% I _{OUT} =0mA CE1 ≤ 0.2V, CE2 ≥ V _{CC} -0.2V V _{IL} ≤ 0.2V, V _{IH} ≥ V _{CC} -0.2V	Write cycle	—	5	10	—	10	20	mA
			Read cycle	—	2.5	5	—	5	10	
Standby current	I _{SB1}	CE2 ≤ 0.2V CE1 ≥ V _{CC} -0.2V or CE2 ≥ V _{CC} -0.2V	0 to +70 °C	—	—	60	—	—	100	μA
			0 to +40 °C	—	—	12	—	—	20	
			+25 °C	—	1.2	5	—	2	8	
	I _{SB2}	CE1=V _{IH} or CE2=V _{IL}	—	0.06	0.3	—	0.6	3	mA	
Output high voltage	V _{OH}	I _{OH} =-1.0mA		2.2	—	—	2.4	—	—	V
Output low voltage	V _{OL}	I _{OL} =2.1mA		—	—	0.4	—	—	0.4	V

* Ta=25 °C

I/O Capacitance

(Ta=25 °C, f=1MHz)

Item	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} =0V	—	—	6	pF
I/O capacitance	C _{I/O}	V _{I/O} =0V	—	—	8	pF

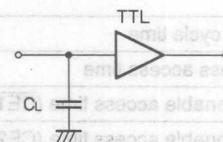
Note) This parameter is sampled and is not 100% tested.

AC Characteristics

● AC test conditions

(V_{CC}=2.7 to 5.5V, T_a=0 to +70 °C)

Item	Conditions	
	V _{CC} =3V	V _{CC} =5V
Input pulse high level	V _{IH} =2.2V	V _{IH} =2.2V
Input pulse low level	V _{IL} =0.4V	V _{IL} =0.8V
Input rise time	tr=5ns	tr=5ns
Input fall time	tf=5ns	tf=5ns
Input and output reference level	1.5V	1.5V
Output load conditions	C _L * =100pF, 1TTL	C _L * =100pF, 1TTL

* C_L includes scope and jig capacitances.

Output enable to output in low Z (OE)	low	low	10	low	low	10
Output enable to output in high Z (OE)	high *	high *	80	high *	high *	80
Output enable to output in high Z (OE)	low *	low *	80	low *	low *	80

* low, high and low are defined as the time required for outputs to turn to high impedance state and are not referred to as output voltage levels.

● Write cycle

Item	Symbol	V _{CC} =3V ± 10%		V _{CC} =5V ± 10%		Unit
		Min.	Max.	Min.	Max.	
Write cycle time	t _{WC}	240	—	120	—	ns
Address valid to end of write	t _{AV}	170	—	88	—	ns
Chip enable to end of write	t _{CE}	170	—	88	—	ns
Data to write time overlap	t _{DO}	100	—	50	—	ns
Data hold from write time	t _{DH}	0	—	0	—	ns
Write pulse width	t _{WP}	180	—	80	—	ns
Address setup time	t _{AS}	0	—	0	—	ns
Write recovery time (WE)	t _{WR}	0	—	0	—	ns
Write recovery time (CE, CEN)	t _{WR}	0	—	0	—	ns
Output active from end of write	t _{OW}	20	—	10	—	ns
Write to output in high Z	t _{OWH} *	—	88	—	30	ns

* t_{OWH} is defined as the time required for outputs to turn to high impedance state and is not referred to as output voltage level.

• Read cycle ($\overline{WE}$ ="H")

Item	Symbol	Vcc=3V $\pm$ 10%		Vcc=5V $\pm$ 10%		Unit
		Min.	Max.	Min.	Max.	
Read cycle time	trc	240	—	120	—	ns
Address access time	tAA	—	240	—	120	ns
Chip enable access time ($\overline{CE1}$)	tC01	—	240	—	120	ns
Chip enable access time ($\overline{CE2}$)	tC02	—	240	—	120	ns
Output enable to output valid	tOE	—	120	—	60	ns
Output hold from address change	tOH	30	—	15	—	ns
Chip enable to output in low Z ($\overline{CE1}$, $\overline{CE2}$)	tLZ1, tLZ2	20	—	10	—	ns
Output enable to output in low Z ($\overline{OE}$)	tOLZ	10	—	5	—	ns
Chip disable to output in high Z ($\overline{CE1}$, $\overline{CE2}$)	tHZ1 *, tHZ2 *	—	80	—	40	ns
Output disable to output in high Z ($\overline{OE}$)	tOHZ *	—	80	—	40	ns

* tHZ1, tHZ2 and tOHZ are defined as the time required for outputs to turn to high impedance state and are not referred to as output voltage levels.

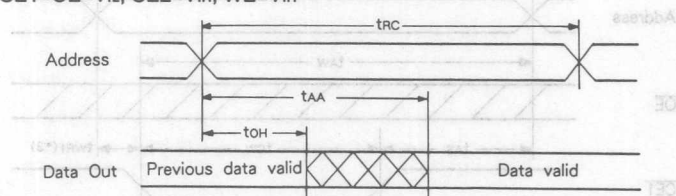
• Write cycle

Item	Symbol	Vcc=3V $\pm$ 10%		Vcc=5V $\pm$ 10%		Unit
		Min.	Max.	Min.	Max.	
Write cycle time	tWC	240	—	120	—	ns
Address valid to end of write	tAW	170	—	85	—	ns
Chip enable to end of write	tCW	170	—	85	—	ns
Data to write time overlap	tDW	100	—	50	—	ns
Data hold from write time	tDH	0	—	0	—	ns
Write pulse width	tWP	160	—	80	—	ns
Address setup time	tAS	0	—	0	—	ns
Write recovery time ($\overline{WE}$)	tWR	0	—	0	—	ns
Write recovery time ($\overline{CE1}$, $\overline{CE2}$)	tWR1	0	—	0	—	ns
Output active from end of write	tOW	20	—	10	—	ns
Write to output in high Z	tWHZ *	—	60	—	30	ns

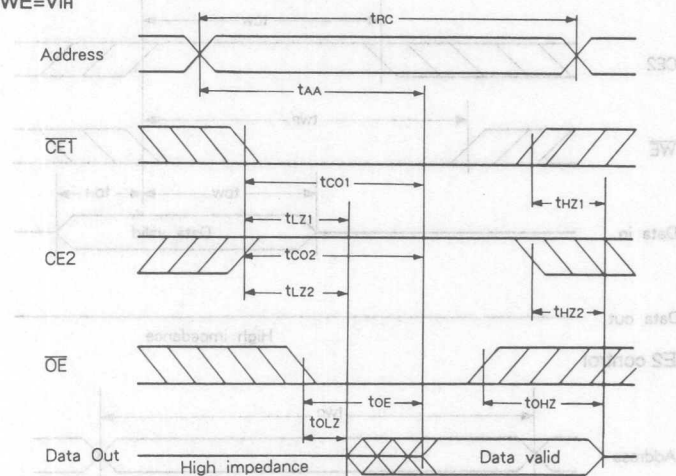
* tWHZ is defined as the time required for outputs to turn to high impedance state and is not referred to as output voltage level.

Timing Waveform

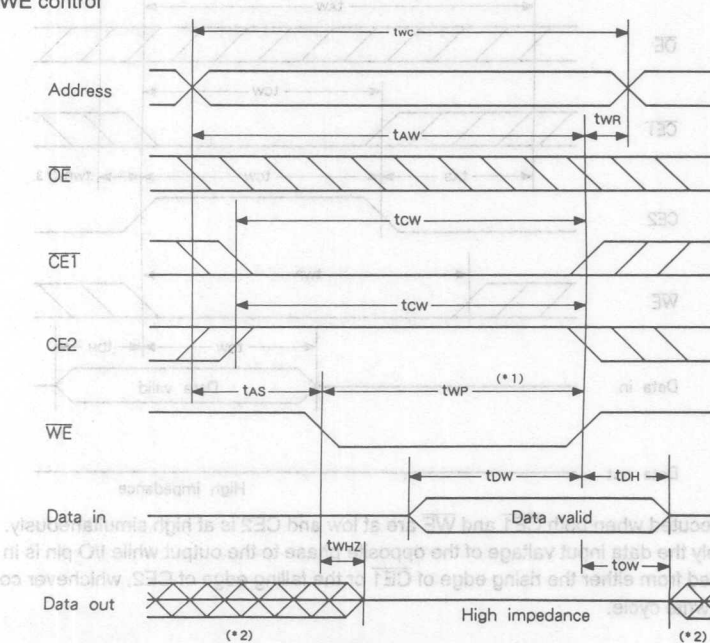
- Read cycle (1) : $\overline{CE1} = \overline{OE} = V_{IL}$, $CE2 = V_{IH}$, $\overline{WE} = V_{IH}$



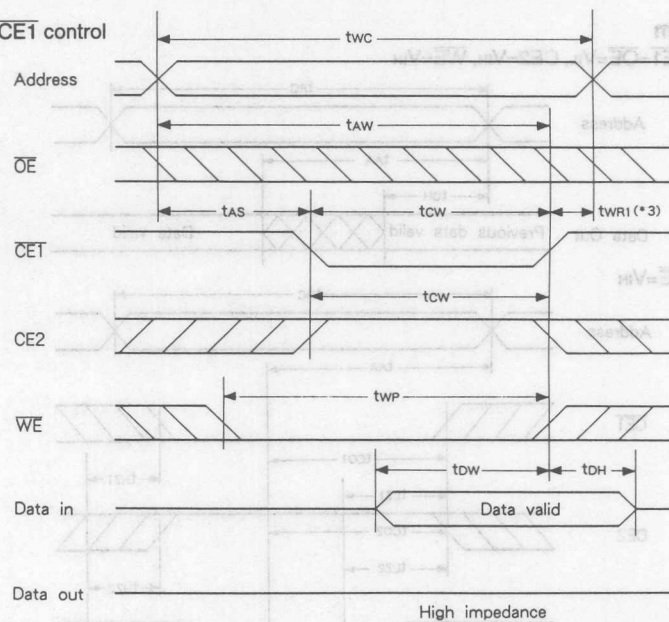
- Read cycle (2) : $\overline{WE}=V_{IH}$



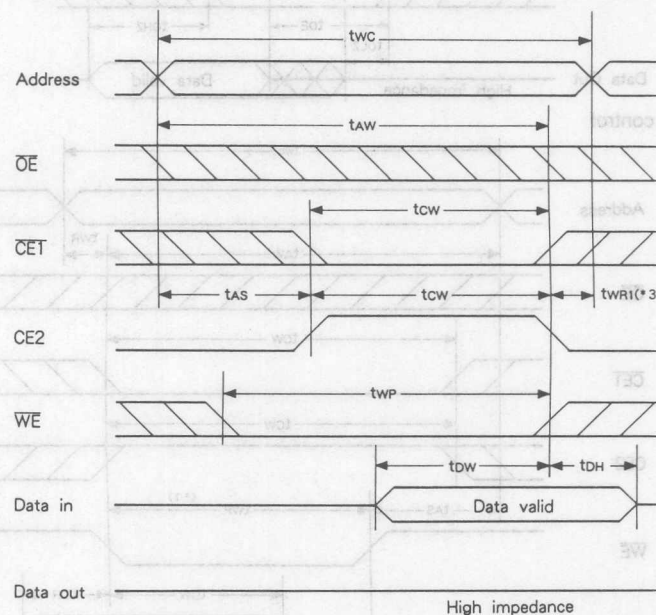
- Write cycle (1) : $\overline{WE}$ control



• Write cycle (2) : $\overline{CE1}$ control



• Write cycle (3) : CE2 control



- * 1. Write is executed when both $\overline{CE1}$ and $\overline{WE}$ are at low and CE2 is at high simultaneously.
- * 2. Do not apply the data input voltage of the opposite phase to the output while I/O pin is in output condition.
- * 3. t_{WR1} is tested from either the rising edge of $\overline{CE1}$ or the falling edge of CE2, whichever comes earlier, until the end of the write cycle.

Data Retention Characteristics

(Ta=0 to +70°C)

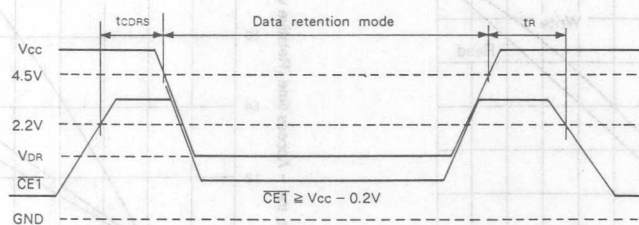
Item	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Data retention voltage	V _{DR}	* 1	2.0	—	5.5	V
Data retention current	I _{CCDR1}	V _{CC} =3.0V * 1	—	—	50	μA
		0 to +70°C	—	—	10	
		+25°C	—	1	4	
	I _{CCDR2}	V _{CC} =2.0 to 5.5V * 1	—	2	100	μA
Data retention setup time	t _{CDRS}	Chip disable to data retention mode	0	—	—	ns
Recovery time	t _R		t _{RC} * 2	—	—	ns

* 1. $\overline{\text{CE1}} \geq V_{\text{CC}} - 0.2\text{V}$, $\text{CE2} \geq V_{\text{CC}} - 0.2\text{V}$ ($\overline{\text{CE1}}$ control) or $\text{CE2} \leq 0.2\text{V}$ (CE2 control)

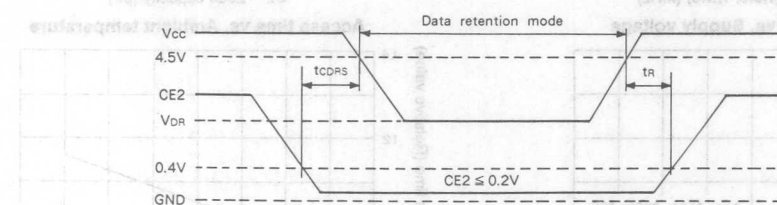
* 2. t_{RC} : Read cycle time

Data Retention Waveform

- Low supply voltage data retention waveform (1) : $\overline{\text{CE1}}$ control

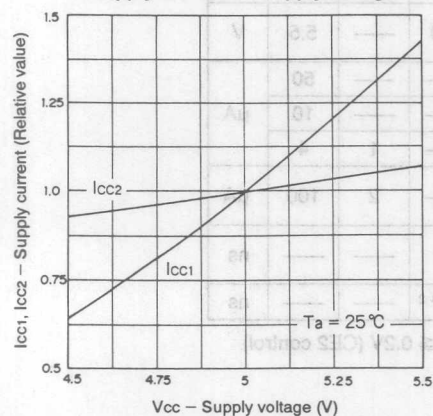


- Low supply voltage data retention waveform (2) : CE2 control

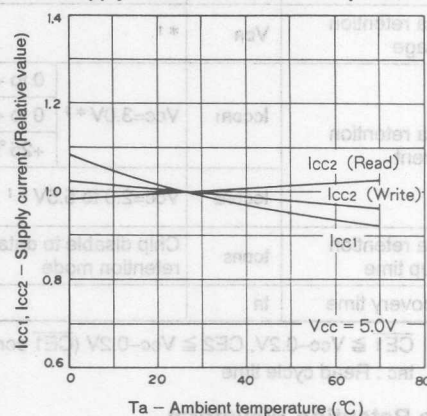


Example of Representative Characteristics

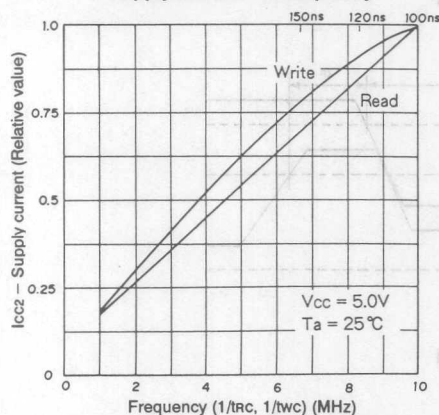
Supply current vs. Supply voltage



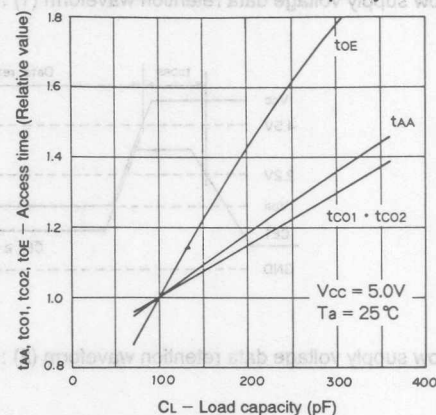
Supply current vs. Ambient temperature



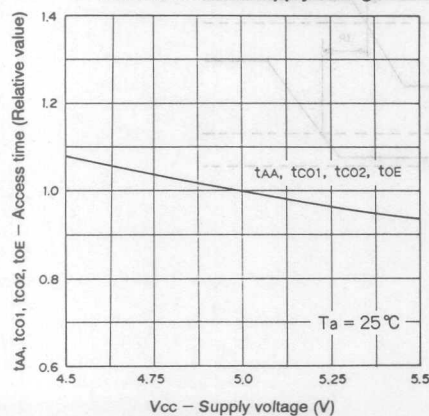
Supply current vs. Frequency



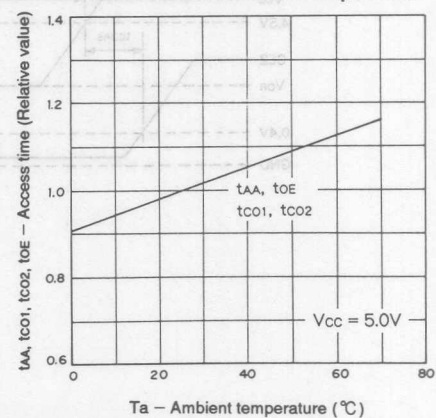
Access time vs. Load capacity



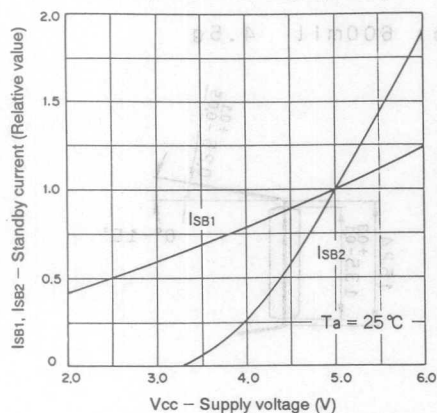
Access time vs. Supply voltage



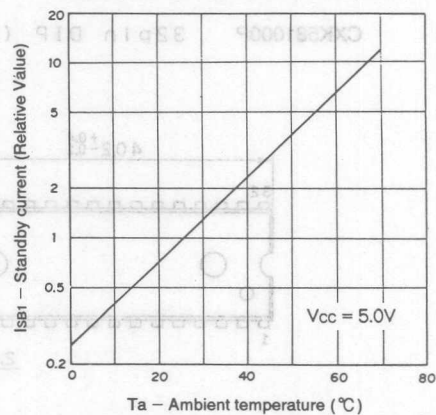
Access time vs. Ambient temperature



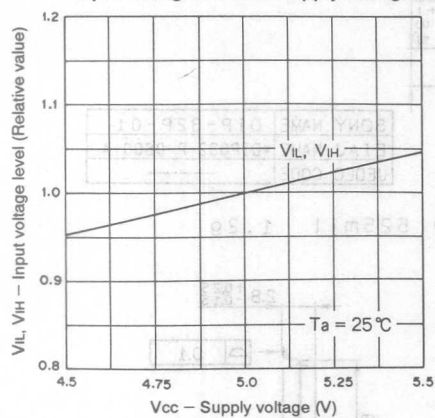
Standby current vs. Supply voltage



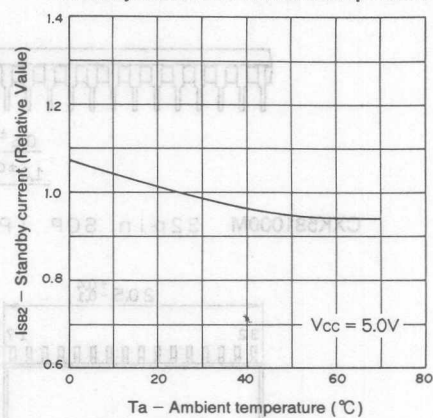
Standby current vs. Ambient temperature



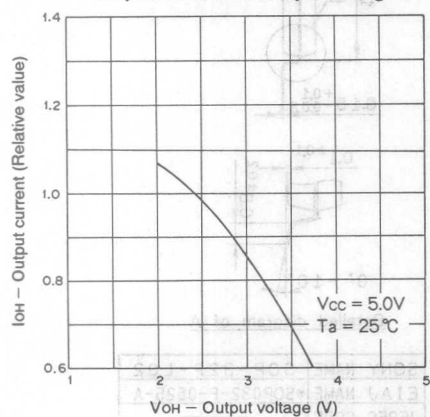
Input voltage level vs. Supply voltage



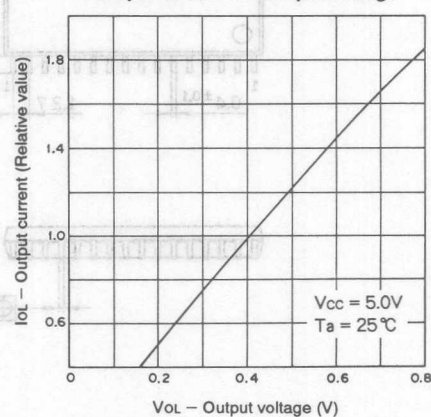
Standby current vs. Ambient temperature



Output current vs. Output voltage

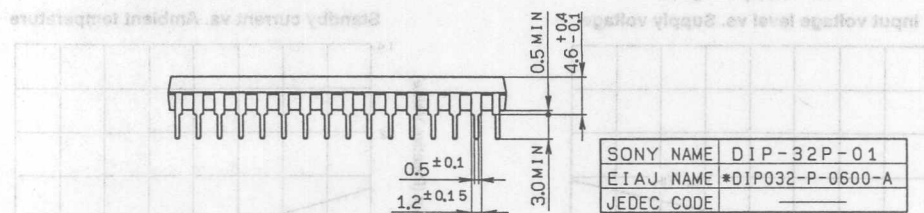
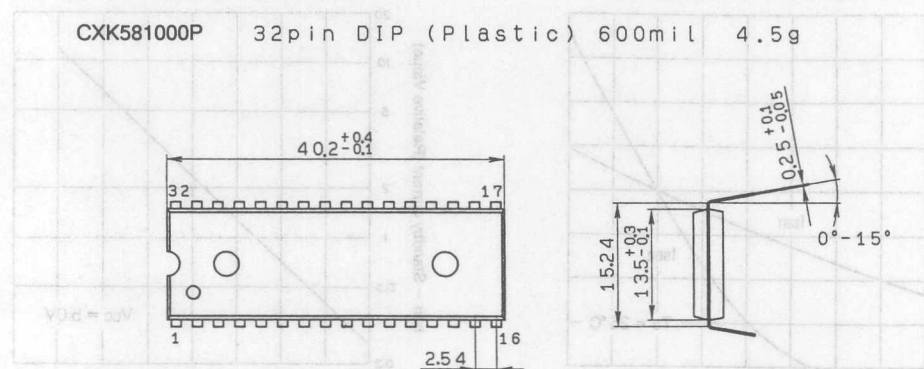


Output current vs. Output voltage

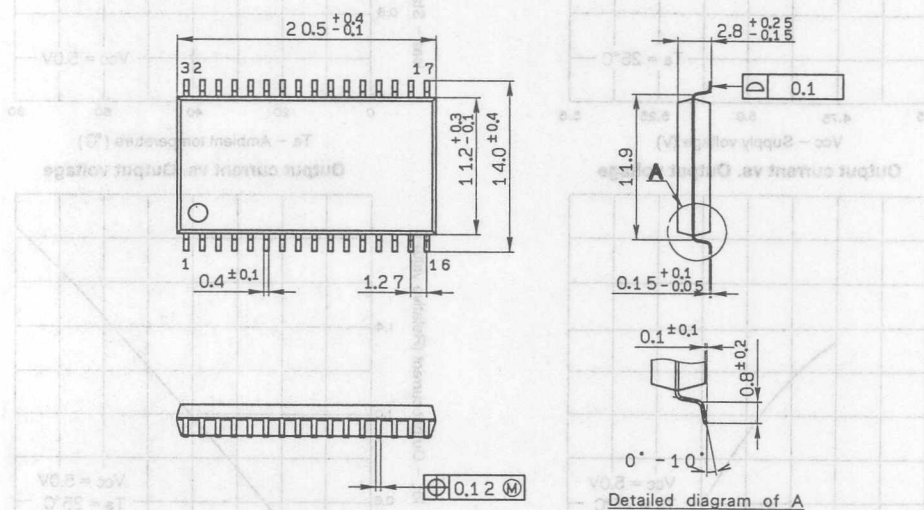


Package Outline Unit : mm

CXK581000P 32pin DIP (Plastic) 600mil 4.5g



CXK581000M 32pin SOP (Plastic) 525mil 1.2g



SONY NAME	SOP-32P-L02
EIAJ NAME	*SOP032-P-0525-A
JEDEC CODE	

SONY® CXK581100TM/YM -10L/12L/15L -10LL/12LL/15LL

131072-word × 8-bit High Speed CMOS Static RAM

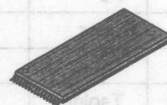
Description

CXK581100TM/YM is a 1M bits, 131072 words by 8 bits, CMOS static RAM. It is suitable for portable and battery back-up systems which require extremely small package and low stand-by current.

Features

- Thin Small-outline Packages of EIAJ standard :
CXK581100TM :
8mm × 20mm 32 pin TSOP
CXK581100YM :
8mm × 20mm 32 pin TSOP (Mirror image pinout)
- Low stand-by current :
L-Version :
100 μ A (Max.) @Vcc=5.5V, Ta=0 to 70 °C
LL-Version :
20 μ A (Max.) @Vcc=5.5V, Ta=0 to 70 °C
- Low voltage data retention : 2.0V (Min.)
- Fast access time : (Access time)
CXK581100TM/YM-10L, -10LL 100ns (Max.)
CXK581100TM/YM-12L, -12LL 120ns (Max.)
CXK581100TM/YM-15L, -15LL 150ns (Max.)
- Single +5V Supply : +5V $\pm$ 10%

CXK581100TM
32 pin TSOP (Plastic)



CXK581100YM
32 pin TSOP (Plastic)



Pin Description

Symbol	Description
A0 to A16	Address input
I/O1 to I/O8	Data input/output
CE1, CE2	Chip enable 1, 2 input
WE	Write enable input
OE	Output enable input
Vcc	+5V power supply
GND	Ground
NC	No connection

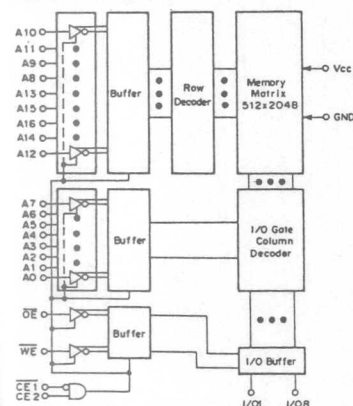
Function

131072-word × 8-bit static RAM

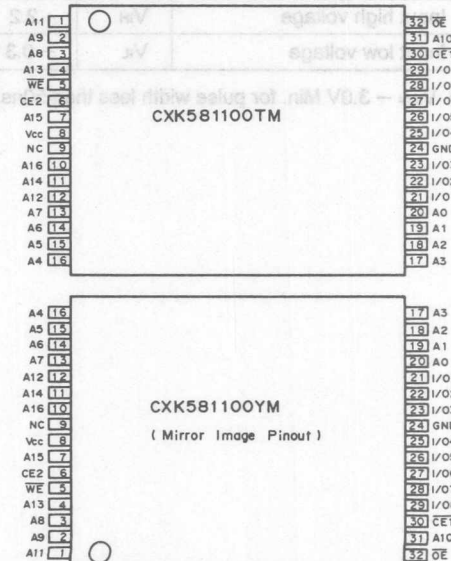
Structure

Silicon gate CMOS IC

Block Diagram



Pin Configuration (Top View)



Absolute Maximum Ratings (Ta=25°C, GND=0V)

Item	Symbol	Rating	Unit
Supply voltage	V _{cc}	- 0.5 * to +7.0	V
Input voltage	V _{in}	- 0.5 * to V _{cc} +0.5	V
Input and output voltage	V _{io}	- 0.5 * to V _{cc} +0.5	V
Allowable power dissipation	P _d	0.7	W
Operating temperature	T _{opr}	0 to +70	°C
Storage temperature	T _{stg}	- 55 to +150	°C
Soldering temperature • time	T _{solder}	235 • 10	°C • sec

* V_{in}, V_{io} = - 3.0V Min. for pulse width less than 50ns.

Truth Table

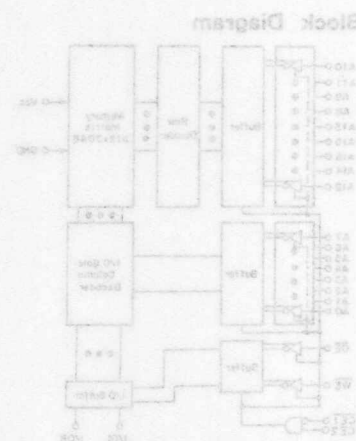
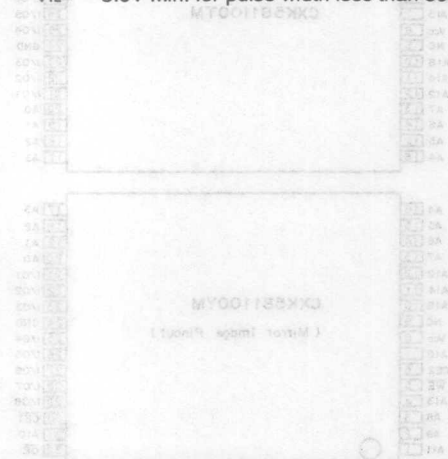
CE1	CE2	OE	WE	Mode	I/O pin	V _{cc} Current
H	X	X	X	Not selected	High Z	I _{SB1} , I _{SB2}
X	L	X	X	Not selected	High Z	I _{SB1} , I _{SB2}
L	H	H	H	Output disable	High Z	I _{cc1} , I _{cc2} , I _{cc3}
L	H	L	H	Read	Data out	I _{cc1} , I _{cc2} , I _{cc3}
L	H	X	L	Write	Data in	I _{cc1} , I _{cc2} , I _{cc3}

X : "H" or "L"

DC Recommended Operating Conditions (Ta=0 to +70°C, GND=0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V _{cc}	4.5	5.0	5.5	V
Input high voltage	V _{IH}	2.2	—	V _{cc} +0.3	V
Input low voltage	V _{IL}	- 0.3 *	—	0.8	V

* V_{IL} = - 3.0V Min. for pulse width less than 50ns.



Electrical Characteristics

• DC characteristics

(V_{CC}=5V ± 10%, GND=0V, T_a=0 to +70 °C)

Item	Symbol	Test conditions		- 10L/12L/15L			- 10LL/12LL/15LL			Unit
				Min.	Typ. *	Max.	Min.	Typ. *	Max.	
Input leakage current	I _{II}	V _{IN} =GND to V _{CC}		- 1	—	1	- 1	—	1	μA
Output leakage current	I _{LO}	CE1=V _{IH} or CE2=V _{IL} or OE=V _{IH} or WE=V _{IL} V _{I/O} =GND to V _{CC}		- 1	—	1	- 1	—	1	μA
Operating power supply current	I _{CC1}	CE1=V _{IL} , CE2=V _{IH} V _{IN} =V _{IH} or V _{IL} I _{OUT} =0mA		—	7	15	—	7	15	mA
Average operating current	I _{CC2}	Min. cycle Duty=100% I _{OUT} =0mA	Write cycle	—	35	60	—	35	60	mA
			Read cycle	—	25	40	—	25	40	
	I _{CC3}	Cycle time 1 μs Duty=100% I _{OUT} =0mA CE1 ≤ 0.2V, CE2 ≥ V _{CC} - 0.2V V _{IL} ≤ 0.2V, V _{IH} ≥ V _{CC} - 0.2V	Write cycle	—	10	20	—	10	20	mA
			Read cycle	—	5	10	—	5	10	
Standby current	I _{SB1}	CE2 ≤ 0.2V or CE1 ≥ V _{CC} - 0.2V or CE2 ≥ V _{CC} - 0.2V	0 to 70 °C	—	—	100	—	—	20	μA
			0 to 40 °C	—	—	20	—	—	4	
			+25 °C	—	2	8	—	0.7	2	
	I _{SB2}	CE1=V _{IH} or CE2=V _{IL}	—	0.6	3	—	0.6	3	mA	
Output high voltage	V _{OH}	I _{OH} = - 1.0mA		2.4	—	—	2.4	—	—	V
Output low voltage	V _{OL}	I _{OL} =2.1mA		—	—	0.4	—	—	0.4	V

* V_{CC}=5V, T_a=25 °C

I/O capacitance

(T_a=25 °C, f=1MHz)

Item	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} =0V	—	—	7	pF
I/O capacitance	C _{I/O}	V _{I/O} =0V	—	—	8	pF

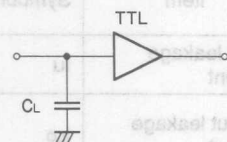
Note) This parameter is sampled and is not 100% tested.

AC characteristics

• AC test conditions ($V_{CC}=5V \pm 10\%$, $T_a=0$ to $+70^\circ C$)

• Test circuit

Item	Conditions
Input pulse high level	$V_{IH}=2.2V$
Input pulse low level	$V_{IL}=0.8V$
Input rise time	$t_r=5ns$
Input fall time	$t_f=5ns$
Input and output reference level	1.5V
Output load conditions	$C_L^* = 100pF, 1TTL$

* C_L includes scope and jig capacitances.

Item	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Input capacitance	C_{in}	$V_{in}=0V$	—	—	7	pF
I/O capacitance	C_{io}	$V_{in}=0V$	—	—	8	pF

Output high voltage	V_{OH}	$I_{OH} = -1.0mA$	2.4	—	2.4	V
Output low voltage	V_{OL}	$I_{OL} = 1.0mA$	0.4	—	0.4	V
Standby current	I_{CCS}	$CET = V_{IH} \text{ or } CET = V_{IL}$	0.6	0.8	0.8	mA
Average operating current	I_{CC}	$V_{IH} \geq V_{CC} - 0.3V$ $V_{IL} \leq 0.3V$ $CES \leq V_{CC} - 0.3V$ $CET \leq 0.3V$ $I_{OH} = 0mA$ $Duty = 100\%$ Cycle time: 1 μs	10	20	—	mA
		Read cycle	5	10	—	mA
		Write cycle	35	40	—	mA
		Min. cycle $Duty = 100\%$ $I_{OH} = 0mA$	35	40	—	mA

* $V_{CC}=5V, T_a=25^\circ C$

I/O capacitance

(Ta=25°C, f=1MHz)

Item	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Input capacitance	C_{in}	$V_{in}=0V$	—	—	7	pF
I/O capacitance	C_{io}	$V_{in}=0V$	—	—	8	pF

(Note) This parameter is sampled and is not 100% tested.

• Read cycle ($\overline{WE}$ ="H")

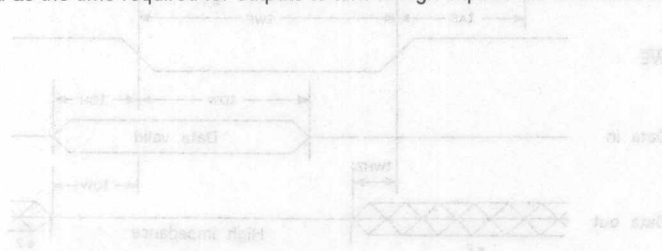
Item	Symbol	- 10L/10LL		- 12L/12LL		- 15L/15LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t_{RC}	100	—	120	—	150	—	ns
Address access time	t_{AA}	—	100	—	120	—	150	ns
Chip enable access time ($\overline{CE1}$)	t_{CO1}	—	100	—	120	—	150	ns
Chip enable access time ($\overline{CE2}$)	t_{CO2}	—	100	—	120	—	150	ns
Output enable to output valid	t_{OE}	—	50	—	60	—	70	ns
Output hold from address change	t_{OH}	15	—	15	—	15	—	ns
Chip enable to output in low Z ($\overline{CE1}$, $\overline{CE2}$)	t_{LZ1} , t_{LZ2}	10	—	10	—	10	—	ns
Output enable to output in low Z ($\overline{OE}$)	t_{OLZ}	5	—	5	—	5	—	ns
Chip disable to output in high Z ($\overline{CE1}$, $\overline{CE2}$)	t_{HZ1}^* , t_{HZ2}^*	—	35	—	40	—	50	ns
Output disable to output in high Z ($\overline{OE}$)	t_{OHZ}^*	—	35	—	40	—	50	ns

* t_{HZ1} , t_{HZ2} and t_{OHZ} are defined as the time required for outputs to turn to high impedance state and are not referred to as output voltage levels.

• Write cycle

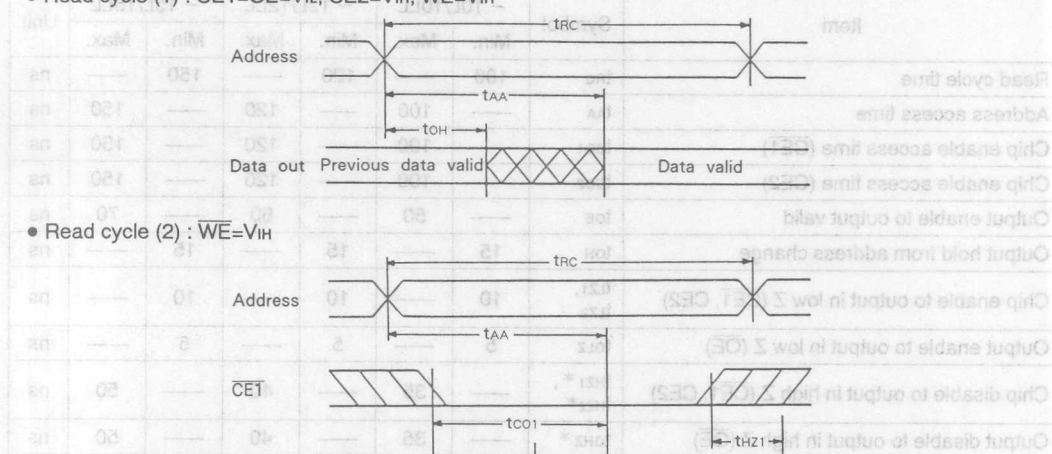
Item	Symbol	- 10L/10LL		- 12L/12LL		- 15L/15LL		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t_{WC}	100	—	120	—	150	—	ns
Address valid to end of write	t_{AW}	70	—	85	—	100	—	ns
Chip enable to end of write	t_{CW}	70	—	85	—	100	—	ns
Data to write time overlap	t_{DW}	40	—	50	—	60	—	ns
Data hold from write time	t_{DH}	0	—	0	—	0	—	ns
Write pulse width	t_{WP}	70	—	80	—	90	—	ns
Address setup time	t_{AS}	0	—	0	—	0	—	ns
Write recovery time ($\overline{WE}$)	t_{WR}	0	—	0	—	0	—	ns
Write recovery time ($\overline{CE1}$, $\overline{CE2}$)	t_{WR1}	0	—	0	—	0	—	ns
Output active from end of write	t_{OW}	10	—	10	—	10	—	ns
Write to output in high Z	t_{WHZ}^*	—	30	—	30	—	30	ns

* t_{WHZ} is defined as the time required for outputs to turn to high impedance state and is not referred to as output voltage level.

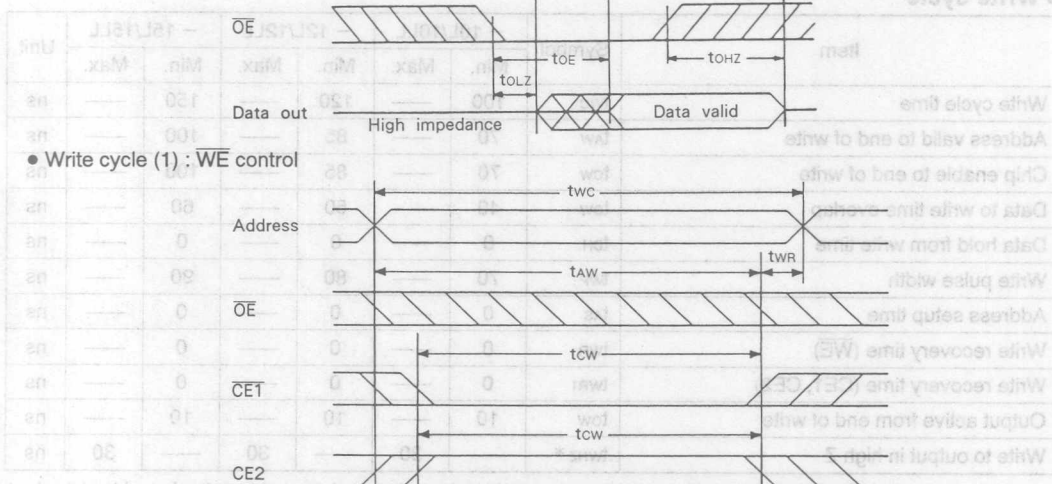
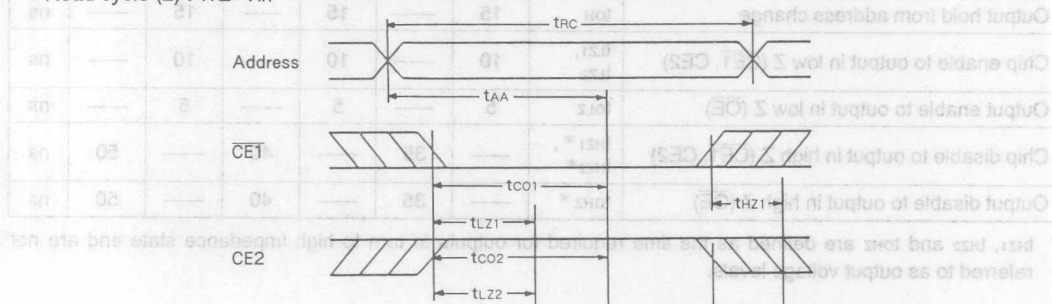


Timing Waveform

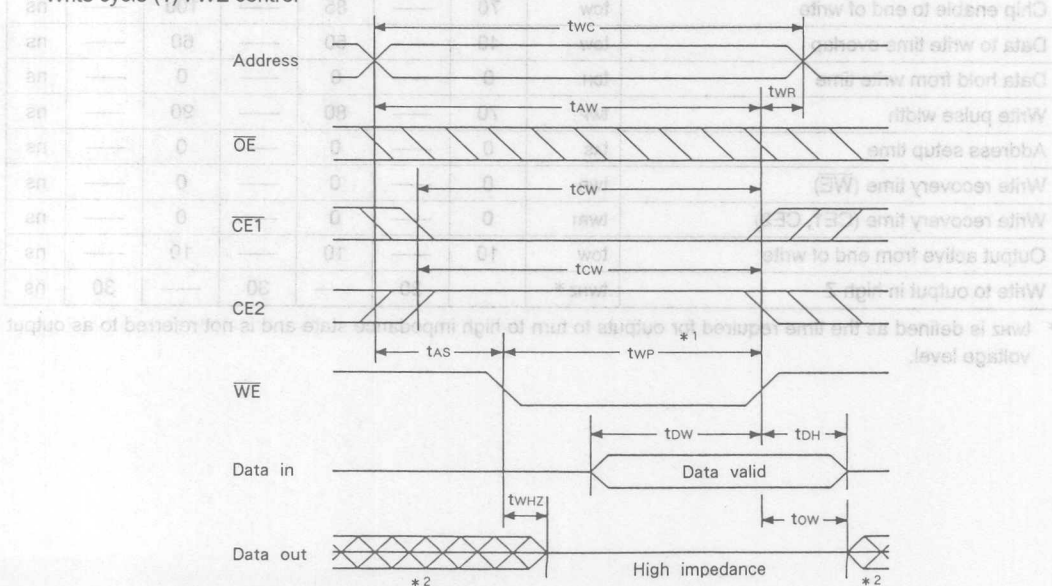
- Read cycle (1) : $\overline{CE1}=\overline{OE}=V_{IL}$, $CE2=V_{IH}$, $\overline{WE}=V_{IH}$



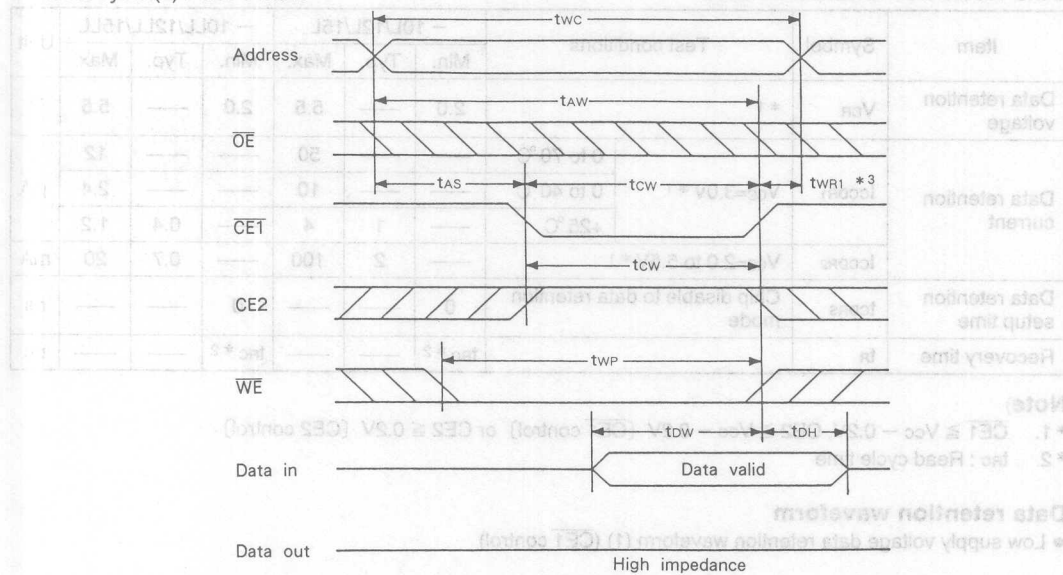
- Read cycle (2) : $\overline{WE}=V_{IH}$



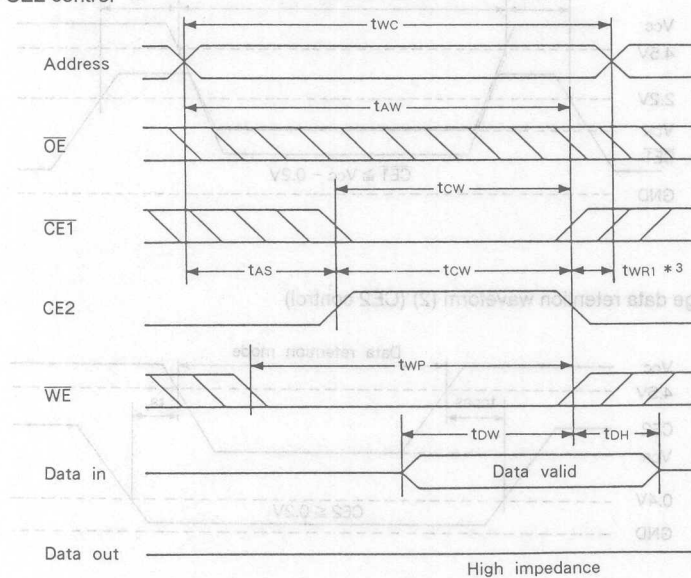
- Write cycle (1) : $\overline{WE}$ control



• Write cycle (2) : $\overline{\text{CE1}}$ control



• Write cycle (3) : CE2 control



Note)

- * 1. Write is executed when both $\overline{\text{CE1}}$ and $\overline{\text{WE}}$ are at low and CE2 is at high simultaneously.
- * 2. Do not apply the data input voltage of the opposite phase to the output while I/O pin is in output condition.
- * 3. twr1 is tested from either the rising edge of CE1 or the falling edge of CE2, whichever comes earlier, until the end of the write cycle.

Parameter	Symbol	Test conditions	T = -40°C			T = 0°C / T = 25°C / T = 55°C			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Data retention voltage	V _{DR}	* 1	2.0	—	5.5	2.0	—	5.5	V
Data retention current	I _{CCDR1}	V _{CC} =3.0V * 1	0 to 70°C	—	50	—	—	12	μA
			0 to 40°C	—	10	—	—	2.4	
			+25°C	—	1	—	0.4	1.2	
	I _{CCDR2}	V _{CC} =2.0 to 5.5V * 1	—	2	100	—	0.7	20	mA
Data retention setup time	t _{CDRS}	Chip disable to data retention mode	0	—	—	0	—	—	ns
Recovery time	t _R		t _{RC} * 2	—	—	t _{RC} * 2	—	—	ns

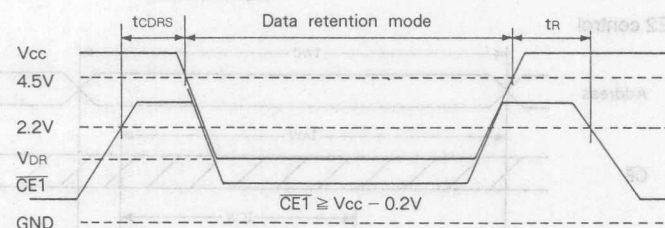
Note)

* 1. $\overline{CE1} \geq V_{CC} - 0.2V$, $CE2 \geq V_{CC} - 0.2V$ ($\overline{CE1}$ control) or $CE2 \leq 0.2V$ ($CE2$ control)

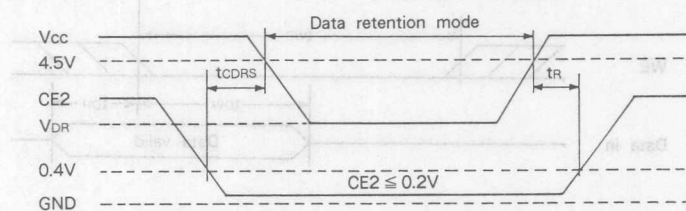
* 2. t_{RC} : Read cycle time

Data retention waveform

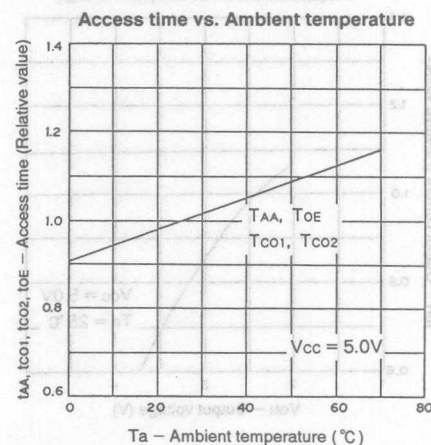
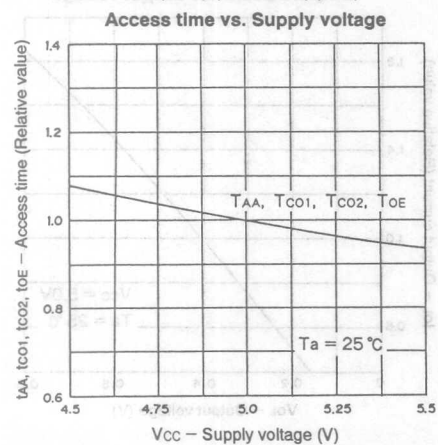
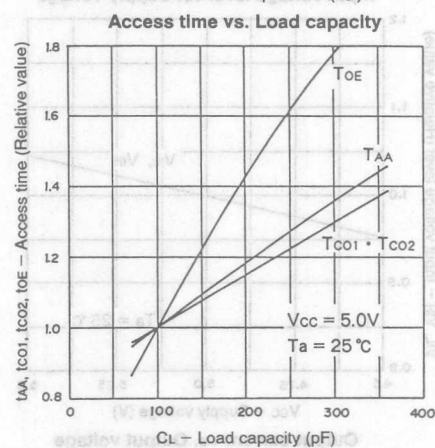
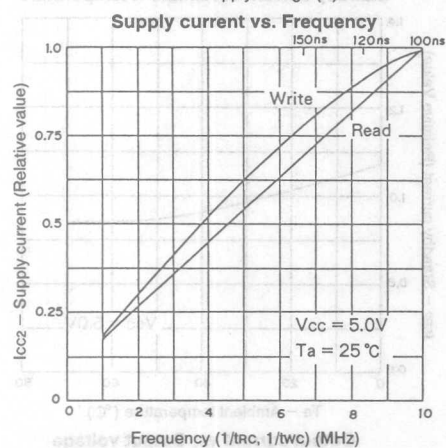
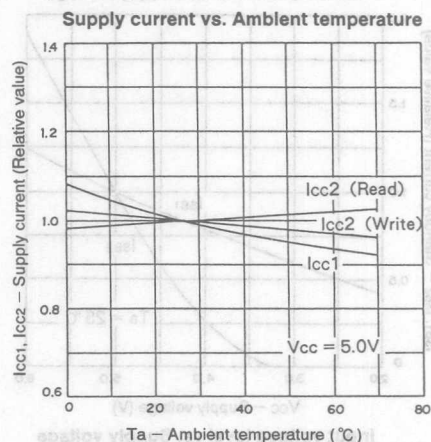
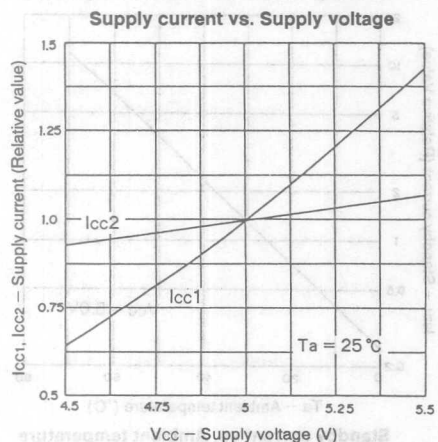
- Low supply voltage data retention waveform (1) ($\overline{CE1}$ control)



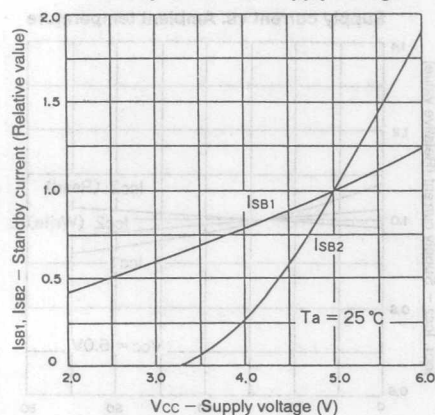
- Low supply voltage data retention waveform (2) ($CE2$ control)



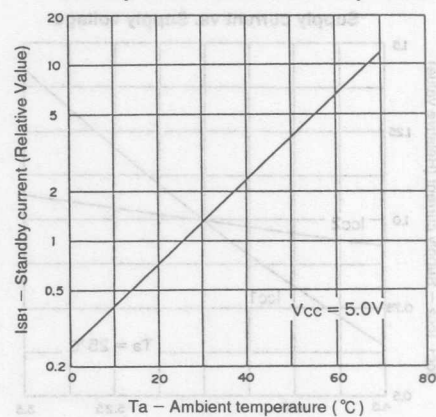
Example of Representative Characteristics



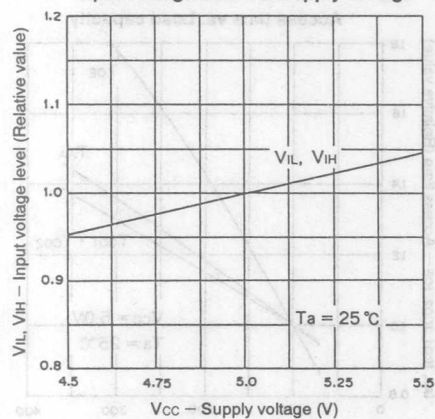
Standby current vs. Supply voltage



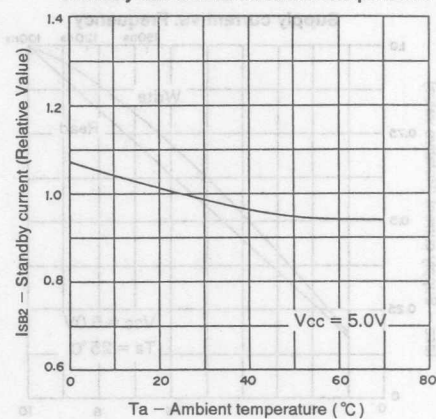
Standby current vs. Ambient temperature



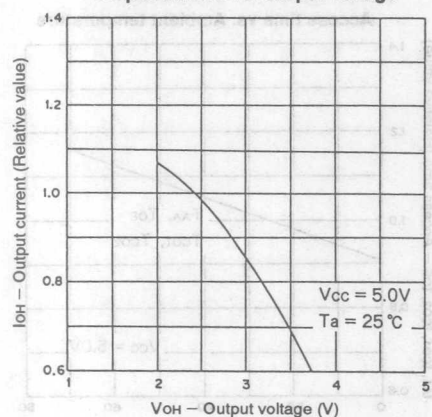
Input voltage level vs. Supply voltage



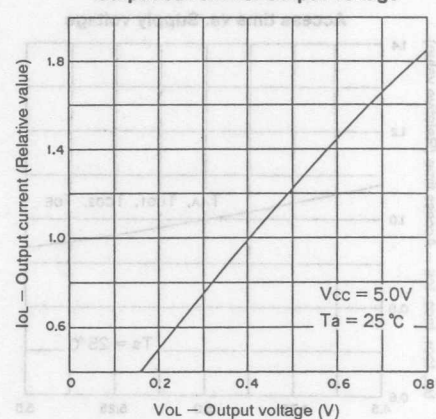
Standby current vs. Ambient temperature



Output current vs. Output voltage



Output current vs. Output voltage

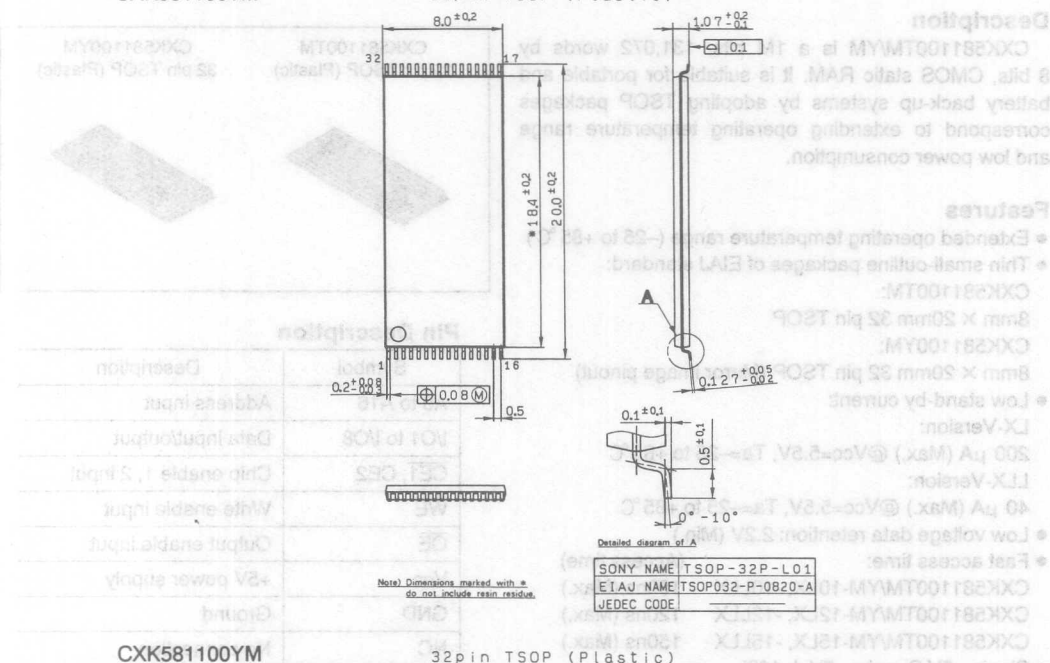


Package Outline

Unit: mm

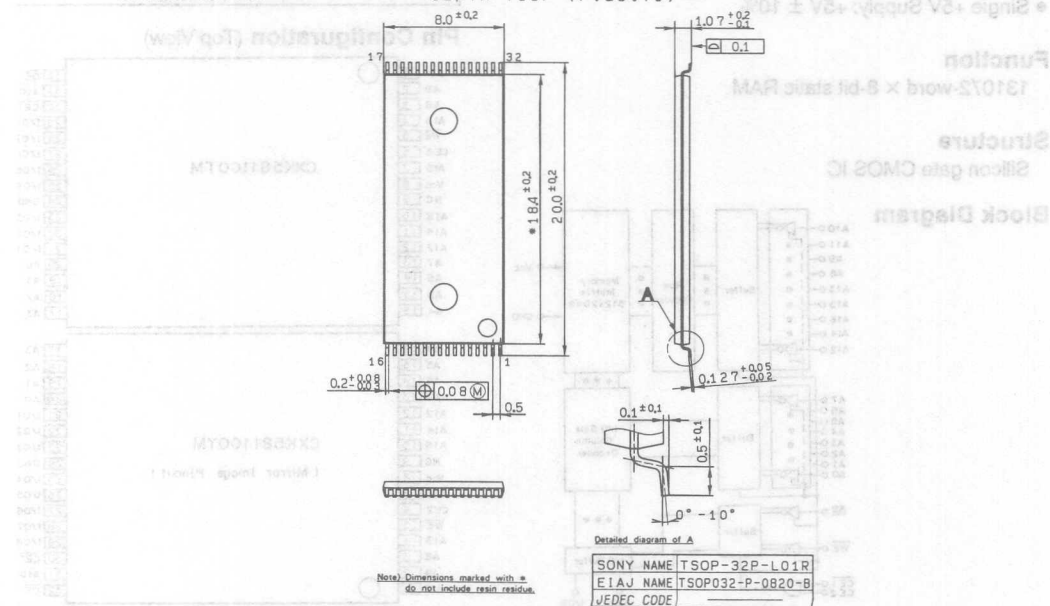
CXK581100TM

32 pin TSOP (Plastic)



CXK581100YM

32 pin TSOP (Plastic)



SONY® CXK581100TM/YM -10LX/12LX/15LX -10LLX/12LLX/15LLX

131072-word × 8-bit High Speed CMOS Static RAM

Description

CXK581100TM/YM is a 1M bits, 131,072 words by 8 bits, CMOS static RAM. It is suitable for portable and battery back-up systems by adopting TSOP packages correspond to extending operating temperature range and low power consumption.

Features

- Extended operating temperature range (-25 to +85 °C)
- Thin small-outline packages of EIAJ standard:
CXK581100TM:
8mm × 20mm 32 pin TSOP
CXK581100YM:
8mm × 20mm 32 pin TSOP (Mirror image pinout)
- Low stand-by current:
LX-Version:
200 μA (Max.) @ Vcc=5.5V, Ta=-25 to +85 °C
LLX-Version:
40 μA (Max.) @ Vcc=5.5V, Ta=-25 to +85 °C
- Low voltage data retention: 2.2V (Min.)
- Fast access time: (Access time)
CXK581100TM/YM-10LX, -10LLX 100ns (Max.)
CXK581100TM/YM-12LX, -12LLX 120ns (Max.)
CXK581100TM/YM-15LX, -15LLX 150ns (Max.)
- Single +5V Supply: +5V ± 10%

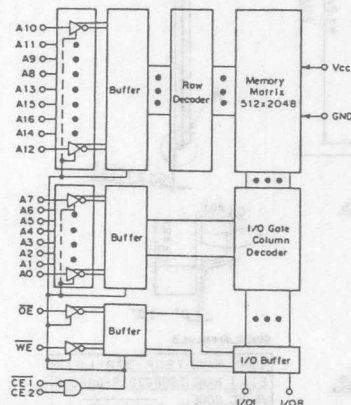
Function

131072-word × 8-bit static RAM

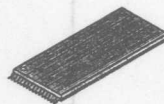
Structure

Silicon gate CMOS IC

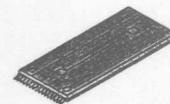
Block Diagram



CXK581100TM
32 pin TSOP (Plastic)



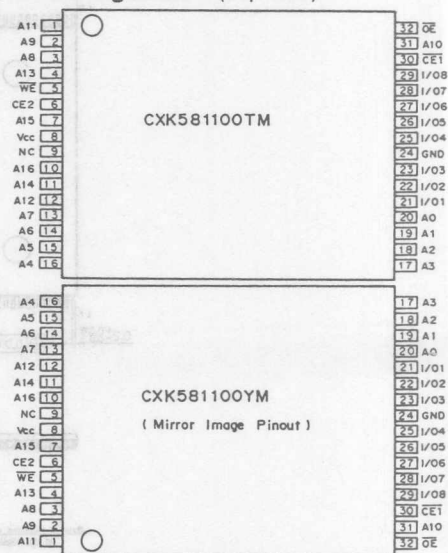
CXK581100YM
32 pin TSOP (Plastic)



Pin Description

Symbol	Description
A0 to A16	Address input
I/O1 to I/O8	Data input/output
CE1, CE2	Chip enable 1, 2 input
WE	Write enable input
OE	Output enable input
Vcc	+5V power supply
GND	Ground
NC	No connection

Pin Configuration (Top View)



Sony reserves the right to change products and specifications without prior notice. This information does not convey any license by any implication or otherwise under any patents or other right. Application circuits shown, if any, are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits.

Absolute Maximum Ratings

(Ta=25°C, GND=0V)

Item	Symbol	Rating	Unit
Supply voltage	Vcc	-0.5 to +7.0	V
Input voltage	V _{IN}	-0.5 * to Vcc+0.5	V
Input and output voltage	V _{IO}	-0.5 * to Vcc+0.5	V
Allowable power dissipation	P _D	0.7	W
Operating temperature	T _{opr}	-25 to +85	°C
Storage temperature	T _{stg}	-55 to +150	°C
Soldering temperature * time	T _{solder}	235 * 10	°C * sec

* V_{IN}, V_{IO}=-3.0V Min. for pulse width less than 50ns.

Truth Table

CE1	CE2	OE	WE	Mode	I/O1 to I/O8	Vcc Current
H	X	X	X	Not selected	High Z	I _{SB1} , I _{SB2}
X	L	X	X	Not selected	High Z	I _{SB1} , I _{SB2}
L	H	H	H	Output disable	High Z	I _{CC1} , I _{CC2} , I _{CC3}
L	H	L	H	Read	Data out	I _{CC1} , I _{CC2} , I _{CC3}
L	H	X	L	Write	Data in	I _{CC1} , I _{CC2} , I _{CC3}

X : "H" or "L"

DC Recommended Operating Conditions

(Ta=-25 to +85°C, GND=0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Vcc	4.5	5.0	5.5	V
Input high voltage	V _{IH}	2.4	—	Vcc+0.3	V
Input low voltage	V _{IL}	-0.3 *	—	0.6	V

* V_{IL}=-3.0V Min. for pulse width less than 50ns.

(Ta=25°C, f=1MHz)

Item	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Input capacitance	C _{in}	V _{IN} =0V	—	—	8	pF
I/O capacitance	C _{IO}	V _{IO} =0V	—	—	8	pF

(Note) This parameter is sampled and is not 100% tested.

Electrical Characteristics

• DC and operating characteristics

(Vcc=5V ± 10%, GND=0V, Ta=-25 to +85 °C)

Item	Symbol	Test conditions	-10LX/12LX/15LX			-10LLX/12LLX/15LLX			Unit	
			Min.	Typ. *	Max.	Min.	Typ. *	Max.		
Input leakage current	I _{LI}	V _{IN} =GND to V _{CC}	-1	—	1	-1	—	1	μA	
Output leakage current	I _{LO}	CE1=V _{IH} or CE2=V _{IL} or OE=V _{IH} or WE=V _{IL} , V _{I/O} =GND to V _{CC}	-1	—	1	-1	—	1	μA	
Operating power supply current	I _{CC1}	CE1=V _{IL} , CE2=V _{IH} , V _{IN} =V _{IH} or V _{IL} I _{OUT} =0mA	—	7	15	—	7	15	mA	
Average operating current	I _{CC2}	Cycle=Min. Duty=100%, I _{OUT} =0mA	Write cycle	—	35	60	—	35	60	mA
			Read cycle	—	25	40	—	25	40	
	I _{CC3}	Cycle time 1 μs Duty=100%, I _{OUT} =0mA CE1 ≤ 0.2V, CE2 ≥ V _{CC} -0.2V V _{IL} ≤ 0.2V, V _{IH} ≥ V _{CC} -0.2V	Write cycle	—	10	20	—	10	20	mA
			Read cycle	—	5	10	—	5	10	
Standby current	I _{SB1}	CE2 ≤ 0.2V or CE1 ≥ V _{CC} -0.2V CE2 ≥ V _{CC} -0.2V	-25 to +85 °C	—	—	200	—	—	40	μA
			-25 to +70 °C	—	—	100	—	—	20	
			-25 to +40 °C	—	—	20	—	—	4	
			+25 °C	—	2	8	—	0.7	2	
	I _{SB2}	CE1=V _{IH} or CE2=V _{IL}	—	0.6	3	—	0.6	3	mA	
Output high voltage	V _{OH}	I _{OH} =-1.0mA	2.4	—	—	2.4	—	—	V	
Output low voltage	V _{OL}	I _{OL} =2.1mA	—	—	0.4	—	—	0.4	V	

* Vcc=5V, Ta=25 °C

I/O Capacitance

(Ta=25 °C, f=1MHz)

Item	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} =0V	—	—	6	pF
I/O capacitance	C _{I/O}	V _{I/O} =0V	—	—	8	pF

Note) This parameter is sampled and is not 100% tested.

• Read cycle ($\overline{WE}$ ="H")

Item	Symbol	-10LX/10LLX		-12LX/12LLX		-15LX/15LLX		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t_{RC}	100	—	120	—	150	—	ns
Address access time	t_{AA}	—	100	—	120	—	150	ns
Chip enable access time ($\overline{CE1}$)	t_{CO1}	—	100	—	120	—	150	ns
Chip enable access time ($\overline{CE2}$)	t_{CO2}	—	100	—	120	—	150	ns
Output enable to output valid	t_{OE}	—	50	—	60	—	70	ns
Output hold from address change	t_{OH}	10	—	10	—	10	—	ns
Chip enable to output in low Z ($\overline{CE1}$, $\overline{CE2}$)	t_{LZ1} , t_{LZ2}	10	—	10	—	10	—	ns
Output enable to output in low Z ($\overline{OE}$)	t_{OLZ}	5	—	5	—	5	—	ns
Chip disable to output in high Z ($\overline{CE1}$, $\overline{CE2}$)	t_{HZ1}^* , t_{HZ2}^*	—	35	—	40	—	50	ns
Chip disable to output in high Z ($\overline{OE}$)	t_{OHZ}^*	—	35	—	40	—	50	ns

* t_{HZ1} , t_{HZ2} and t_{OHZ} are defined as the time required for outputs to turn to high impedance state and are not referred to as output voltage levels.

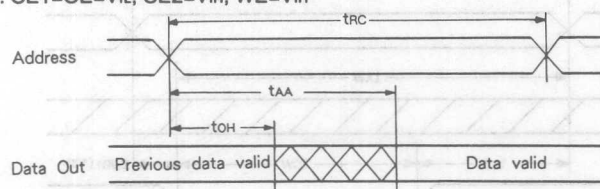
• Write cycle

Item	Symbol	-10LX/10LLX		-12LX/12LLX		-15LX/15LLX		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t_{WC}	100	—	120	—	150	—	ns
Address valid to end of write	t_{AW}	70	—	85	—	100	—	ns
Chip enable to end of write	t_{CW}	70	—	85	—	100	—	ns
Data to write time overlap	t_{DW}	40	—	50	—	60	—	ns
Data hold from write time	t_{DH}	0	—	0	—	0	—	ns
Write pulse width	t_{WP}	70	—	80	—	90	—	ns
Address setup time	t_{AS}	0	—	0	—	0	—	ns
Write recovery time ($\overline{WE}$)	t_{WR}	5	—	5	—	5	—	ns
Write recovery time ($\overline{CE1}$, $\overline{CE2}$)	t_{WR1}	0	—	0	—	0	—	ns
Output active from end of write	t_{OW}	10	—	10	—	10	—	ns
Write to output in high Z	t_{WHZ}^*	—	30	—	30	—	30	ns

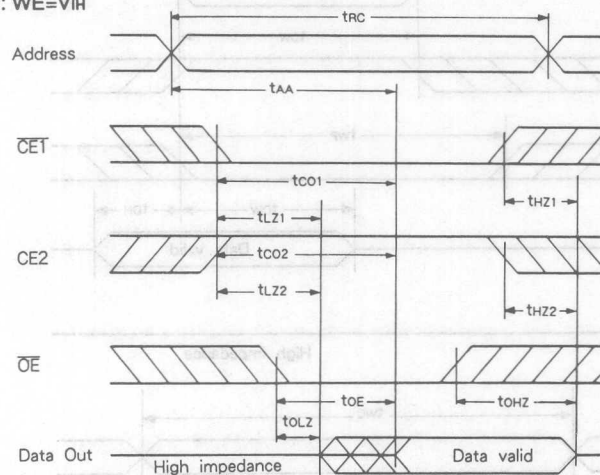
* t_{WHZ} is defined as the time required for outputs to turn to high impedance state and is not referred to as output voltage level.

Timing Waveform

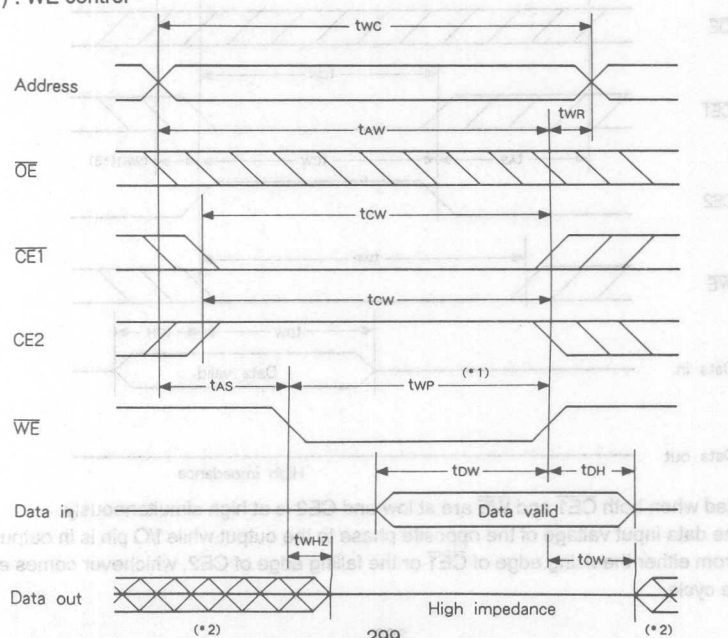
- Read cycle (1) : $\overline{CE1}=\overline{OE}=V_{IL}$, $CE2=V_{IH}$, $\overline{WE}=V_{IH}$



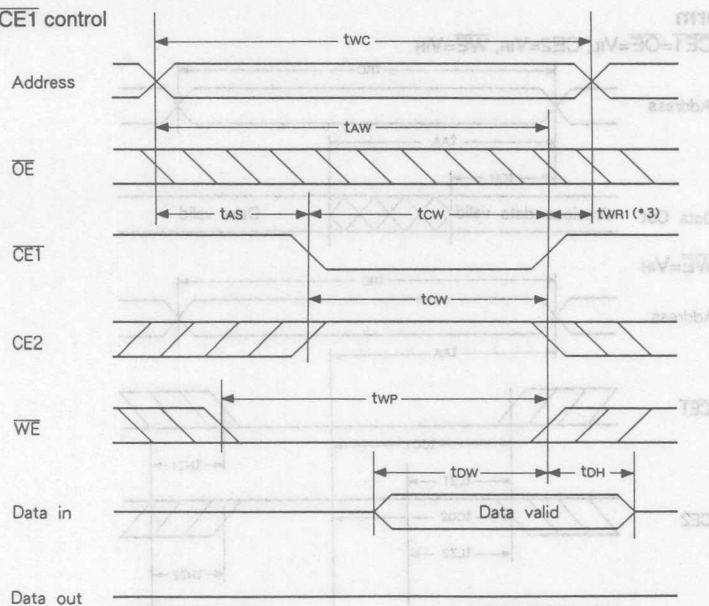
- Read cycle (2) : $\overline{WE}=V_{IH}$



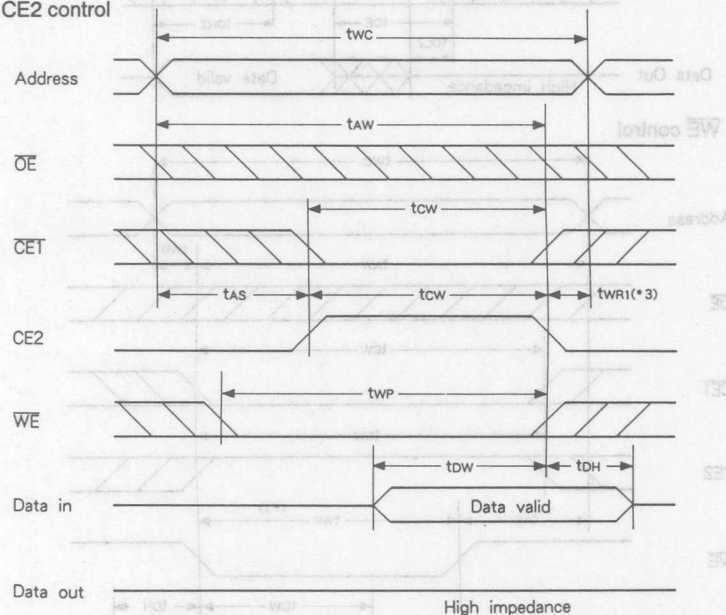
- Write cycle (1) : $\overline{WE}$ control



• Write cycle (2) : $\overline{\text{CE1}}$ control



• Write cycle (3) : CE2 control



- *1. Write is executed when both $\overline{\text{CE1}}$ and $\overline{\text{WE}}$ are at low and CE2 is at high simultaneously.
- *2. Do not apply the data input voltage of the opposite phase to the output while I/O pin is in output condition.
- *3. t_{WR1} is tested from either the rising edge of $\overline{\text{CE1}}$ or the falling edge of CE2, whichever comes earlier, until the end of the write cycle.

Data Retention Characteristics

(Ta = -25 to +85 °C)

Item	Symbol	Test conditions	-10LX/12LX/15LX			-10LLX/12LLX/15LLX			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Data retention voltage	V _{DR}	* 1	2.2	—	5.5	2.2	—	5.5	V
Data retention current	I _{CCDR1}	V _{CC} =3.0V * 1	-25 to +85 °C	—	100	—	—	24	μA
			-25 to +70 °C	—	50	—	—	12	
			-25 to +40 °C	—	10	—	—	2.4	
			+25 °C	—	1	—	0.4	1.2	
	I _{CCDR2}	V _{CC} =2.2 to 5.5V * 1	—	2 * 3	200	—	0.7 * 3	40	μA
Data retention setup time	t _{CDRS}	Chip disable to data retention mode	0	—	—	0	—	—	ns
Recovery time	t _R		t _{RC} * 2	—	—	t _{RC} * 2	—	—	ns

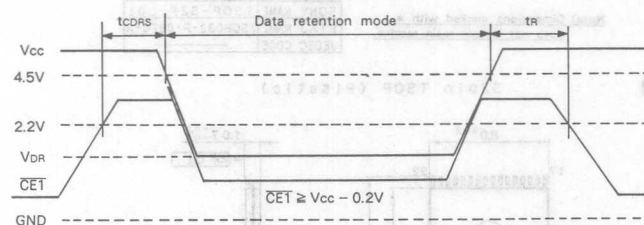
* 1. $\overline{CE1} \geq V_{CC} - 0.2V$, $CE2 \geq V_{CC} - 0.2V$ ($\overline{CE1}$ control) or $CE2 \leq 0.2V$ ($CE2$ control)

* 2. t_{RC}: Read cycle time

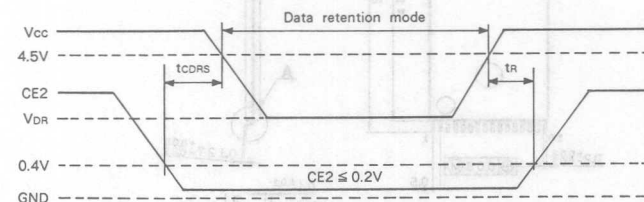
* 3. V_{CC}=5V, Ta=25 °C

Data Retention Waveform

- Low supply voltage data retention waveform (1) : $\overline{CE1}$ control



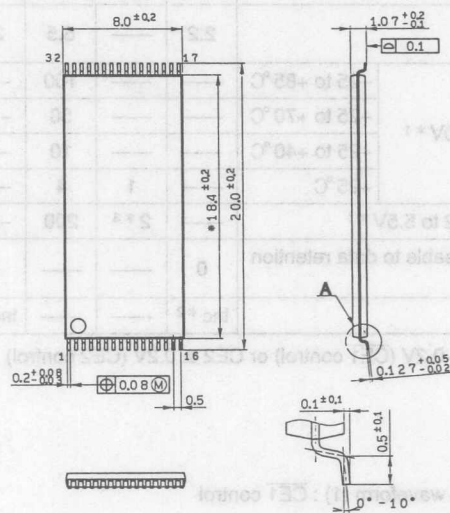
- Low supply voltage data retention waveform (2) : $CE2$ control



Package Outline Unit : mm

CXK581100TM

32pin TSOP (Plastic)



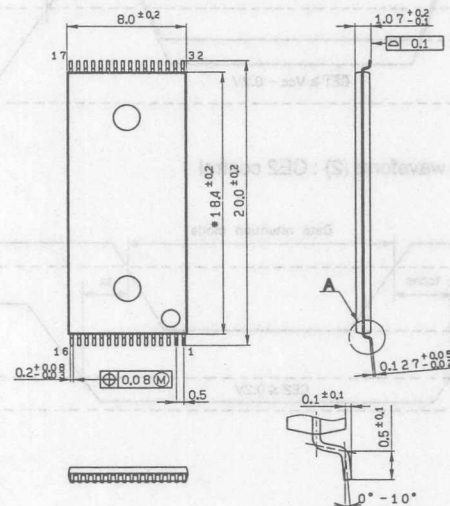
Detailed diagram of A(20/1)

Note) Dimensions marked with *
does not include resin residue.

SONY NAME	TSOP-32P-L01
EIAJ NAME	TSOP032-P-0820-A
JEDEC CODE	

CXK581100YM

32pin TSOP (Plastic)



Detailed diagram of A(20/1)

Note) Dimensions marked with *
does not include resin residue.

SONY NAME	TSOP-32P-L01R
EIAJ NAME	TSOP032-P-0820-B
JEDEC CODE	

SONY

CXK581100TM/YM -12LB

131072-word × 8-bit High Speed CMOS Static RAM

Description

CXK581100TM/YM is a general purpose high speed CMOS static RAM organized as 131,072 words by 8 bits. It is suitable for portable and battery back-up systems by adopting TSOP packages correspond to 2.7 to 5.5V power supply operation and low power consumption.

Features

- Wide supply voltage range operation: 2.7 to 5.5V
- Thin small-outline packages of EIAJ standard:
CXK581100TM:
8mm × 20mm 32 pin TSOP
CXK581100YM:
8mm × 20mm 32 pin TSOP (Mirror image pinout)
- Low power consumption operation:
Standby / DC operation
3V operation; 3 μW (Typ.) / 1.2mW (Typ.)
5V operation; 10 μW (Typ.) / 35mW (Typ.)
- Fast access time: (Access time)
3V operation; 240ns (Max.)
5V operation; 120ns (Max.)
- Low voltage data retention: 2.0V (Min.)

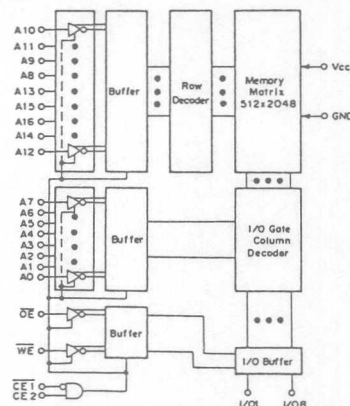
Function

131072-word × 8-bit static RAM

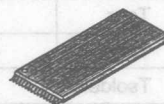
Structure

Silicon gate CMOS IC

Block Diagram



CXK581100TM
32 pin TSOP (Plastic)



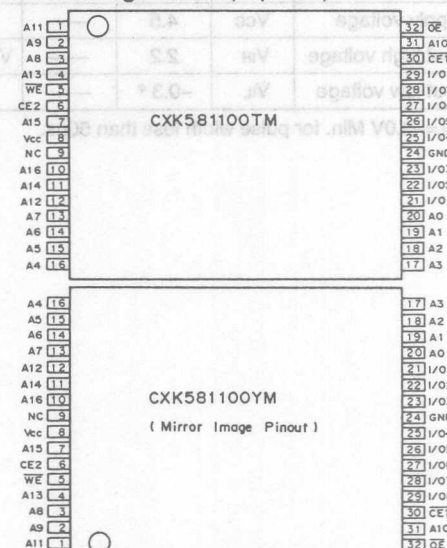
CXK581100YM
32 pin TSOP (Plastic)



Pin Description

Symbol	Description
A0 to A16	Address input
I/O1 to I/O8	Data input/output
CE1, CE2	Chip enable 1, 2 input
WE	Write enable input
OE	Output enable input
Vcc	2.7 to 5.5V power supply
GND	Ground
NC	No connection

Pin Configuration (Top View)



Sony reserves the right to change products and specifications without prior notice. This information does not convey any license by any implication or otherwise under any patents or other right. Application circuits shown, if any, are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits.

Absolute Maximum Ratings (Ta=25 °C, GND=0V)

Item	Symbol	Rating	Unit
Supply voltage	V _{CC}	-0.5 * to +7.0	V
Input voltage	V _{IN}	-0.5 * to V _{CC} +0.5	V
Input and output voltage	V _{I/O}	-0.5 * to V _{CC} +0.5	V
Allowable power dissipation	P _D	0.7	W
Operating temperature	T _{opr}	0 to +70	°C
Storage temperature	T _{stg}	-55 to +150	°C
Soldering temperature • time	T _{solder}	235 • 10	°C • sec

* V_{IN}, V_{I/O} = -3.0V Min. for pulse width less than 50ns.

Truth Table

CE1	CE2	OE	WE	Mode	I/O pin	V _{CC} Current
H	X	X	X	Not selected	High Z	I _{SB1} , I _{SB2}
X	L	X	X	Not selected	High Z	I _{SB1} , I _{SB2}
L	H	H	H	Output disable	High Z	I _{CC1} , I _{CC2} , I _{CC3}
L	H	L	H	Read	Data out	I _{CC1} , I _{CC2} , I _{CC3}
L	H	X	L	Write	Data in	I _{CC1} , I _{CC2} , I _{CC3}

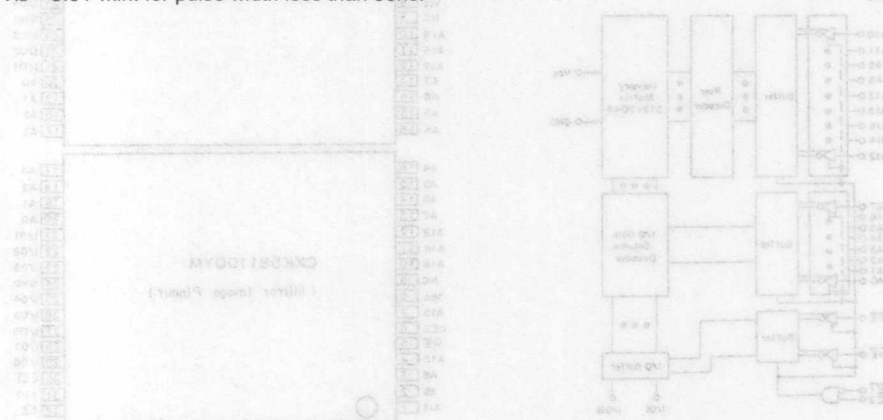
X : "H" or "L"

DC Recommended Operating Conditions

(Ta=0 to +70 °C, GND=0V)

Item	Symbol	V _{CC} =5V ± 10%			V _{CC} =2.7 to 5.5V			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Supply voltage	V _{CC}	4.5	—	5.5	2.7	—	5.5	V
Input high voltage	V _{IH}	2.2	—	V _{CC} +0.3	2.2	—	V _{CC} +0.3	V
Input low voltage	V _{IL}	-0.3 *	—	0.8	-0.3 *	—	0.4	V

* V_{IL} = -3.0V Min. for pulse width less than 50ns.



Electrical Characteristics

• DC characteristics

(GND=0V, Ta=0 to +70°C)

Item	Symbol	Test conditions		Vcc=3V ± 10%			Vcc=5V ± 10%			Unit
				Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Input leakage current	I _{LI}	V _{IN} =GND to V _{CC}		-1	—	1	-1	—	1	μA
Output leakage current	I _{LO}	CE1=V _{IH} or CE2=V _{IL} or OE=V _{IH} or WE=V _{IL} V _{I/O} =GND to V _{CC}		-1	—	1	-1	—	1	μA
Operating power supply current	I _{CC1}	CE1=V _{IL} , CE2=V _{IH} V _{IN} =V _{IH} or V _{IL} I _{OUT} =0mA		—	0.4	0.8	—	7	15	mA
Average operating current	I _{CC2}	Min. cycle Duty=100% I _{OUT} =0mA	Write cycle	—	10	15	—	35	60	mA
			Read cycle	—	10	15	—	25	40	
	I _{CC3}	Cycle time 1 μs Duty=100% I _{OUT} =0mA CE1 ≤ 0.2V, CE2 ≥ V _{CC} -0.2V V _{IL} ≤ 0.2V, V _{IH} ≥ V _{CC} -0.2V	Write cycle	—	5	10	—	10	20	mA
			Read cycle	—	2.5	5	—	5	10	
Standby current	I _{SB1}	CE2 ≤ 0.2V or CE1 ≥ V _{CC} -0.2V or CE2 ≥ V _{CC} -0.2V	0 to +70℃	—	—	60	—	—	100	μA
			0 to +40℃	—	—	12	—	—	20	
			+25℃	—	1.2	5	—	2	8	
	I _{SB2}	CE1=V _{IH} or CE2=V _{IL}	—	0.06	0.3	—	0.6	3	mA	
Output high voltage	V _{OH}	I _{OH} =-1.0mA		2.2	—	—	2.4	—	—	V
Output low voltage	V _{OL}	I _{OL} =2.1mA		—	—	0.4	—	—	0.4	V

* Ta=25°C

I/O Capacitance

(Ta=25°C, f=1MHz)

Item	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} =0V	—	—	7	pF
I/O capacitance	C _{I/O}	V _{I/O} =0V	—	—	8	pF

Note) This parameter is sampled and is not 100% tested.

AC Characteristics

● AC test conditions

(Vcc=2.7 to 5.5V, Ta=0 to +70°C)

Item	Conditions	
	Vcc=3V	Vcc=5V
Input pulse high level	V _{IH} =2.2V	V _{IH} =2.2V
Input pulse low level	V _{IL} =0.4V	V _{IL} =0.8V
Input rise time	tr=5ns	tr=5ns
Input fall time	tf=5ns	tf=5ns
Input and output reference level	1.5V	1.5V
Output load conditions	C _L *=100pF, 1TTL	C _L *=100pF, 1TTL

* C_L includes scope and jig capacitances.

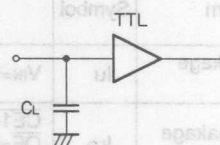
mA	40	25	—	15	10	—	Read cycle	Min. cycle Duty=100%	less	Averaging operating current
mA	30	10	—	10	5	—	Write cycle	Cycle time 1 μs Duty=100%	less	Averaging operating current
mA	10	5	—	5	2.5	—	Read cycle	V _{IH} ≤ Vcc-0.2V V _{IL} ≤ 0.2V C _{ES} ≤ Vcc-0.2V C _{EF} ≤ 0.2V I _{out} ≤ 0mA	less	Averaging operating current
mA	100	—	—	50	—	—	0 to +70°C	C _{ES} ≤ 0.2V C _{EF} ≤ Vcc-0.2V 0 to +40°C	less	Standby current
mA	20	—	—	15	—	—	0 to +40°C	C _{ES} ≤ Vcc-0.2V 0 to +25°C	less	Standby current
mA	8	3	—	5	1.5	—	+25°C	C _{ES} ≤ Vcc-0.2V	less	Standby current
mA	0.8	—	—	0.5	0.05	—	—	C _{ES} ≤ V _{IH} or C _{ES} ≤ V _{IL}	less	Standby current
V	—	—	—	2.5	—	—	—	I _{OH} =-1.0mA	V _{OH}	Output high voltage
V	0.4	—	—	0.4	—	—	—	I _{OL} =2.1mA	V _{OL}	Output low voltage

* Ta=25°C

(Ta=25°C, f=1MHz)

Item	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Input capacitance	C _{in}	V _{in} =0V	—	—	7	pF
I/O capacitance	C _{io}	V _{io} =0V	—	—	8	pF

(Note) This parameter is sampled and is not 100% tested.



• Read cycle ($\overline{WE}$ ="H")

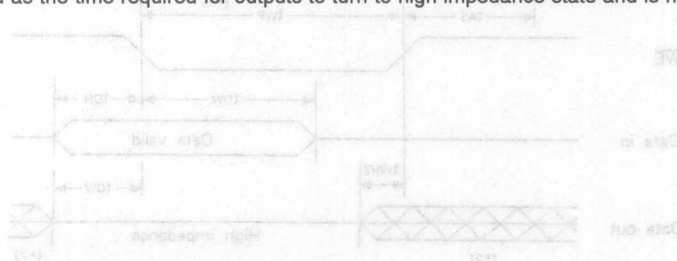
Item	Symbol	Vcc=3V ± 10%		Vcc=5V ± 10%		Unit
		Min.	Max.	Min.	Max.	
Read cycle time	t _{RC}	240	—	120	—	ns
Address access time	t _{AA}	—	240	—	120	ns
Chip enable access time ($\overline{CE1}$)	t _{CO1}	—	240	—	120	ns
Chip enable access time (CE2)	t _{CO2}	—	240	—	120	ns
Output enable to output valid	t _{OE}	—	120	—	60	ns
Output hold from address change	t _{OH}	30	—	15	—	ns
Chip enable to output in low Z ($\overline{CE1}$, CE2)	t _{LZ1} , t _{LZ2}	20	—	10	—	ns
Output enable to output in low Z ($\overline{OE}$)	t _{OLZ}	10	—	5	—	ns
Chip disable to output in high Z ($\overline{CE1}$, CE2)	t _{HZ1} *, t _{HZ2} *	—	80	—	40	ns
Output disable to output in high Z ($\overline{OE}$)	t _{OHZ} *	—	80	—	40	ns

* t_{HZ1}, t_{HZ2} and t_{OHZ} are defined as the time required for outputs to turn to high impedance state and are not referred to as output voltage levels.

• Write cycle

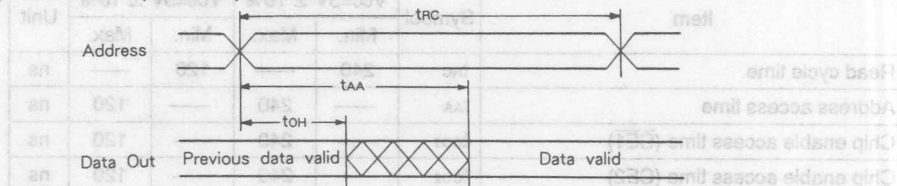
Item	Symbol	Vcc=3V ± 10%		Vcc=5V ± 10%		Unit
		Min.	Max.	Min.	Max.	
Write cycle time	t _{WC}	240	—	120	—	ns
Address valid to end of write	t _{AW}	170	—	85	—	ns
Chip enable to end of write	t _{CW}	170	—	85	—	ns
Data to write time overlap	t _{DW}	100	—	50	—	ns
Data hold from write time	t _{DH}	0	—	0	—	ns
Write pulse width	t _{WP}	160	—	80	—	ns
Address setup time	t _{AS}	0	—	0	—	ns
Write recovery time ($\overline{WE}$)	t _{WR}	0	—	0	—	ns
Write recovery time ($\overline{CE1}$, CE2)	t _{WR1}	0	—	0	—	ns
Output active from end of write	t _{OW}	20	—	10	—	ns
Write to output in high Z	t _{WHZ} *	—	60	—	30	ns

* t_{WHZ} is defined as the time required for outputs to turn to high impedance state and is not referred to as output voltage level.

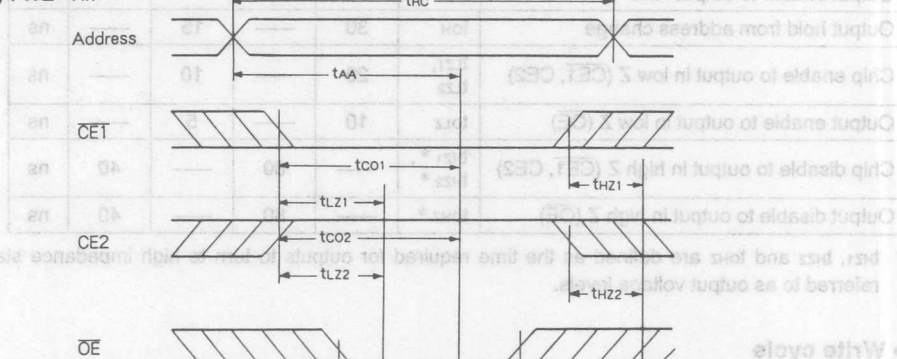


Timing Waveform

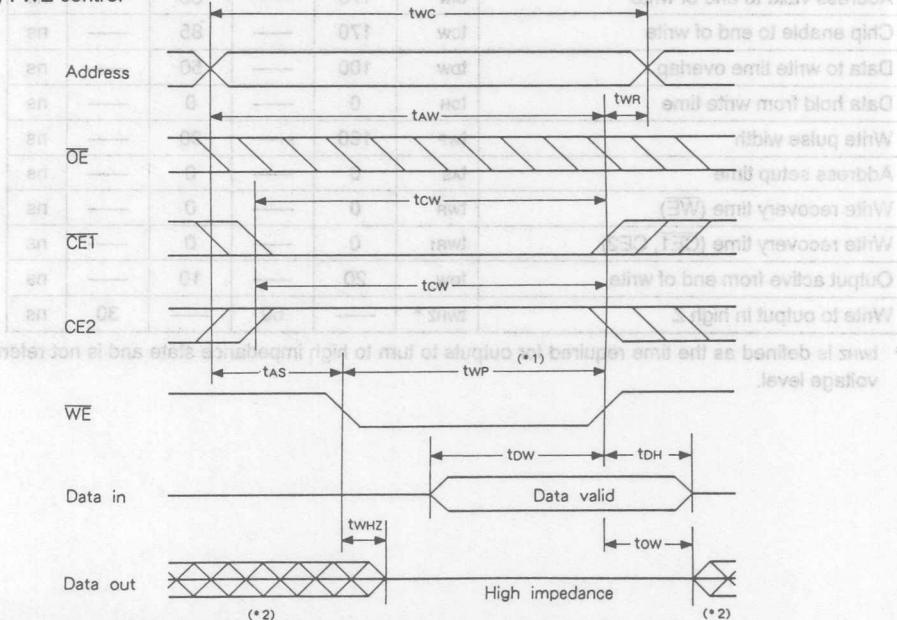
- Read cycle (1) : $\overline{CE1}=\overline{OE}=V_{IL}$, $CE2=V_{IH}$, $WE=V_{IH}$



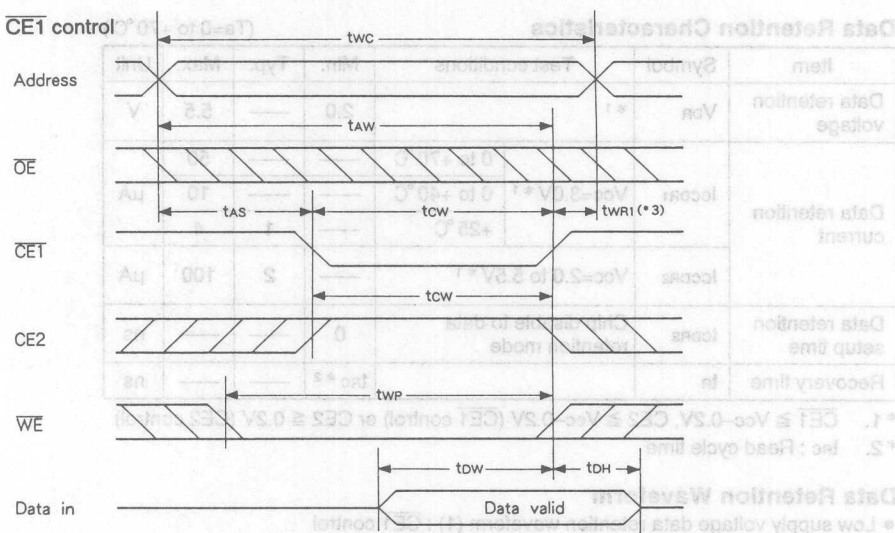
- Read cycle (2) : $WE=V_{IH}$



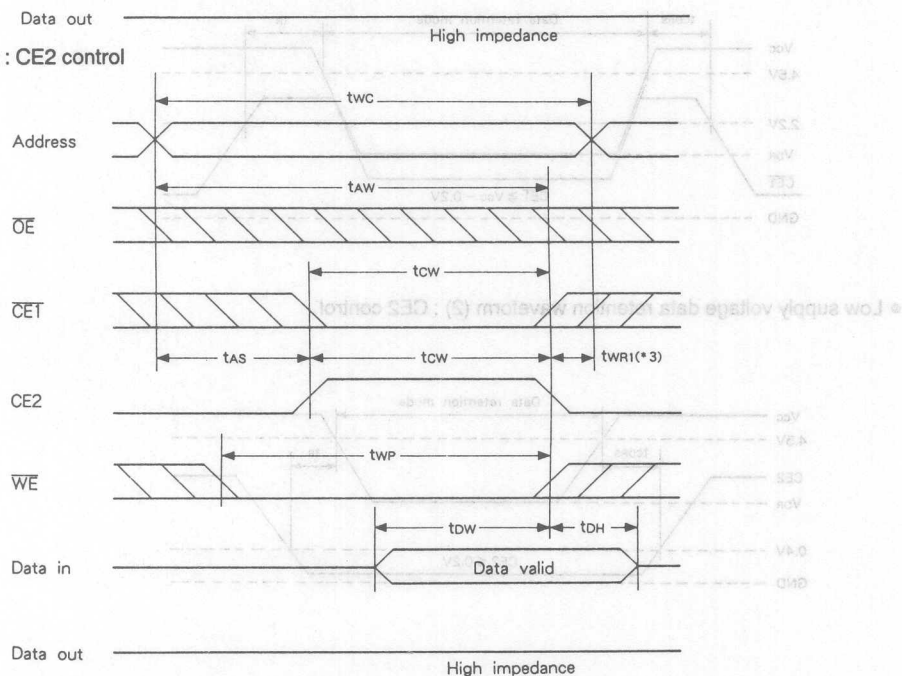
- Write cycle (1) : WE control



• Write cycle (2) : $\overline{\text{CE1}}$ control



• Write cycle (3) : CE2 control



- * 1. Write is executed when both $\overline{\text{CE1}}$ and $\overline{\text{WE}}$ are at low and CE2 is at high simultaneously.
- * 2. Do not apply the data input voltage of the opposite phase to the output while I/O pin is in output condition.
- * 3. t_{WR1} is tested from either the rising edge of $\overline{\text{CE1}}$ or the falling edge of CE2, whichever comes earlier, until the end of the write cycle.

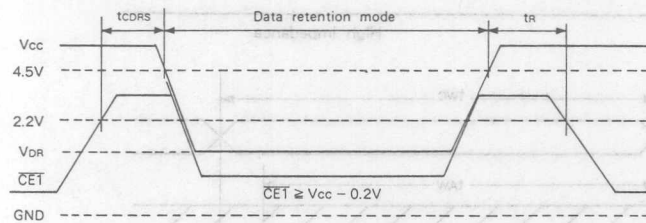
Item	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Data retention voltage	V _{DR}	* 1	2.0	—	5.5	V
Data retention current	I _{CCDR1}	V _{CC} =3.0V * 1	—	—	50	μA
		0 to +70 °C	—	—	10	
		+25 °C	—	1	4	
	I _{CCDR2}	V _{CC} =2.0 to 5.5V * 1	—	2	100	μA
Data retention setup time	t _{CDRS}	Chip disable to data retention mode	0	—	—	ns
Recovery time	t _R		t _{RC} * 2	—	—	ns

* 1. $\overline{CE1} \geq V_{CC}-0.2V$, $CE2 \geq V_{CC}-0.2V$ ($\overline{CE1}$ control) or $CE2 \leq 0.2V$ ($CE2$ control)

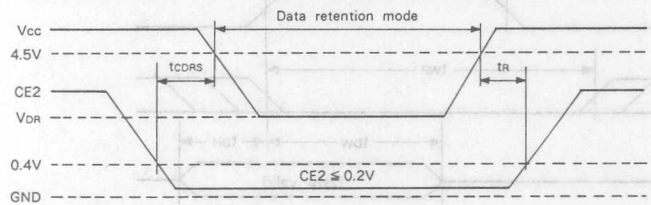
* 2. t_{RC} : Read cycle time

Data Retention Waveform

- Low supply voltage data retention waveform (1) : $\overline{CE1}$ control

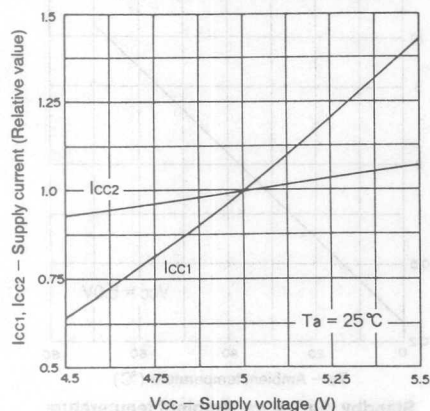


- Low supply voltage data retention waveform (2) : $CE2$ control

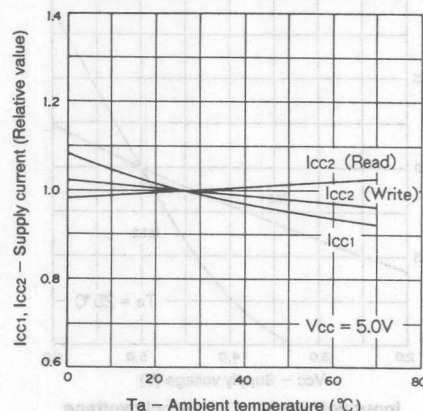


Example of Representative Characteristics

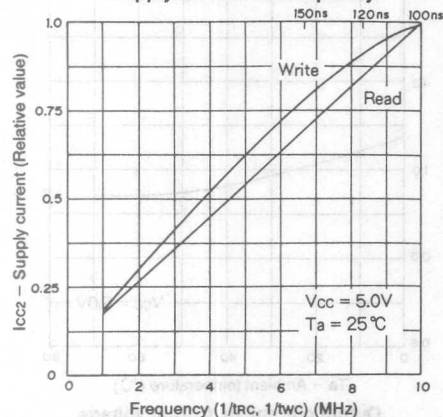
Supply current vs. Supply voltage



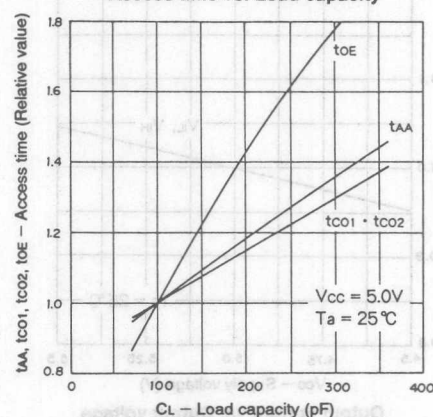
Supply current vs. Ambient temperature



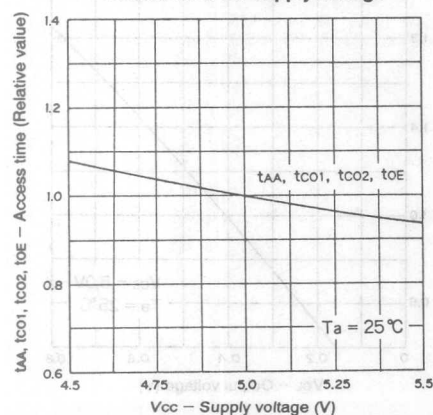
Supply current vs. Frequency



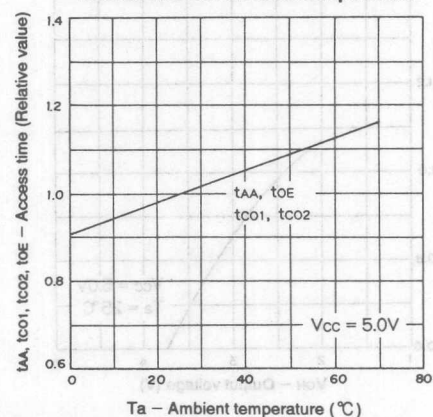
Access time vs. Load capacity



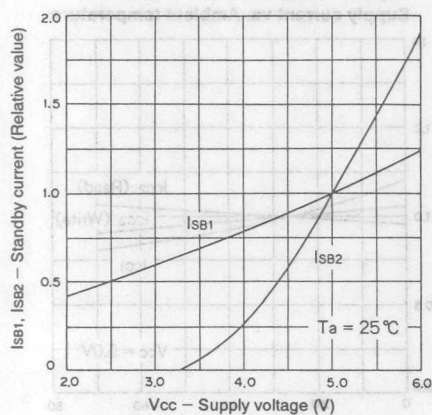
Access time vs. Supply voltage



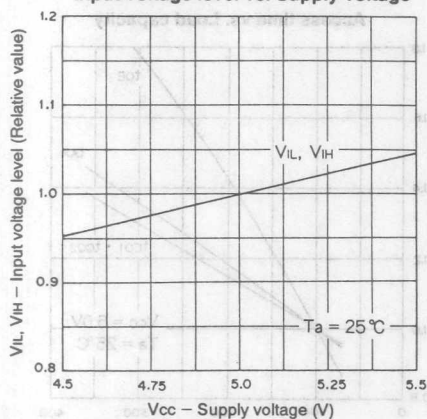
Access time vs. Ambient temperature



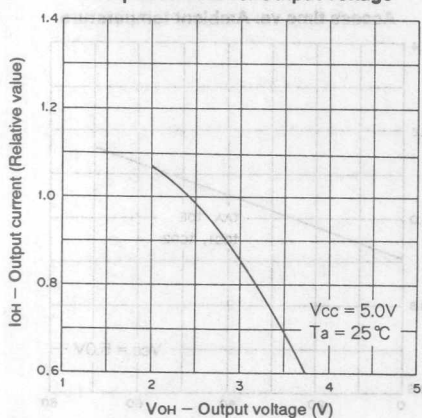
Standby current vs. Supply voltage



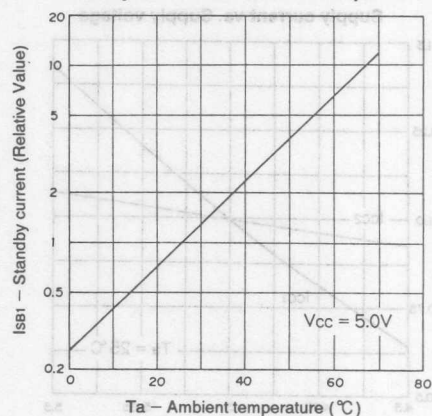
Input voltage level vs. Supply voltage



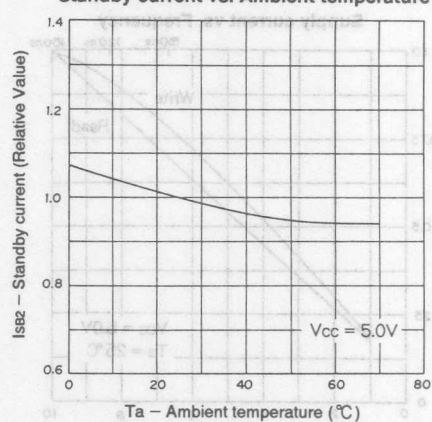
Output current vs. Output voltage



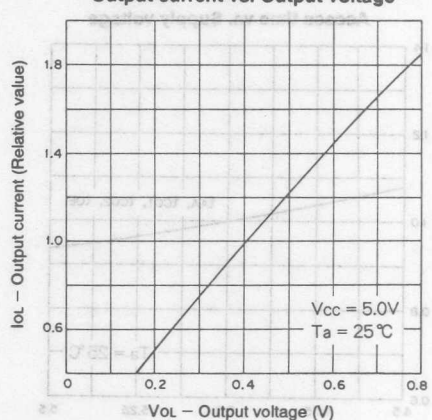
Standby current vs. Ambient temperature



Standby current vs. Ambient temperature

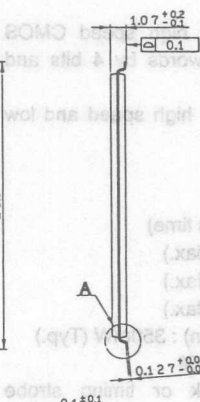


Output current vs. Output voltage



Unit : mm

32pin TSOP (Plastic)

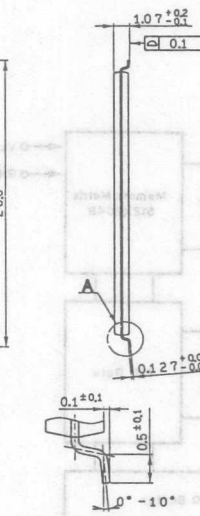


Detailed diagram of A(20/1)

Note) Dimensions marked with *
does not include resin residue.

SONY NAME	TSOP-32P-L01
EIAJ NAME	TSOP032-P-0820-A
JEDEC CODE	_____

32pin TSOP (Plastic)



Detailed diagram of A(20/1)

Note) Dimensions marked with *
does not include resin residue

SONY NAME	TSOP-32P-L018
EIAJ NAME	TSOP032-P-0820-
JDEC CODE	_____

262144-word × 4-bit High Speed CMOS Static RAM Preliminary

Description

CXK541000J is a 1048576 bits high speed CMOS static RAM organized as 262144 words by 4 bits and operates from a single 5V supply.

This device is suitable for use in high speed and low power applications.

Features

- Fast access time (Access time)
CXK541000J-25 25ns (Max.)
CXK541000J-30 30ns (Max.)
CXK541000J-35 35ns (Max.)
- Low power consumption (operation) : 350mW (Typ.)
- Single +5V power supply: 5V ± 10%
- Fully static memory No clock or timing strobe required.
- Equal access and cycle time.
- Separated data input and output: three-state output
- Directly TTL compatible: All inputs and outputs
- High density: 400 mil 32 pin SOJ plastic package

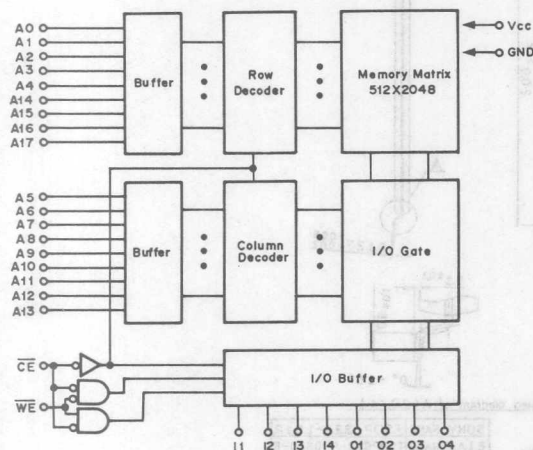
Function

262144-word × 4-bit static RAM

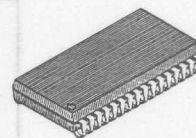
Structure

Silicon gate CMOS IC

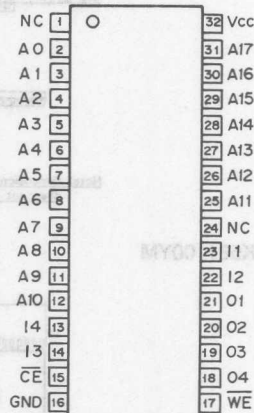
Block Diagram



32 pin SOJ (Plastic)



Pin Configuration (Top View)



Pin Description

Symbol	Description
A0 to A17	Address input
I1 to I4	Data input
O1 to O4	Data output
CE	Chip enable input
WE	Write enable input
Vcc	+5V Power supply
GND	Ground
NC	No connection

Sony reserves the right to change products and specifications without prior notice. This information does not convey any license by any implication or otherwise under any patents or other right. Application circuits shown, if any, are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits.

Absolute Maximum Ratings

(Ta=25°C, GND=0V)

Item	Symbol	Rating	Unit
Supply voltage	V _{CC}	-0.5 * to +7.0	V
Input voltage	V _{IN}	-0.5 * to V _{CC} +0.5	V
Input and output voltage	V _{I/O}	-0.5 * to V _{CC} +0.5	V
Allowable power dissipation	P _D	1.0	W
Operating temperature	T _{opr}	-10 to +85	°C
Storage temperature	T _{stg}	-55 to +150	°C
Soldering temperature*time	T _{solder}	260*10	°C*sec

* V_{CC}, V_{IN}, V_{I/O}=+7.5V Max. for pulse width less than 10ns.V_{CC}, V_{IN}, V_{I/O}=-3.5V Min. for pulse width less than 10ns.

Truth Table

CE	WE	Mode	Data Output	V _{CC} Current
H	X	Not selected	High Z	I _{SB1} , I _{SB2}
L	H	Read	Data out	I _{CC}
L	L	Write	High Z	I _{CC}

X : "H" or "L"

DC Recommended Operating Conditions

(Ta=0 to +70°C, GND=0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Input high voltage	V _{IH}	2.2	—	V _{CC} +0.5	V
Input low voltage	V _{IL}	-0.5 *	—	0.8	V
Input rise time	t _r	—	5	100	ns
Input fall time	t _f	—	5	100	ns

* V_{IH}=+7.0V Max. for pulse width less than 10ns.V_{IL}=-3.0V Min. for pulse width less than 10ns.

Electrical Characteristics

● DC and operating characteristics

(Vcc=5V ± 10%, GND=0V, Ta=0 to +70 °C)

Item	Symbol	Test conditions	Min.	Typ.*	Max.	Unit
Input leak current	I _{LI}	V _{IN} =GND to V _{CC} V _{CC} =5.5V	-1	—	1	μA
Output leak current	I _{LO}	$\overline{CE}=V_{IH}$ or $\overline{WE}=V_{IL}$ V _{OUT} =GND to V _{CC}	-1	—	1	μA
Average operating current	I _{CC}	Cycle=Min, Duty=100% I _{OUT} =0mA	—	70	120	mA
Standby current	I _{SB1}	$\overline{CE} \geq V_{CC}-0.2V$, V _{IN} ≥ V _{CC} -0.2V or V _{IN} ≤ 0.2V	—	—	2	mA
	I _{SB2}	$\overline{CE}=V_{IH}$, V _{IN} =V _{IH} /V _{IL} , min. cycle	—	15	30	mA
Output high voltage	V _{OH}	I _{OH} =-4.0mA	2.4	—	—	V
Output low voltage	V _{OL}	I _{OL} =8.0mA	—	—	0.4	V

* Vcc=5V, Ta=25 °C

I/O capacitance

(Ta=25 °C, f=1MHz)

Item	Symbol	Test conditions	Min.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} =0V	—	6	pF
Output capacitance	C _{OUT}	V _{OUT} =0V	—	10	pF

(Note) This parameter is sampled and is not 100% tested.

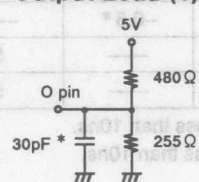
AC characteristics

● AC test conditions

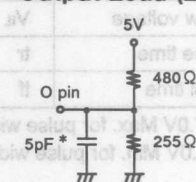
(Vcc=5V ± 10%, Ta=0 to +70 °C)

Item	Conditions
Input pulse high level	V _{IH} =3.0V
Input pulse low level	V _{IL} =0V
Input rise time	t _r =5ns
Input fall time	t _f =5ns
Input and output reference level	1.5V
Output load conditions	Fig. 1

Output Load (1)



Output Load (2)**



* including scope and jig

** for t_{LZ}, t_{HZ}, t_{OW}, t_{WHZ}

Fig. 1

• Read cycle

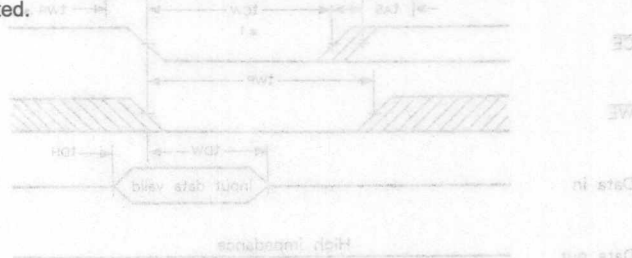
Item	Symbol	-25		-30		-35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t _{RC}	25	—	30	—	35	—	ns
Address access time	t _{AA}	—	25	—	30	—	35	ns
Chip enable access time ($\overline{\text{CE}}$)	t _{CO}	—	25	—	30	—	35	ns
Output hold from address change	t _{OH}	5	—	5	—	5	—	ns
Chip enable to output in low Z ($\overline{\text{CE}}$)	t _{LZ} *	5	—	5	—	5	—	ns
Chip disable to output in high Z	t _{HZ} *	0	15	0	15	0	15	ns
Chip enable to power up time	t _{PU}	0	—	0	—	0	—	ns
Chip disable to power down time	t _{PD}	—	25	—	30	—	35	ns

* Transition is measured $\pm 200\text{mV}$ from steady voltage with specified loading in Fig. 1. This parameter is sampled and is not 100% tested.

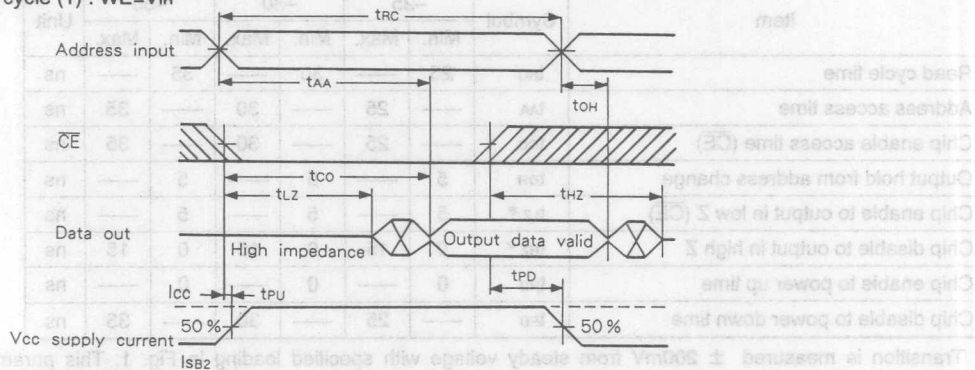
• Write cycle

Item	Symbol	-25		-30		-35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t _{WC}	25	—	30	—	35	—	ns
Address valid to end of write	t _{AW}	18	—	20	—	20	—	ns
Chip enable to end of write	t _{CW}	18	—	20	—	20	—	ns
Data to write time overlap	t _{DW}	12	—	15	—	15	—	ns
Data hold from write time	t _{DH}	0	—	0	—	0	—	ns
Write pulse width	t _{WP}	15	—	18	—	18	—	ns
Address set up time	t _{AS}	0	—	0	—	0	—	ns
Write recovery time	t _{WR}	2	—	2	—	2	—	ns
Output active from end of write	t _{OW} *	5	—	5	—	5	—	ns
Write to output in high Z	t _{WHZ} *	0	15	0	15	0	15	ns

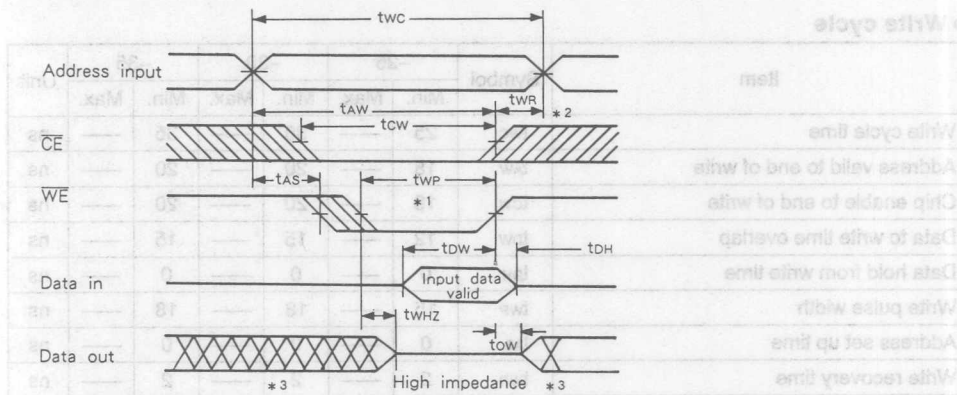
* Transition is measured $\pm 200\text{mV}$ from steady voltage with specified loading in Fig. 1. This parameter is sampled and is not 100% tested.



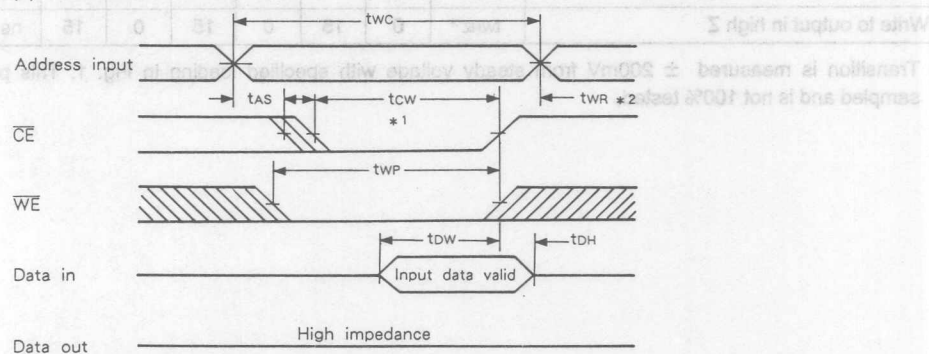
- Read cycle (1) : $\overline{WE}=V_{IH}$



- Write cycle (1) : $\overline{WE}$ control



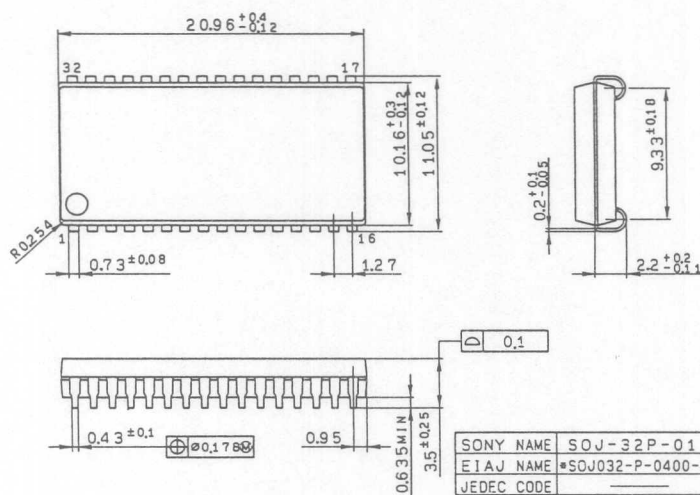
- Write cycle (2) : $\overline{\text{CE}}$ control



- *1. A write occurs during the low overlap of $\overline{CE}$ and $\overline{WE}$.
- *2. t_{WR} is measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high to the end of write cycle.
- *3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the output must not be applied.

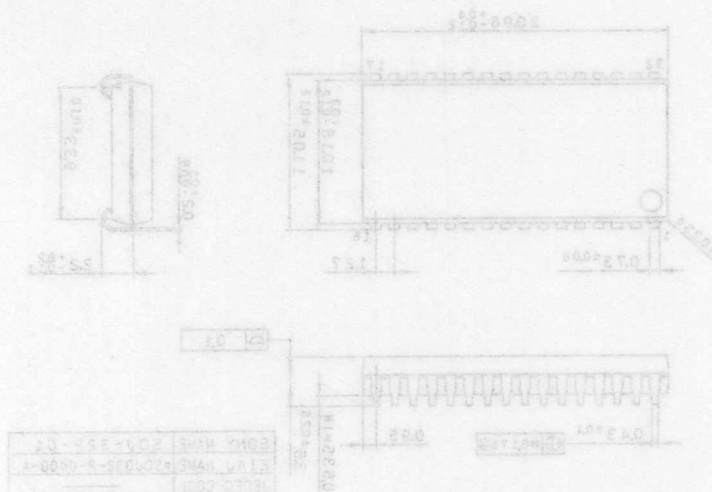
Unit : mm

32pin SOJ (Plastic) 400mil 1.3g



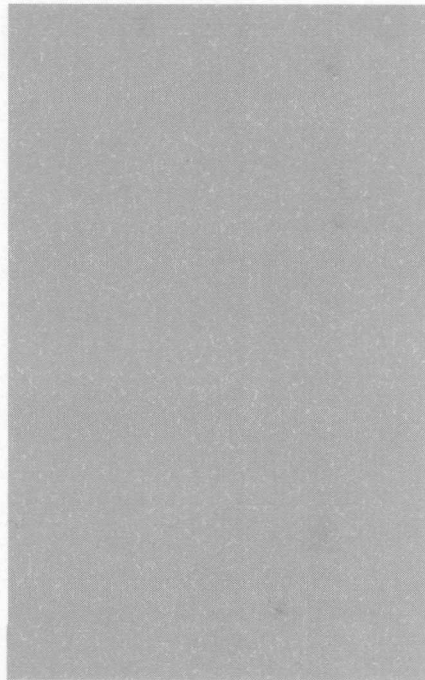
Package Outline Unit: mm

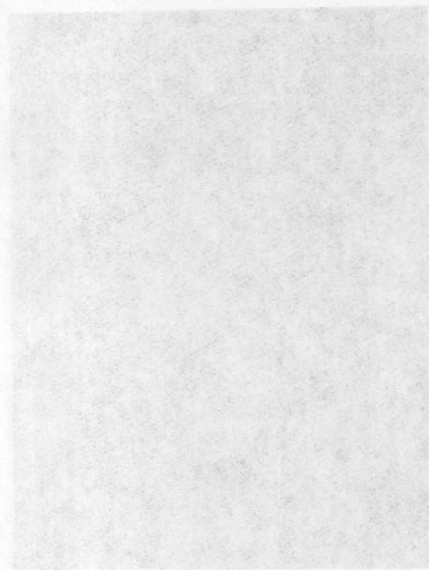
35mm SOV (Plastic) 400mil 1.38



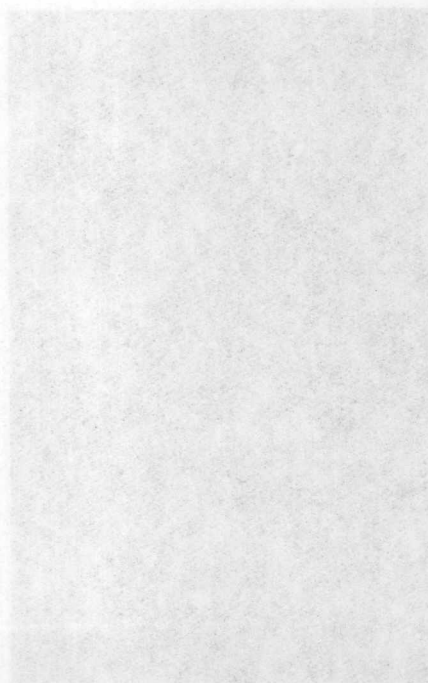


ASM (Application Specific Memory)





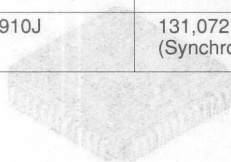
ASM (Application Specific Memory)



High-Speed Latched Cache-SRAM

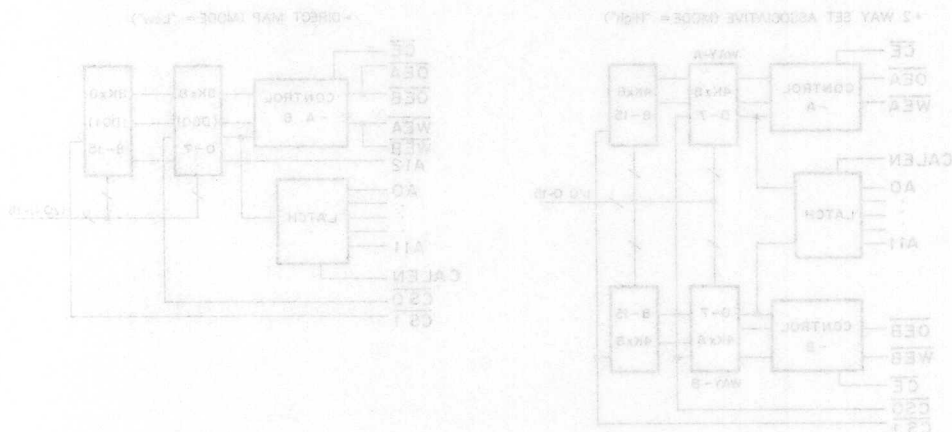
2) ASM (Application Specific Memory)

Type	Function	Process	Page
CXK7701J	8,192 word x 16bits, 30/35/45ns SRAM	MIX CMOS	324
CXK77910J	131,072 word x 9 bits, 17/20ns SRAM (Synchronous)	MIX CMOS	339



- Features
- Best fit for Cache configurations
 - Intel 82385 Cache Controller (for 80386-33 MHz, 33MHz, 50MHz)
 - Fast access time:
 - CXK7701J-30 30ns (Max)
 - CXK7701J-35 35ns (Max)
 - CXK7701J-45 45ns (Max)
 - Fast output Enable
 - CXK7701J-30 10ns (Max)
 - CXK7701J-35 13ns (Max)
 - CXK7701J-45 16ns (Max)
 - Available in 85 pin PLCC
 - Internal 12-bit address latch (A0 - A11)
 - Directly TTL compatible: All inputs and outputs

Block Diagram



High-Speed Latched Cache-SRAM

Description

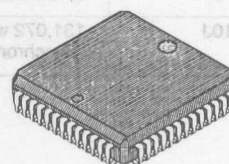
The CXK7701J is a 131,072-bit high speed latched Cache-SRAM suitable for use in high speed cache configurations and low power applications.

Organized as 8192 word × 16-bit or 4096 word × 16-bit × 2 WAY selected by mode control pin, it operates from a single 5V supply.

Features

- Best fit for Cache configurations
Intel 82385 Cache Controller (for 80386-33 MHz, 25MHz, 20MHz)
- Fast access time : (Access time)
CXK7701J-30 30ns (Max.)
CXK7701J-35 35ns (Max.)
CXK7701J-45 45ns (Max.)
- Fast output Enable
CXK7701J-30 10ns (Max.)
CXK7701J-35 13ns (Max.)
CXK7701J-45 16ns (Max.)
- Available in 52 pin PLCC
- Internal 12-bit address latch (A0 – A11)
- Directly TTL compatible : All inputs and outputs

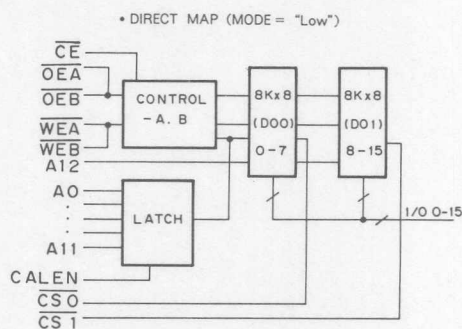
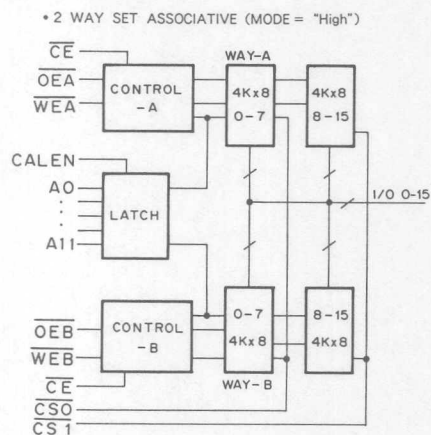
52 pin PLCC (Plastic)



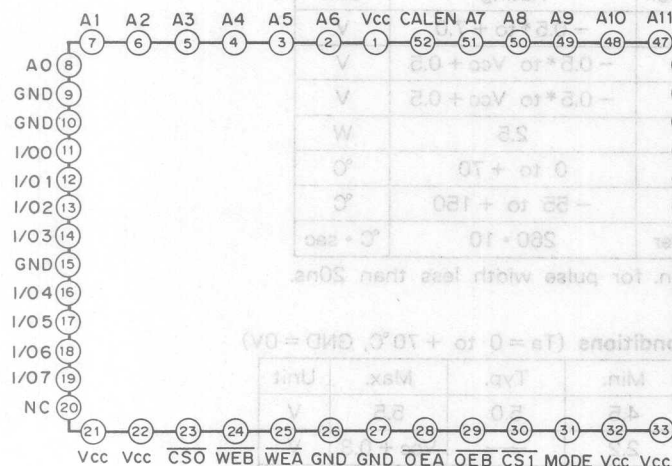
Structure

Silicon gate CMOS IC

Block Diagram



Pin Configuration



Pin Description

Symbol	Description
A0 to A12	Address Input
I/O0 to I/O15	Data Input Output
CE	Global Chip Enable Input
CS0, CS1	Chip Enable Input for I/O 0-7, I/O 8-15
OEA, OEB	Output Enable Input for Bank-A, Bank-B
WEA, WEB	Write Enable Input for Bank-A, Bank-B
CALEN	Address Latch Enable Input
MODE	Mode Control
Vcc	+ 5V Power Supply
GND	Ground
NC	No Connection

Item	Symbol	Rating	Unit
Supply Voltage	V _{CC}	- 0.5*to + 7.0	V
Input Voltage	V _{IN}	- 0.5*to V _{CC} + 0.5	V
Input & Output Voltage	V _{I/O}	- 0.5*to V _{CC} + 0.5	V
Power Dissipation	P _D	2.5	W
Operating Temperature	T _{opr}	0 to + 70	°C
Storage temperature	T _{stg}	- 55 to + 150	°C
Soldering Temperature	T _{solder}	260 • 10	°C • sec

* **Note)** V_{CC}, V_{IN}, V_{I/O} = - 3.5V Min. for pulse width less than 20ns.

DC Recommended Operating Conditions (T_a = 0 to + 70°C, GND = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Input high voltage	V _{IH}	2.2	—	V _{CC} + 0.3	V
Input low voltage	V _{IL}	- 0.3*	—	0.8	V

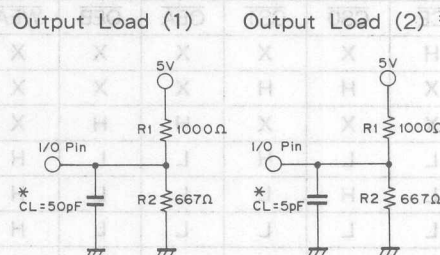
* **Note)** V_{IL} = - 3.0V Min. for pulse width less than 20ns.

DC and Operating Characteristics (V_{CC} = 5V ± 10%, GND = 0V, T_a = 0 to + 70°C)

Item	Symbol	Test conditions	Min.	Max.	Unit
Input Leakage Current	I _{LI}	V _{IN} = GND to V _{CC}	- 2	2	μA
Output Leakage Current	I _{LO}	V _{I/O} = GND to V _{CC} , $\overline{CE}$ = V _{IH} or $\overline{CS0}$, CS1 = V _{IH} or OEA, OEB = V _{IH} or WEA, WEB = V _{IL}	- 2	2	μA
Operating Supply Current	I _{CC1}	$\overline{CS0}$, CS1 & $\overline{CE}$ = V _{IL} V _{IN} = V _{IL} or V _{IH} I _{OUT} = 0mA	—	180	mA
Average Operating Current	I _{CC2}	100 % Duty Cycle V _{IN} = GND to V _{CC} I _{OUT} = 0mA	—	240	mA
	I _{CC3}	50 % Duty Cycle V _{IN} = GND to V _{CC} I _{OUT} = 0mA	—	220	mA
Output High Voltage	V _{OH}	I _{OH} = - 1.0mA	2.4	—	V
Output Low Voltage	V _{OL}	I _{OL} = 4.0mA	—	0.4	V

A. C. Test Condition (Applies to Read & Write Cycle Timing)(V_{CC} = 5V ± 10 %, T_a = 0 to + 70 °C)**Fig-1**

Item	Conditions	Unit	Output Load (1)	Output Load (2) **
Input Pulse High Level	V _{IH} = 3.0	V	X	X
Input Pulse Low Level	V _{IL} = 0.0	V	X	X
Input Rise Time	t _r = 3	ns	X	X
Input Fall Time	t _f = 3	ns	X	X
Input and Output Reference Level	1.5	V	X	X
Output Load (See Test Circuit Fig-1)	R1 1000	Ω	X	X
	R2 667	Ω	X	X
	CL 50	pF	X	X



* Including scope and jig capacitance

** For tLZ, tHZ, tOHZ, tOLZ, tWLZ, tWHZ

Truth Tables**Two-Way Mode (Mode = High)**

$\overline{\text{CE}}$	$\overline{\text{CS0}}$	$\overline{\text{CS1}}$	$\overline{\text{OEA}}$	$\overline{\text{OEB}}$	$\overline{\text{WEA}}$	$\overline{\text{WEB}}$	Operation
H	X	X	X	X	X	X	Outputs High-Z, Write Disabled
X	H	H	X	X	X	X	Outputs High-Z, Write Disabled
X	X	X	H	H	X	X	Outputs High-Z
X	X	X	L	L	X	X	Outputs High-Z
L	L	H	L	H	H	H	Read I/O 0 - 7 Way A
L	L	H	H	L	H	H	Read I/O 0 - 7 Way B
L	H	L	L	H	H	H	Read I/O 8 - 15 Way A
L	H	L	H	L	H	H	Read I/O 8 - 15 Way B
L	L	L	L	H	H	H	Read I/O 0 - 15 Way A
L	L	L	H	L	H	H	Read I/O 0 - 15 Way B
L	L	H	X	X	L	H	Write I/O 0 - 7 Way A
L	L	H	X	X	H	L	Write I/O 0 - 7 Way B
L	H	L	X	X	L	H	Write I/O 8 - 15 Way A
L	H	L	X	X	H	L	Write I/O 8 - 15 Way B
L	L	L	X	X	L	H	Write I/O 0 - 15 Way A
L	L	L	X	X	H	L	Write I/O 0 - 15 Way B
L	L	H	X	X	L	L	Write I/O 0 - 7 Way A & B
L	H	L	X	X	L	L	Write I/O 8 - 15 Way A & B
L	L	L	X	X	L	L	Write I/O 0 - 15 Way A & B

Note) X : "H" or "L"

Truth Tables

Direct Mode (Mode = Low)

$\overline{CE}$	$\overline{CS0}$	$\overline{CS1}$	$\overline{OE0}$	$\overline{OE1}$	$\overline{WE0}$	$\overline{WE1}$	Operation
H	X	X	X	X	X	X	Outputs High-Z, Write Disabled
X	H	H	X	X	X	X	Outputs High-Z, Write Disabled
X	X	X	H	H	X	X	Outputs High-Z
L	L	H	L	L	H	H	Read I/O 0-7
L	H	L	L	L	H	H	Read I/O 8-15
L	L	L	L	L	H	H	Read I/O 0-15
L	L	H	X	X	L	L	Write I/O 0-7
L	H	L	X	X	L	L	Write I/O 8-15
L	L	L	X	X	L	L	Write I/O 0-15

Note) X: "H" or "L"

I/O capacitance

(Ta = 25°C, f = 1MHz)

Item	Symbol	Test conditions	Min.	Max.	Unit
Input capacitance	C_{IN}	$V_{IN} = 0V$	—	7	pF
Input/Output capacitance	$C_{I/O}$	$V_{I/O} = 0V$	—	9	pF

Note) This parameter is sampled and is not 100% tested.

• Write Cycle Timing

(V_{CC} = 5V ± 10 %)

Item	Symbol	- 30		- 35		- 45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	t _{WC}	30	—	35	—	45	—	ns
Address Valid to End of Write	t _{AW}	20	—	25	—	35	—	ns
A12 Valid to End of Write	t _{A12W}	18	—	22	—	30	—	ns
Chip Select to End of Write	t _{CW}	18	—	22	—	30	—	ns
Data Valid to End of Write	t _{DW}	10	—	12	—	15	—	ns
Data Hold from End of Write	t _{DH}	0	—	0	—	0	—	ns
Write Enable Active to High-Z	t _{WHZ} *	—	15	—	15	—	20	ns
WRITE Enable Inactive to Low-Z	t _{WLZ} *	3	—	3	—	3	—	ns
Write Pulse Width	t _{WP}	18	—	22	—	30	—	ns
CE Pulse Width During Chip Enable Controlled Write	t _{CP}	18	—	22	—	30	—	ns
Address Setup Time	t _{AS}	0	—	0	—	0	—	ns
Write Recovery Time	t _{WR}	0	—	0	—	2	—	ns
Address Latch Enable Pulse Width	t _{CALEN}	8	—	10	—	15	—	ns
Address Setup to Latch Low	t _{ASL}	4	—	6	—	10	—	ns
Address Hold to Latch Low	t _{AHL}	5	—	5	—	5	—	ns

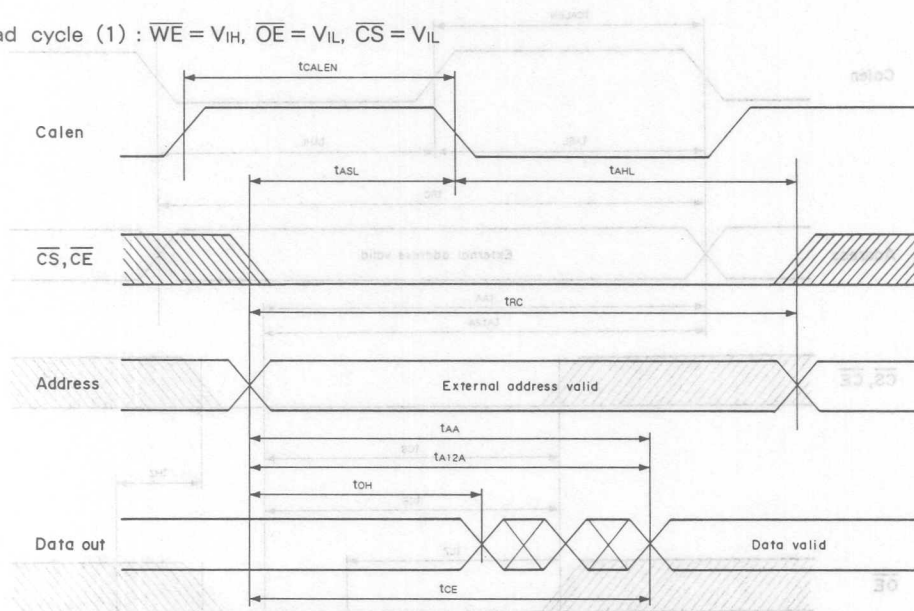
* Transition is measured ± 200mV from steady voltage with specified loading in Fig. 1 (2).
This parameter is sampled and is not 100% tested.

Item	Symbol	- 30		- 35		- 45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t _{RC}	30	—	35	—	45	—	ns
Address Access Time	t _{AA}	—	30	—	35	—	45	ns
A12 Address Access Time	t _{A12A}	—	17	—	25	—	30	ns
Chip Select Access Time	t _{CS} t _{CE}	—	20	—	25	—	35	ns
Output Enable to Output Valid	t _{OE}	—	10	—	13	—	16	ns
Output Hold from Address Change	t _{OH}	3	—	3	—	3	—	ns
Chip Select to Output Low-Z	t _{LZ} *	3	—	3	—	3	—	ns
Output Enable to Output Low-Z	t _{OLZ} *	2	—	2	—	2	—	ns
Chip Deselect to Output High-Z	t _{HZ} *	—	15	—	25	—	30	ns
Output Disable to Output High-Z	t _{OHZ} *	—	10	—	14	—	14	ns
Address Latch Enable Pulse Width	t _{CALEN}	8	—	10	—	15	—	ns
Address Setup to Latch Low	t _{ASL}	4	—	6	—	10	—	ns
Address Hold to Latch Low	t _{AHL}	5	—	5	—	5	—	ns

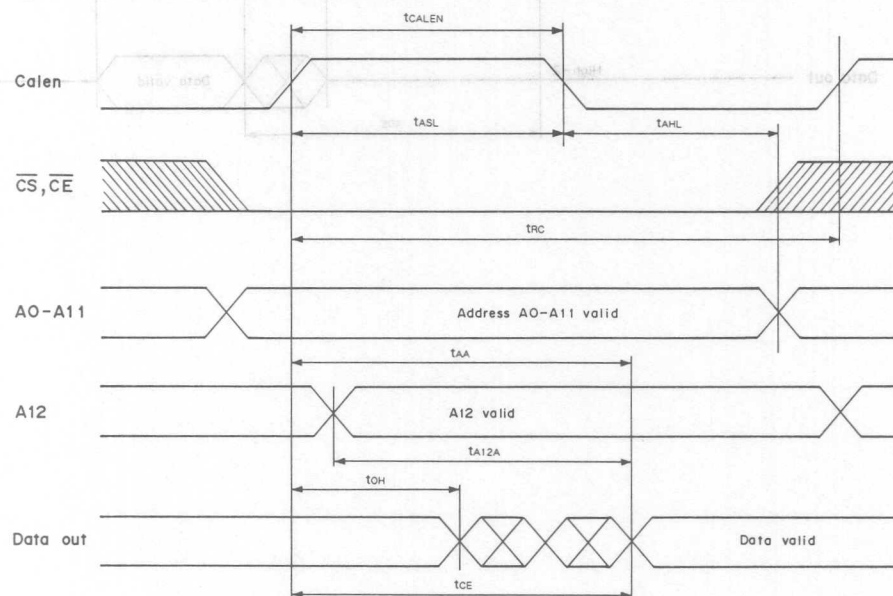
* Transition is measured $\pm 200\text{mV}$ from steady voltage with specified loading in Fig. 1 (2).
This parameter is sampled and is not 100% tested.

Timing Waveform

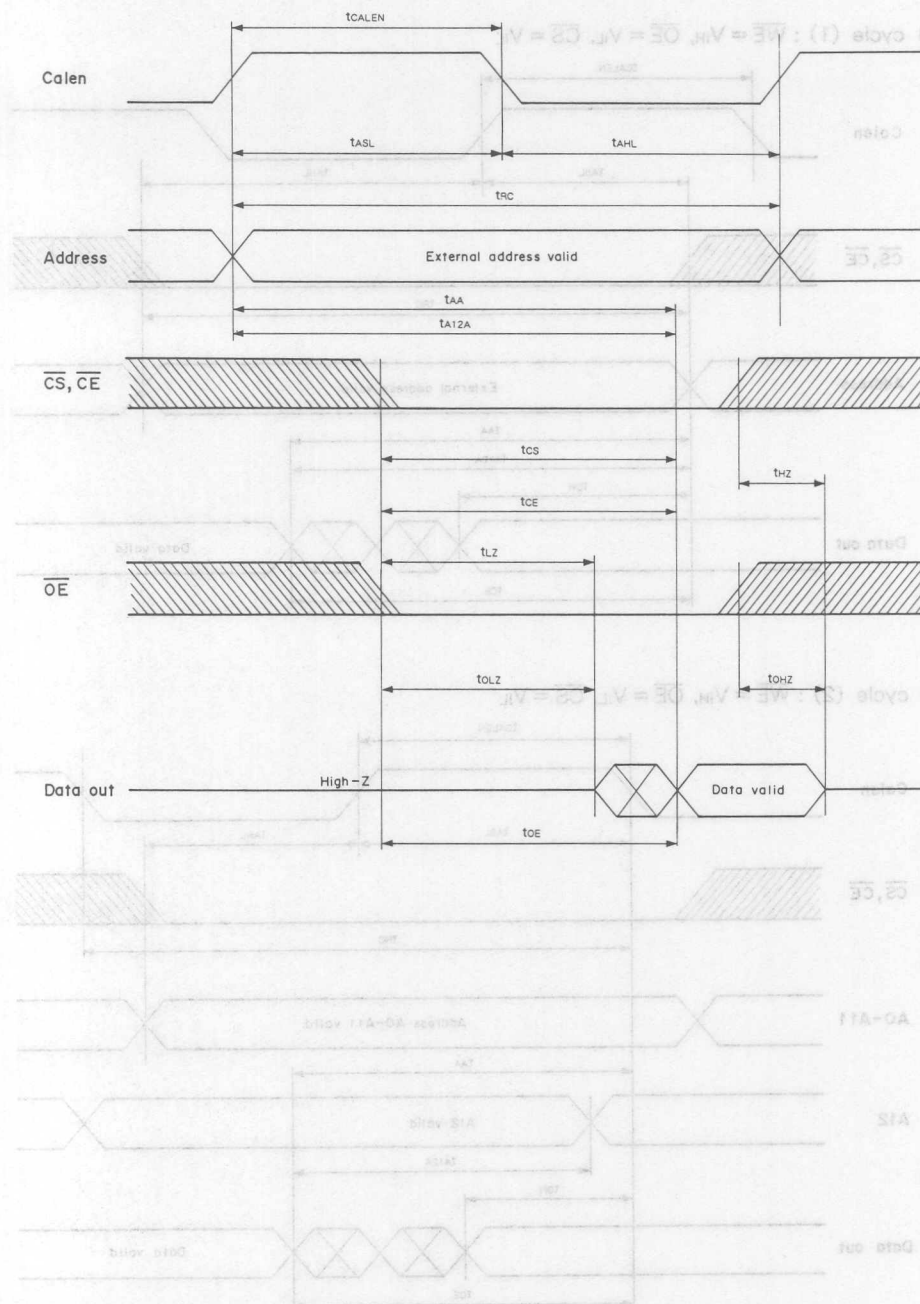
- Read cycle (1) : $\overline{WE} = V_{IH}$, $\overline{OE} = V_{IL}$, $\overline{CS} = V_{IL}$



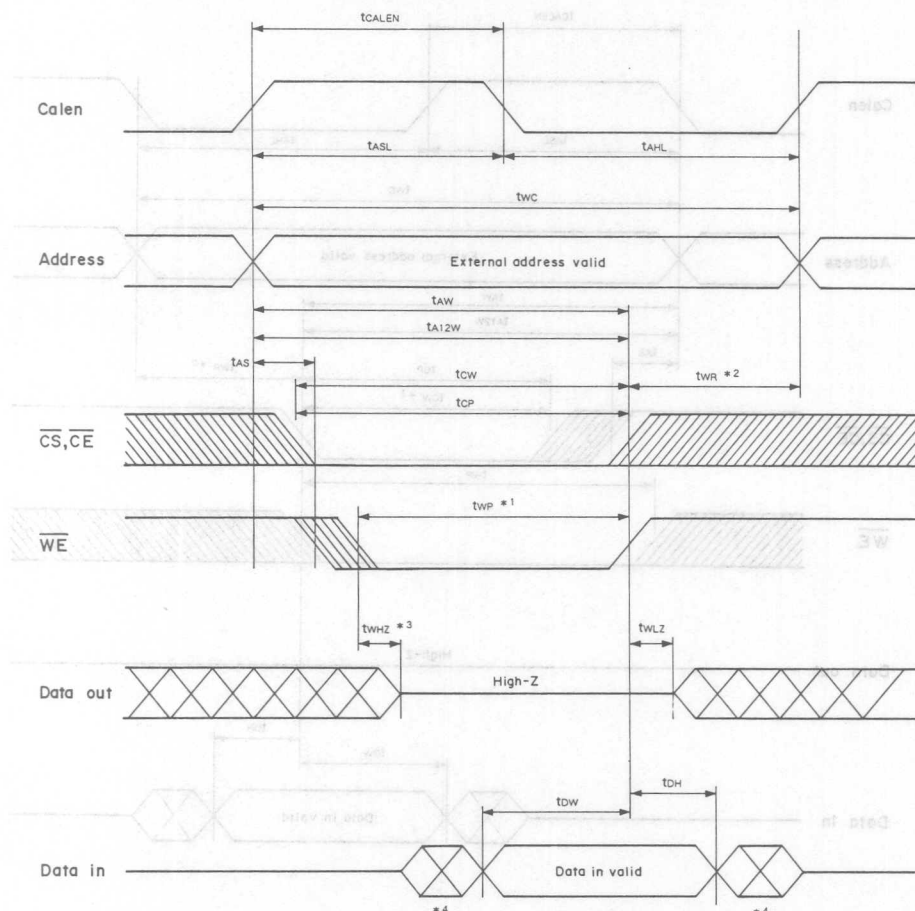
- Read cycle (2) : $\overline{WE} = V_{IH}$, $\overline{OE} = V_{IL}$, $\overline{CS} = V_{IL}$



• Read cycle (3) : $\overline{WE} = V_{IH}$

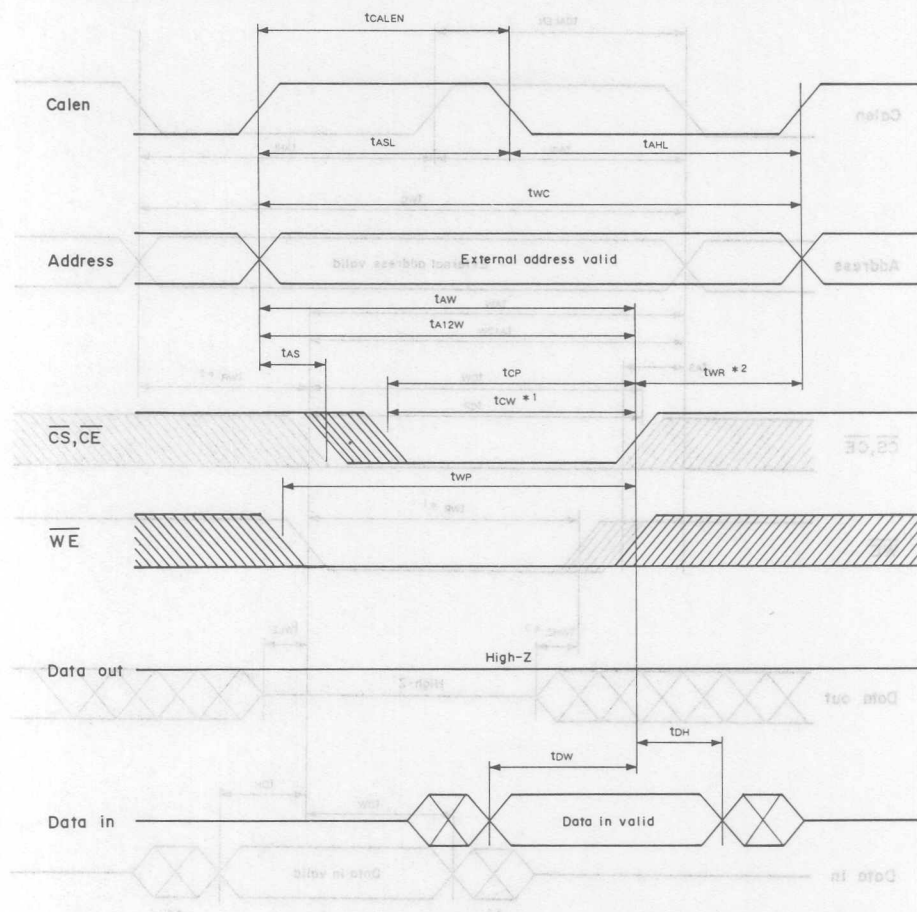


• Write cycle (1) : $\overline{WE}$ control



- *1. A write occurs during the low overlap of $\overline{CS}$, $\overline{CE}$ and $\overline{WE}$.
- *2. t_{WR} is measured from the start of $\overline{CE}$ or $\overline{WE}$ going high to the end of write cycle.
- *3. If $\overline{CE}$ and $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or at the same time, t_{WR} is measured from the start of $\overline{WE}$ going high to the end of write cycle.
- *4. During this period, I/O pins are in the output state so that the input signals of output phase to the output must not be applied.

• Write cycle (2) : $\overline{CE}$ control



- *1. A write occurs during the low overlap of $\overline{CS}$, $\overline{CE}$ and $\overline{WE}$.
- *2. t_{WR} is measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high to the end of write cycle.
- *3. If $\overline{CE}$ and $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, output remains in a high impedance state.
- *4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the output must not be applied.

Control Pin Description

CALEN (Cache Address Latch Enable)

This signal controls the internal address latch that resides between the address inputs and the memory array. When CALEN is high the latch is transparent. The falling edge of CALEN latches the current address inputs.

MODE

This signal controls whether the memory device is to be used in a direct mapped ($8k \times 16$) configuration or a two-way set associative ($2-4k \times 16$) configuration. When the mode signal is high, the device is placed in two-way mode. When the mode pin is low, the device is placed in direct mode.

 $\overline{CS0}$, $\overline{CS1}$ (Cache Chip Selects)

These active low signals tie to the cache ram chip selects and individually enable the two bytes of the memory. $\overline{CS0}$ enables bits $I/O0-I/O7$ and, $\overline{CS1}$ enables bits $I/O8-I/O15$.

 $\overline{CE}$ (Cache Chip Enable)

This active low signal, when active, enable writes to the data ram or reads from the data ram. It is a global signal, and controls both cache bank A and cache bank B. It's function is the same in both the set associative mode and the direct mapped mode. This input also functions as a chip enable controlled write.

 $\overline{OEa}$, $\overline{OEb}$ (Cache Output Enables)

In two-way mode, these active low signals enable cache bank A or B to drive the data bus. Either $\overline{OEa}$ or $\overline{OEb}$ is active during a read hit, depending on which bank is selected. Activation of $\overline{OEa}$ simultaneous with $\overline{OEb}$ will cause both banks to become deselected. In direct mode, these inputs will be externally wired together and A12 will determine which $4K \times 16$ memory bank is enabled.

 $\overline{WEa}$, $\overline{WEb}$ (Cache Write Enables)

In two-way mode, these active low signals enable cache bank A or B to receive data from the data bus. Either $\overline{WEa}$ or $\overline{WEb}$ is enabled in a read miss update or write hit. In direct mode, these inputs will be externally wired together and A12 will determine which $4K \times 16$ memory bank will be enabled for writing.

A0 – A11 (Addresses)

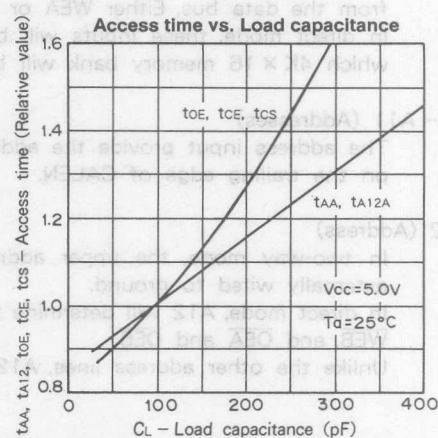
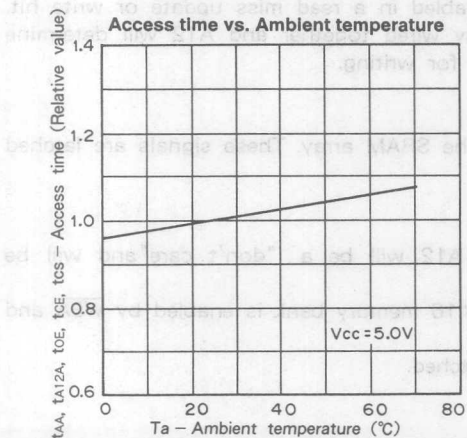
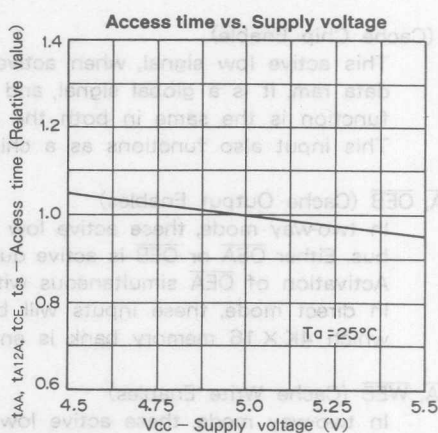
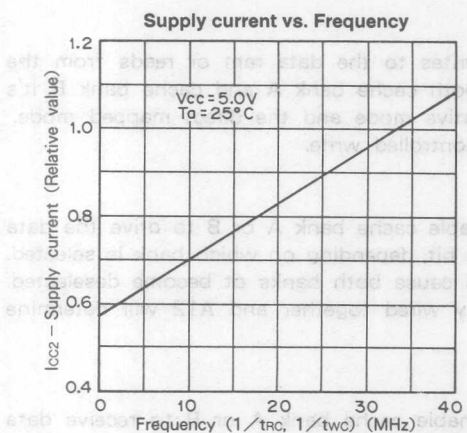
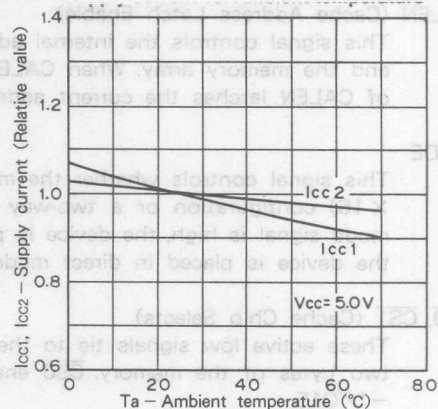
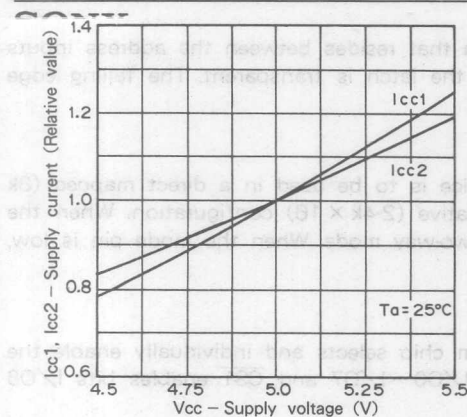
The address input provide the address into the SRAM array. These signals are latched on the trailing edge of CALEN.

A12 (Address)

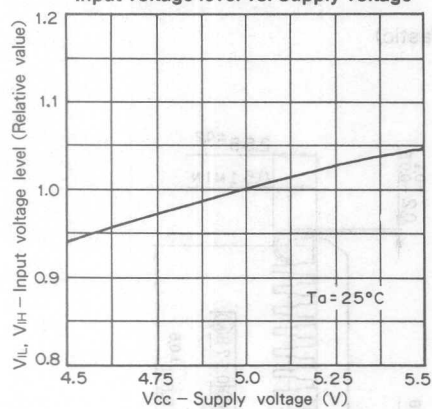
In two-way mode, the upper address input A12 will be a "don't care" and will be externally wired to ground.

In direct mode, A12 will determine which $4K \times 16$ memory bank is enabled by $\overline{WEa}$ and $\overline{WEb}$, and $\overline{OEa}$ and $\overline{OEb}$.

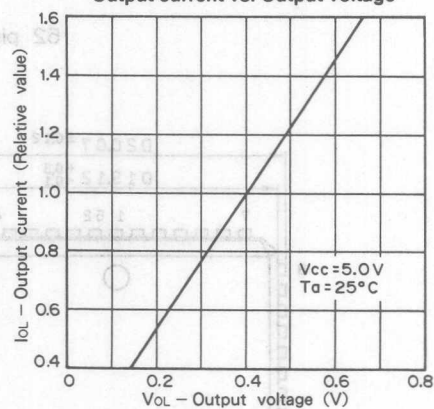
Unlike the other address lines, A12 is not latched.



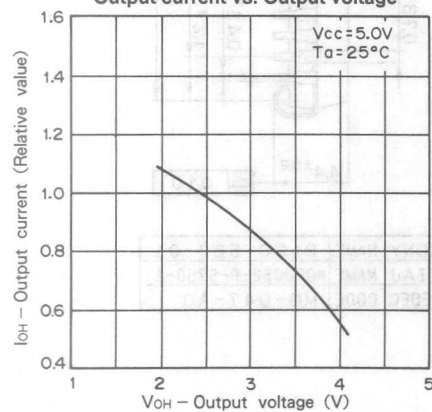
Input voltage level vs. Supply voltage



Output current vs. Output voltage

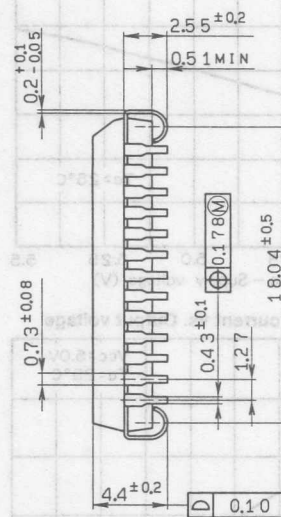
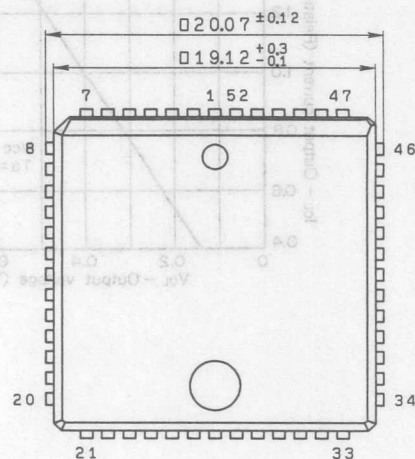


Output current vs. Output voltage



Package Outline Unit : mm

52 pin PLCC (Plastic)



SONY NAME	PLCC-52P-01
EIAJ NAME	*QFJ052-P-S750-A
JEDEC CODE	MO-047-AD

Description

The CXK77910J is a 1,179,648 bit Self-Timed Static Random Access Memory organized as 128K words by 9 bits. This STRAM integrates Input Registers, High Speed SRAM and Output Registers onto a single monolithic circuit. All Registers are triggered with the positive edge of an external clock (CLK). At the positive edge of CLK, the RAM data of the previous CLK cycle is presented. Write operation is initiated by the positive edge of CLK and internally self-timed. This feature eliminates complex off-chip write pulse generation and provides increased flexibility for incoming signals.

Function

There are three possible user transactions with the STRAM. (Read operation, write operation and deselect operation.)

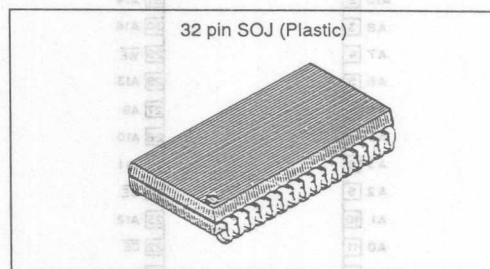
The read operation requires $\overline{WE}$ ="HIGH" and $\overline{OE}=\overline{CE}$ ="low" on the positive edge of CLK.

The memory location pointed to by the contents of the Address registers is read internally and the contents of the location are captured in the Data-out registers on the next positive edge of CLK. The state of Data-out will reflect the contents of the Data-out registers.

The write operation requires $\overline{CE}=\overline{WE}$ ="LOW" on the positive edge of CLK. The memory location pointed to by the contents of the Address registers is written with the contents of the Data-in registers. The write operation is entirely self-timed, eliminating critical timing edges.

The deselect cycle requires $\overline{CE}$ ="HIGH" or $\overline{OE}=\overline{WE}$ ="HIGH" on the positive edge of CLK. Write operation and internal read operation are disabled during the clock cycle. The data outputs are forced to a high impedance state during the next clock cycle. During the deselect cycle by $\overline{CE}$ ="HIGH", STRAM turns to power down mode.

The write cycle needs three preceding deselect cycles since the data for the write cycle must be supplied to I/O terminals during high impedance state. But immediately after power-on of the STRAM, the write operation can start on the first positive edge of CLK since the I/O terminals are initialized to be in high-impedance state.



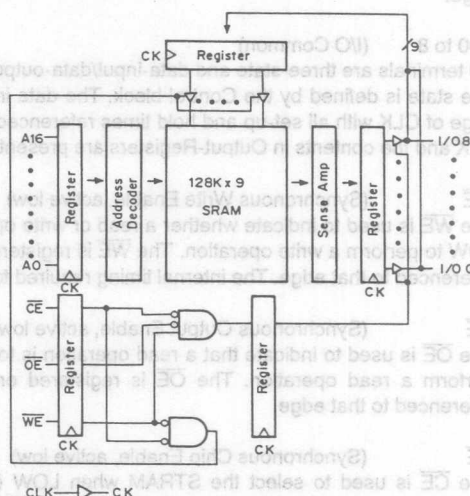
Features

- Fast Cycle Time: (Cycle) (Frequency)
CXK77910J-17 16.6ns 60MHz
CXK77910J-20 20.0ns 50MHz
- Fast Clock to Data Valid
CXK77910J-17/20 10ns
- Available in Plastic 32 pin 400mil SOJ
- All inputs and outputs registered with clock
- Direct TTL compatible
- Low power consumption (min. cycle, 100% duty)
CXK77910J-17/20 715mW (Max.)

Structure

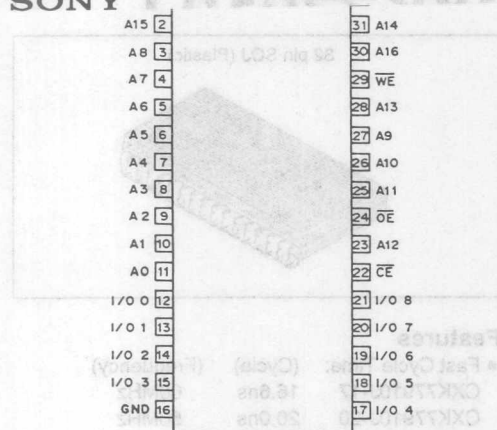
Silicon gate CMOS IC

Block Diagram



Sony reserves the right to change products and specifications without prior notice. This information does not convey any license by any implication or otherwise under any patents or other right. Application circuits shown, if any, are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits.

SONY



A0 to A16	Address input
I/O0 to I/O8	Data input/output
CE	Chip enable input
OE	Output enable input
WE	Write enable input
CLK	Clock input
Vcc	+5V power supply
GND	Ground

Pin Description (2)

CLK (Clock, positive edge triggered)

All timing is controlled by the positive edge of CLK. All synchronous input and output signals are registered on the positive edge of CLK with set-up and hold times referenced to that edge.

Since only one edge of CLK is referenced, the duty cycle of CLK is not critical.

A0 to A16 (Address)

The Address inputs are decoded on-chip to select one of 131,072 words.

The state of the Address inputs is registered into the Address register on the positive edge of CLK.

The Address inputs must be valid during every positive edge with all set-up and hold times referenced to that edge.

I/O0 to 8 (I/O Common)

I/O terminals are three-state and data-input/data-output common.

The state is defined by the Control block. The data inputs for write operation must be valid during every positive edge of CLK with all set-up and hold times referenced to that edge. The data outputs are triggered by the edge of CLK and the contents in Output-Registers are presented.

WE (Synchronous Write Enable, active low)

The WE is used to indicate whether a read or write operation is to be performed. If the STRAM is selected, WE is LOW to perform a write operation. The WE is registered on every positive edge of CLK with set-up and hold times referenced to that edge. The internal timing required to store data into the memory array is self-timed.

OE (Synchronous Output Enable, active low)

The OE is used to indicate that a read operation is to be performed. If the STRAM is selected, the OE is LOW to perform a read operation. The OE is registered on every positive edge of CLK with set-up and hold times referenced to that edge.

CE (Synchronous Chip Enable, active low)

The CE is used to select the STRAM when LOW (or deselect when HIGH). When selected, the STRAM will perform a read or write operation. The state of the CE is registered on every positive edge of CLK with set-up and hold times referenced to that edge.

Absolute Maximum Ratings

(Ta=25°C, GND=0V)

Item	Symbol	Rating	Unit
Supply voltage	V _{CC}	-0.5 to +7.0	V
Input voltage	V _{IN}	-0.5 to V _{CC} +0.5	V
Input and output voltage	V _{IO}	-0.5 to V _{CC} +0.5	V
Allowable power dissipation	P _D	1.0	W
Operating temperature	T _{opr}	0 to +70	°C
Storage temperature	T _{stg}	-55 to +150	°C

DC Recommended Operating Conditions

(Ta=0 to +70°C, GND=0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Power Supply voltage	V _{CC}	4.5	5.0	5.5	V
Input high voltage	V _{IH}	2.2	—	V _{CC} +0.3	V
Input low voltage	V _{IL}	-0.3*	—	0.8	V

* V_{IL}=-1V Min. for 3ns per cycle.

Electrical Characteristics

• DC and operating characteristics (V_{CC}=5V ± 10%, GND=0V, Ta=0 to +70°C)

Item	Symbol	Test conditions	Min.	Max.	Unit
Input leakage current	I _{LI}	V _{IN} =GND to V _{CC}	-1	1	μA
Output leakage current	I _{LO}	V _{IO} =GND to V _{CC} , CE=V _{IH} or OE=V _{IH} or WE=V _{IL}	-1	1	μA
Operating power supply current	I _{CC1}	CE=V _{IL} , V _{IN} =V _{IH} or V _{IL} , I _{OUT} =0mA	—	100	mA
Average operating current	I _{CC2}	Cycle=Min, Duty=100%, I _{OUT} =0mA	—	130	mA
Standby current	I _{SB1}	CE ≥ V _{CC} -0.2V V _{IN} ≥ V _{CC} -0.2V or V _{IN} ≤ 0.2V	—	1	mA
	I _{SB2}	CE=V _{IH} , I _{OUT} =0mA Cycle=Min, Duty=100%	—	80	mA
Output high voltage	V _{OH}	I _{OH} =-1.0mA	2.4	—	V
Output low voltage	V _{OL}	I _{OL} =4.0mA	—	0.4	V

Truth tables

CLK	CE	OE	WE	Operation
	H	x	x	Outputs High-Z, Write Disabled, Power Down
	x	H	H	Outputs High-Z, Write Disabled
	L	L	H	Read I/O 0 to 8
	L	x	L	Write I/O 0 to 8

x : "H" or "L"

I/O capacitance

(Ta=25°C, f=1MHz)

Item	Symbol	Test conditions	Min.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} =0V	—	5	pF
I/O capacitance	C _{I/O}	V _{I/O} =0V	—	7	pF

Note) This parameter is sampled and is not 100% tested.

AC characteristics

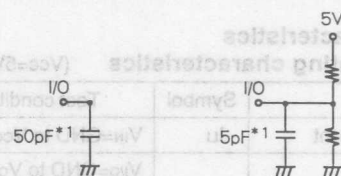
● AC test conditions

(V_{CC}=5V ± 10%, T_a=0 to +70°C)

Item	Conditions
Input pulse high level	V _{IH} =3.0V
Input pulse low level	V _{IL} =0V
Input rise time	t _r =3ns
Input fall time	t _f =3ns
Input and output reference level	1.5V
Output load (See test circuit below)	Fig. 1

Output Load (1)

Output Load (2) *2

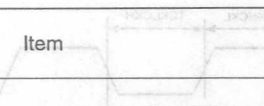


* 1 including scope and jig capacitance

* 2 for t_{CKH}QZ, t_{CKH}X2

Fig. 1

• Read cycle

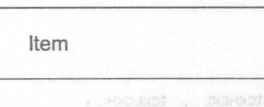


Item	Symbol	-17		-20		Unit
		Min	Max	Min	Max	
Read cycle time	t _{CKHCKH}	16.6	—	20	—	ns
Clock high pulse width	t _{CKHCKL}	5	—	5	—	ns
Clock low pulse width	t _{CKLCKH}	5	—	5	—	ns
Clock to data valid	t _{CKHdV}	—	10	—	10	ns
Address setup to clock high	t _{AVCKH}	3	—	3	—	ns
Address hold from clock high	t _{CKHAX}	0.5	—	1	—	ns
Chip enable setup to clock high	t _{CEVCKH}	3	—	3	—	ns
Chip enable hold from clock high	t _{CKHCEX}	0.5	—	1	—	ns
Output enable setup to clock high	t _{OEVCKH}	3	—	3	—	ns
Output enable hold from clock high	t _{CKHOEX}	0.5	—	1	—	ns
Output hold from clock high	t _{CKHQX1}	2	—	3	—	ns
Clock high to output low-Z	t _{CKHQX2} *	0	—	0	—	ns
Clock high to output high-Z	t _{CKHQZ} *	—	8	—	10	ns

* Transition is measured $\pm 200\text{mV}$ from steady voltage with specified loading in Fig. 1-(2).

This parameter is sampled and is not 100% tested.

• Write cycle



Item	Symbol	-17		-20		Unit
		Min	Max	Min	Max	
Write cycle time	t _{CKHCKH}	16.6	—	20	—	ns
Clock high pulse width	t _{CKHCKL}	5	—	5	—	ns
Clock low pulse width	t _{CKLCKH}	5	—	5	—	ns
Address setup to clock high	t _{AVCKH}	3	—	3	—	ns
Address hold from clock high	t _{CKHAX}	0.5	—	1	—	ns
Chip enable setup to clock high	t _{CEVCKH}	3	—	3	—	ns
Chip enable hold from clock high	t _{CKHCEX}	0.5	—	1	—	ns
Write enable setup to clock high	t _{WEVCKH}	3	—	3	—	ns
Write enable hold from clock high	t _{CKHWEX}	0.5	—	1	—	ns
Input data setup to clock high	t _{DVCKH}	3	—	3	—	ns
Input data hold from clock high	t _{CKHDX}	0.5	—	1	—	ns

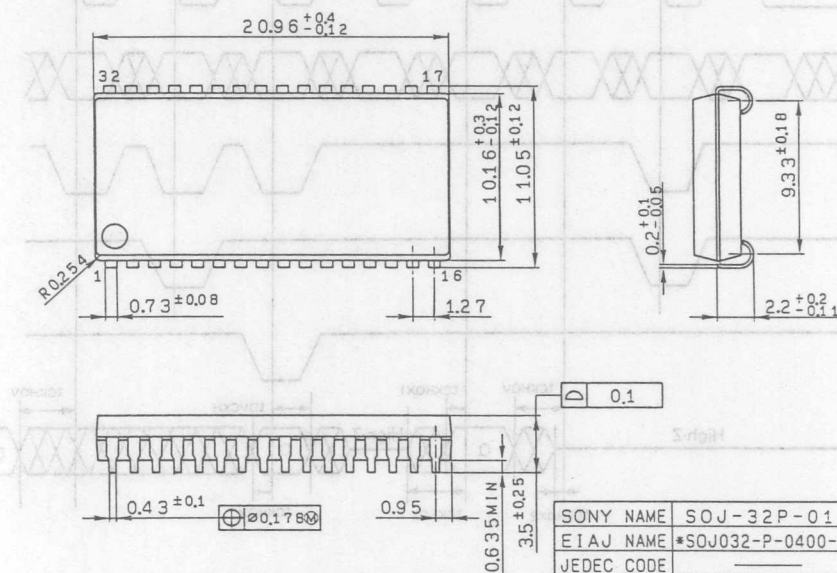
* 2 Valid data from CLK high is the data from the previous cycle.

344

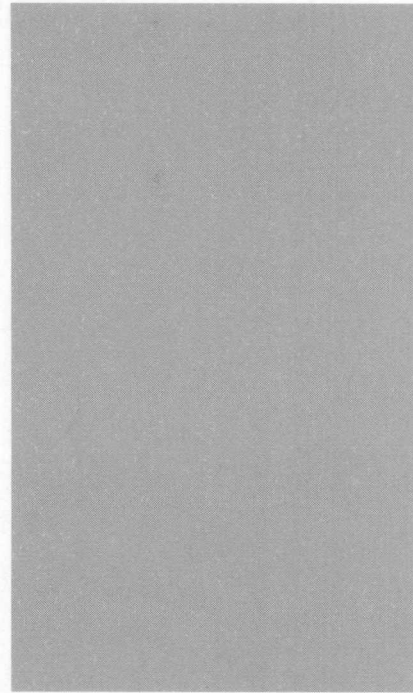
Package Outline

Unit : mm

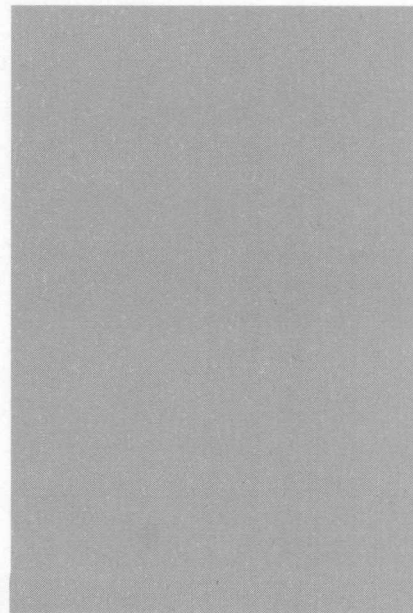
32pin SOJ (Plastic) 400mil 1.3g

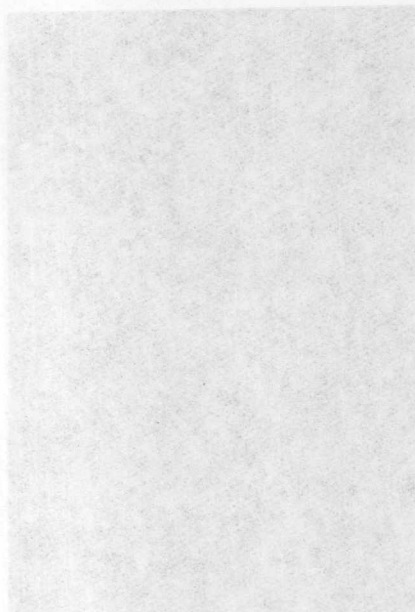


SONY NAME	SOJ-32P-01
EIAJ NAME	*SOJ032-P-0400-A
JEDEC CODE	

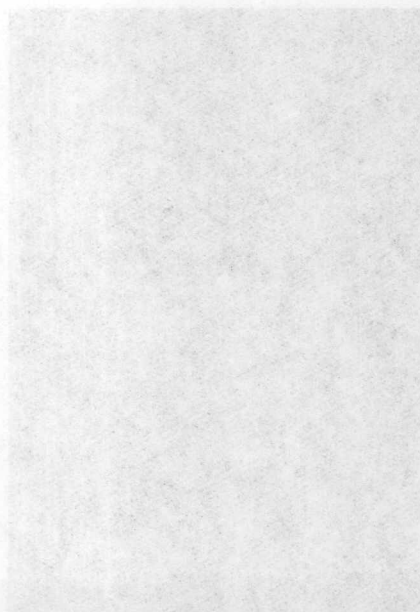


Mask ROM



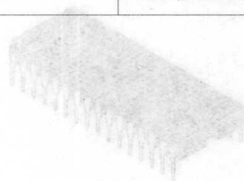


Mask ROM



3) Mask ROM

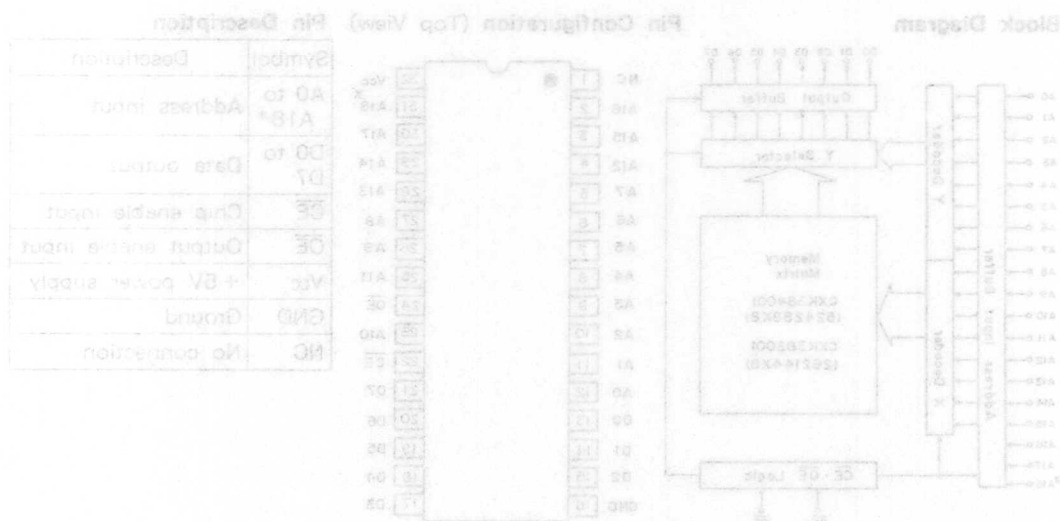
Type	Function	Process	Page
CXK384001	524,288 word x 8bits, 200ns	CMOS	350



Functions
CXK384001
524,288-word x 8-bit mask programmable ROM
CXK382001
285,144-word x 8-bit mask programmable ROM

Structure
Silicon gate CMOS IC

- Features
- Single +5V power supply operation
 - Tri-state output
 - NO TTL compatible
 - Static operation
 - 8.0mW (Standby CMOS input level)
 - 0.5mW (Standby TTL input level)
 - 100mW (Operation)
 - Power consumption (Typ.)
 - Output enable access time 70ns
 - Chip enable access time 200ns
 - Address access time 200ns
 - Access time (Max.)



Note: See the below table.

Typ.	Block Diagram	Pin Configuration	Pin Description
CXK384001	A18	A18	A0 to A18
CXK382001	No A18	NC	A0 to A17

SONY®

CXK384001/382001

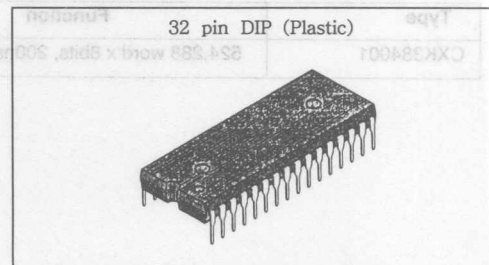
524,288 /262,144-word × 8-bit CMOS Mask Programmable ROM

Description

CXK384001 / 382001 is a CMOS mask-programmable ROM organized as 524,288 words by 8-bit (CXK384001) and 262,144 words by 8-bit (CXK382001). The chip enable input disable outputs and sets the chip to low power standby mode.

Features

- Access time (Max.)
 - Address access time 200ns
 - Chip enable access time 200ns
 - Output enable access time 70ns
- Power consumption (Typ.)
 - 100mW (Operation)
 - 0.5mW (Standby TTL input level)
 - 5.0nW (Standby CMOS input level)
- Static operation
- I/O TTL compatible
- Tri-state output
- Single +5V power supply operation



Functions

CXK384001

524,288-word × 8-bit mask programmable ROM

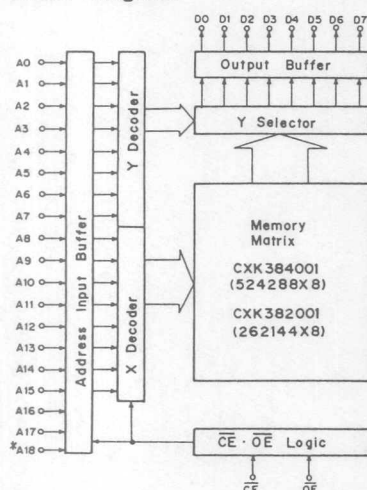
CXK382001

262,144-word × 8-bit mask programmable ROM

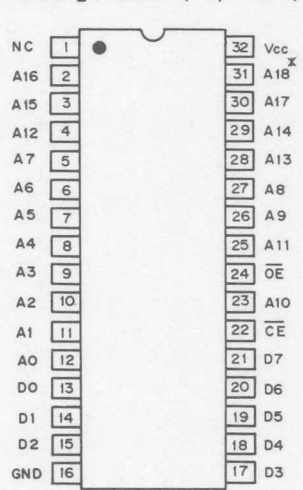
Structure

Silicon gate CMOS IC

Block Diagram



Pin Configuration (Top View)



Pin Description

Symbol	Description
A0 to A18*	Address input
D0 to D7	Data output
$\overline{CE}$	Chip enable input
$\overline{OE}$	Output enable input
Vcc	+5V power supply
GND	Ground
NC	No connection

Note)* See the below table.

Typ.	Block Diagram	Pin Configuration	Pin Description
CXK384001	A18	A18	A0 to A18
CXK382001	No A18	NC	A0 to A17

Absolute Maximum Ratings

(Ta = 25 °C, GND = 0V)

Item	Symbol	Ratings	Unit
Supply voltage	V _{CC}	- 0.5* to + 7.0	V
Input voltage	V _{IN}	- 0.5* to V _{CC} + 0.5	V
Output voltage	V _{OUT}	- 0.5* to V _{CC} + 0.5	V
Allowable power dissipation	P _D	1.0	W
Operating temperature	T _{opr}	0 to + 70	°C
Storage temperature	T _{stg}	- 55 to + 150	°C
Soldering temperature • time	T _{solder}	260 • 10	°C • sec

Note) * V_{IN}, V_{OUT} = - 3.5V Min. for pulse width less than 20ns.

Truth Table

$\overline{\text{CE}}$	$\overline{\text{OE}}$	Mode	Output pin	V _{CC} current
H	X	Not selected	High Z	I _{SB1} , I _{SB2}
L	H	Output disable	High Z	I _{CC1} , I _{CC2}
L	L	Selected	Data output	I _{CC1} , I _{CC2}

Note) X : "H" or "L"

DC Recommended Operating Conditions (Ta = 0 to + 70 °C, GND = 0V)

Item	Symbol	Min.	Typ.*	Max.	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Input high voltage	V _{IH}	2.2	—	V _{CC} + 0.3	V
Input low voltage	V _{IL}	- 0.3**	—	0.8	V

Note) * V_{CC} = 5V, Ta = 25 °C

** V_{IL} = - 3.0V Min. for pulse width less than 20ns.

Electrical Characteristics

DC characteristics

(V_{CC} = 5V ± 10 %, GND = 0V, Ta = 0 to + 70 °C)

Item	Symbol	Test Condition	Min.	Typ.*	Max.	Unit
Input leakage current	I _{LI}	0V ≤ V _{IN} ≤ V _{CC}	- 1	—	1	μA
Output leakage current	I _{LO}	$\overline{\text{CE}} = \text{V}_{\text{IH}}$ or $\overline{\text{OE}} = \text{V}_{\text{IH}}$ 0V ≤ V _{OUT} ≤ V _{CC}	- 1	—	1	μA
Operating current (DC)	I _{CC1}	$\overline{\text{CE}} = \text{V}_{\text{IL}}$, I _{OUT} = 0mA	—	10	40	mA
Average operating current	I _{CC2}	$\overline{\text{CE}} = \text{V}_{\text{IL}}$, I _{OUT} = 0mA Duty = 100 %, Minimum cycle	—	20	50	mA
Standby current	I _{SB1}	$\overline{\text{CE}} \geq \text{V}_{\text{CC}} - 0.2\text{V}$	—	0.001	30	μA
	I _{SB2}	$\overline{\text{CE}} = \text{V}_{\text{IH}}$	—	0.1	2.0	mA
Output high voltage	V _{OH}	I _{OH} = - 400 μA	2.4	—	—	V
Output low voltage	V _{OL}	I _{OL} = 2.1mA	—	—	0.4	V

Note) * V_{CC} = 5V, Ta = 25 °C

SONY

Input capacitance	C _{IN}	V _{IN} = 0V	—	8	15	pF
Output capacitance	C _{OUT}	V _{OUT} = 0V	—	6	15	pF

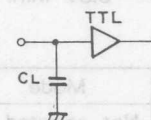
Note) This parameter is sampled and is not 100% tested.

AC characteristics

AC test condition (V_{CC} = 5V ± 10%, T_a = 0 to +70°C)

Item	Condition
Input pulse high level	V _{IH} = 2.4V
Input pulse low level	V _{IL} = 0.6V
Input rise time	t _r = 10ns
Input fall time	t _f = 10ns
Input timing reference level	V _{IL} = V _{IH} = 1.5V
Output timing reference level	V _{OL} = V _{OH} = 1.5V
Output load	C _L * = 100pF, 1TTL

• Test circuit



Note) C_L includes scope and jig capacitances.

AC characteristics

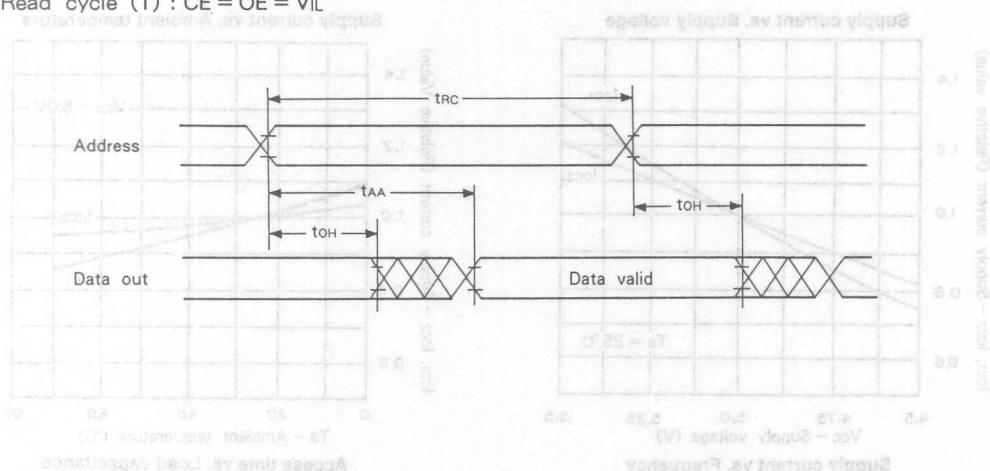
Item	Symbol	Min.	Typ.**	Max.	Unit
Read cycle time	t _{RC}	200	130	—	ns
Address access time	t _{AA}	—	120	200	ns
Chip enable access time	t _{CO}	—	130	200	ns
Output enable access time	t _{OE}	—	40	70	ns
Output data hold time	t _{OH}	0	—	—	ns
Output enable time (from $\overline{CE}$)	t _{LZ}	0	—	—	ns
Output enable time (from $\overline{OE}$)	t _{OLZ}	0	—	—	ns
Output disable time (from $\overline{CE}$)	t _{HZ} *	—	40	70	ns
Output disable time (from $\overline{OE}$)	t _{OHZ} *	—	40	70	ns

Note) * t_{HZ} and t_{OHZ} are defined as the time required for the outputs to turn to high impedance state and are not referred to as output voltage levels.

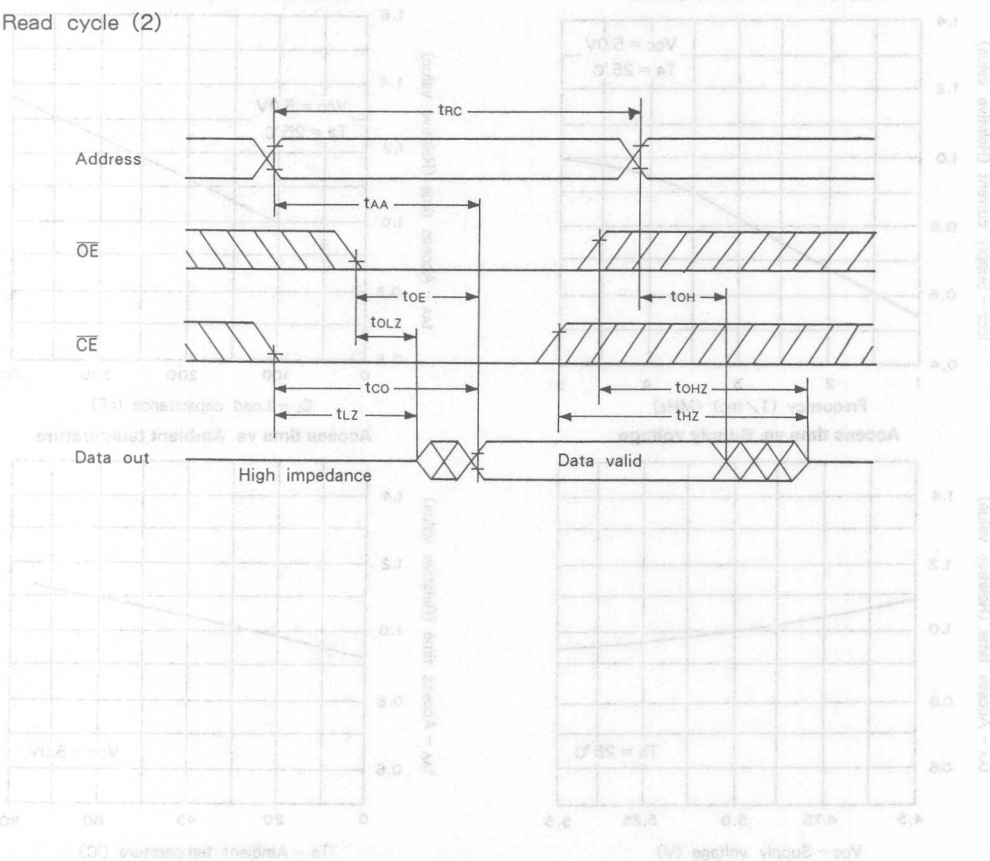
** V_{CC} = 5V, T_a = 25°C

Timing Waveform

- Read cycle (1) : $\overline{CE} = \overline{OE} = V_{IL}$

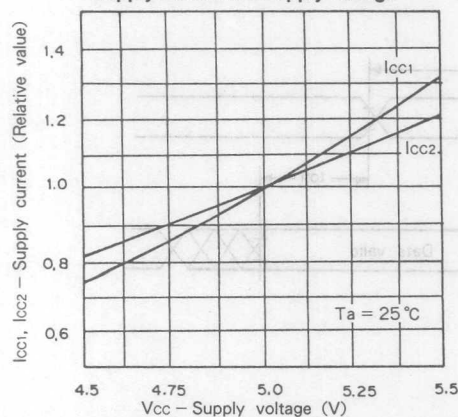


- Read cycle (2)

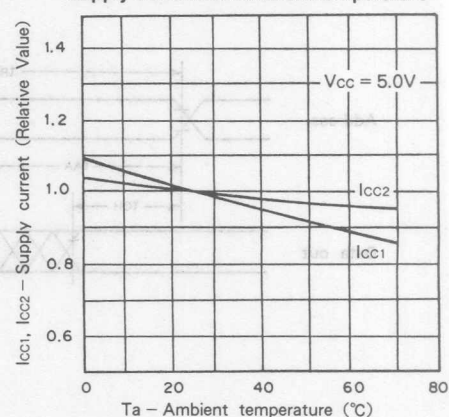


Example of Representative Characteristics

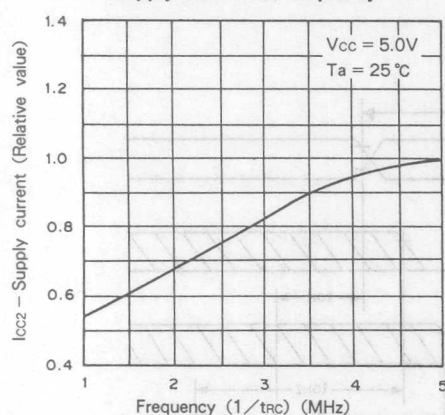
Supply current vs. Supply voltage



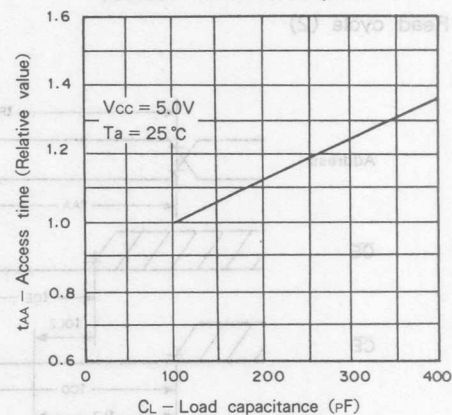
Supply current vs. Ambient temperature



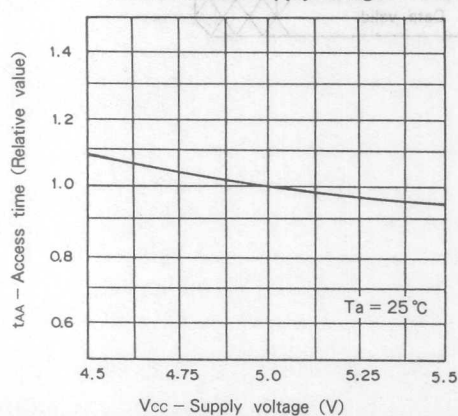
Supply current vs. Frequency



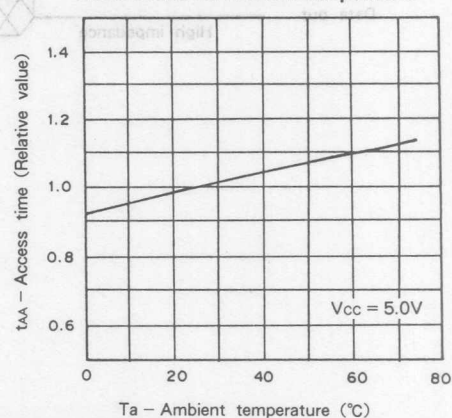
Access time vs. Load capacitance



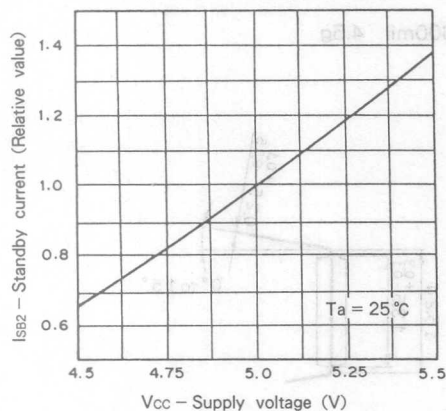
Access time vs. Supply voltage



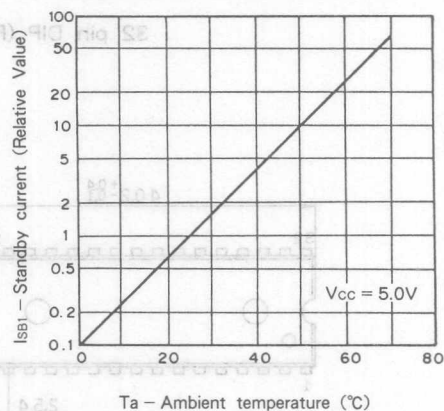
Access time vs. Ambient temperature



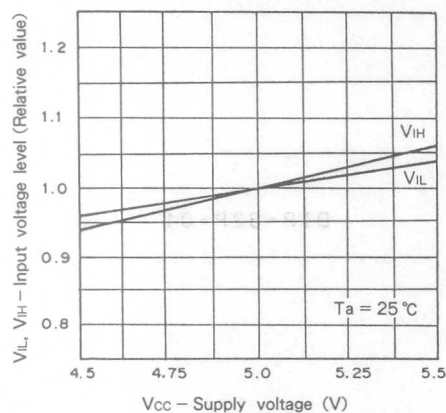
Standby current vs. Supply voltage



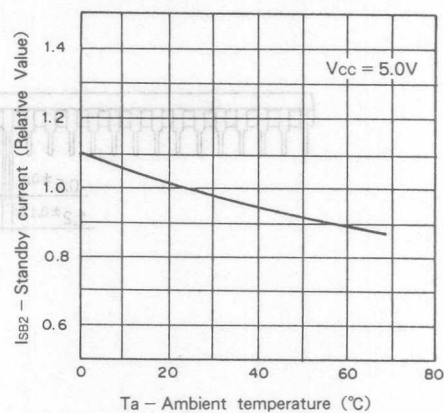
Standby current vs. Ambient temperature



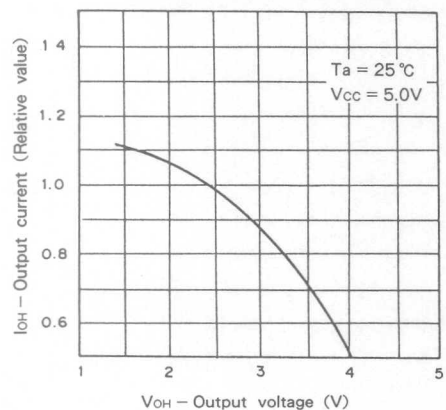
Input voltage level vs. Supply voltage



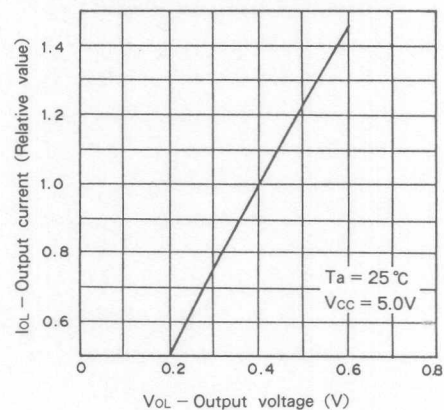
Standby current vs. Ambient temperature



Output current vs. Output voltage



Output current vs. Output voltage



Package Outline Unit : mm

32 pin DIP (Plastic) 600mil 4.5g

